



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1057
Number of Logic Elements/Cells	10570
Total RAM Bits	920448
Number of I/O	335
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s10f484i6n

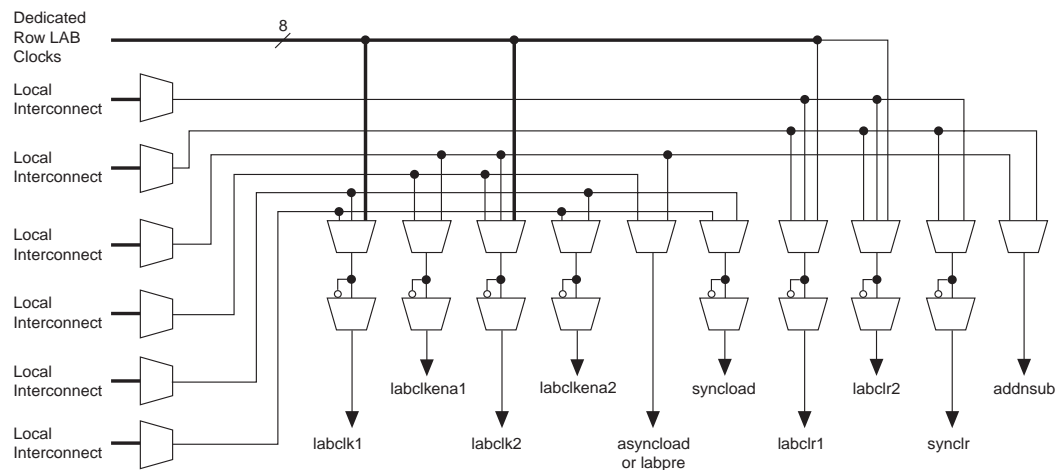
Chapter	Date/Version	Changes Made
2	July 2005 v3.2	<ul style="list-style-type: none"> Added “Clear Signals” section. Updated “Power Sequencing & Hot Socketing” section. Format changes.
	September 2004, v3.1	<ul style="list-style-type: none"> Updated fast regional clock networks description on page 2–73. Deleted the word preliminary from the “specification for the maximum time to relock is 100 μs” on page 2–90. Added information about differential SSTL and HSTL outputs in “External Clock Outputs” on page 2–92. Updated notes in Figure 2–55 on page 2–93. Added information about <i>m</i> counter to “Clock Multiplication & Division” on page 2–101. Updated Note 1 in Table 2–58 on page 2–101. Updated description of “Clock Multiplication & Division” on page 2–88. Updated Table 2–22 on page 2–102. Added references to AN 349 and AN 329 to “External RAM Interfacing” on page 2–115. Table 2–25 on page 2–116: updated the table, updated Notes 3 and 4. Notes 4, 5, and 6, are now Notes 5, 6, and 7, respectively. Updated Table 2–26 on page 2–117. Added information about PCI Compliance to page 2–120. Table 2–32 on page 2–126: updated the table and deleted Note 1. Updated reference to device pin-outs now being available on the web on page 2–130. Added Notes 4 and 5 to Table 2–36 on page 2–130. Updated Note 3 in Table 2–37 on page 2–131. Updated Note 5 in Table 2–41 on page 2–135.
	April 2004, v3.0	<ul style="list-style-type: none"> Added note 3 to rows 11 and 12 in Table 2–18. Deleted “Stratix and Stratix GX Device PLL Availability” table. Added I/O standards row in Table 2–28 that support max and min strength. Row <code>clk [1,3,8,10]</code> was removed from Table 2–30. Added checkmarks in Enhanced column for LVPECL, 3.3-V PCML, LVDS, and HyperTransport technology rows in Table 2–32. Removed the Left and Right I/O Banks row in Table 2–34. Changed RCLK values in Figures 2–50 and 2–51. External RAM Interfacing section replaced.
	November 2003, v2.2	<ul style="list-style-type: none"> Added 672-pin BGA package information in Table 2–37. Removed support for series and parallel on-chip termination. Termination Technology renamed differential on-chip termination. Updated the number of channels per PLL in Tables 2–38 through 2–42. Updated Figures 2–65 and 2–67.
	October 2003, v2.1	<ul style="list-style-type: none"> Updated DDR I information. Updated Table 2–22. Added Tables 2–25, 2–29, 2–30, and 2–72. Updated Figures 2–59, 2–65, and 2–67. Updated the Lock Detect section.

Chapter	Date/Version	Changes Made
4		<ul style="list-style-type: none"> Updated Table 4–123 on page 4–85 through Table 4–126 on page 4–92. Updated Note 3 in Table 4–123 on page 4–85. Table 4–125 on page 4–88: moved to correct order in chapter, and updated table. Updated Table 4–126 on page 4–92. Updated Table 4–127 on page 4–94. Updated Table 4–128 on page 4–95.
	April 2004, v3.0	<ul style="list-style-type: none"> Table 4–129 on page 4–96: updated table and added Note 10. Updated Table 4–131 and Table 4–132 on page 4–100. Updated Table 4–110 on page 4–74. Updated Table 4–123 on page 4–85. Updated Table 4–124 on page 4–87. through Table 4–126 on page 4–92. Added Note 10 to Table 4–129 on page 4–96. Moved Table 4–127 on page 4–94 to correct order in the chapter. Updated Table 4–131 on page 4–100 through Table 4–132 on page 4–100. Deleted t_{XZ} and t_{ZX} from Figure 4–4. Waveform was added to Figure 4–6. The minimum and maximum duty cycle values in Note 3 of Table 4–8 were moved to a new Table 4–9. Changes were made to values in SSTL-3 Class I and II rows in Table 4–17. Note 1 was added to Table 4–34. Added t_{SU_R} and t_{SU_C} rows in Table 4–38. Changed Table 4–55 title from “EP1S10 Column Pin Fast Regional Clock External I/O Timing Parameters” to “EP1S10 External I/O Timing on Column Pins Using Fast Regional Clock Networks.” Changed values in Tables 4–46, 4–48 to 4–51, 4–128, and 4–131. Added t_{ARESET} row in Tables 4–127 to 4–132. Deleted -5 Speed Grade column in Tables 4–117 to 4–119 and 4–122 to 4–123. Fixed differential waveform in Figure 4–1. Added “Definition of I/O Skew” section. Added t_{SU} and t_{CO_C} rows and made changes to values in t_{PRE} and t_{CLKHL} rows in Table 4–46. Values changed in the t_{SU} and t_H rows in Table 4–47. Values changed in the $t_{M4KCLKHL}$ row in Table 4–49. Values changed in the $t_{MRAMCLKHL}$ row in Table 4–50. Added Table 4–51 to “Internal Timing Parameters” section. The timing information is preliminary in Tables 4–55 through 4–96. Table 4–111 was separated into 3 tables: Tables 4–111 to 4–113.
	November 2003, v2.2	<ul style="list-style-type: none"> Updated Tables 4–127 through 4–129.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [7..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. [Figure 2–4](#) shows the LAB control signal generation circuit.

Figure 2–4. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the Stratix architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See [Figure 2–5](#).

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in [Figure 2-7](#), the LAB carry-in signal selects either the carry-in0 or carry-in1 chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums: $\text{data1} + \text{data2} + \text{carry-in0}$ or $\text{data1} + \text{data2} + \text{carry-in1}$. The other two LUTs use the data1 and data2 signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The carry-in0 signal acts as the carry select for the carry-out0 output and carry-in1 acts as the carry select for the carry-out1 output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The addnsub LAB-wide signal controls whether the LE acts as an adder or subtractor.

can drive other R8 interconnects to extend their range as well as C8 interconnects for row-to-row connections. One R8 interconnect is faster than two R4 interconnects connected together.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, TriMatrix memory and DSP blocks, and horizontal IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C8 interconnects traversing a distance of eight blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. [Figure 2-10](#) shows the LUT chain and register chain interconnects.

Table 2–9. M-RAM Block Configurations (True Dual-Port)

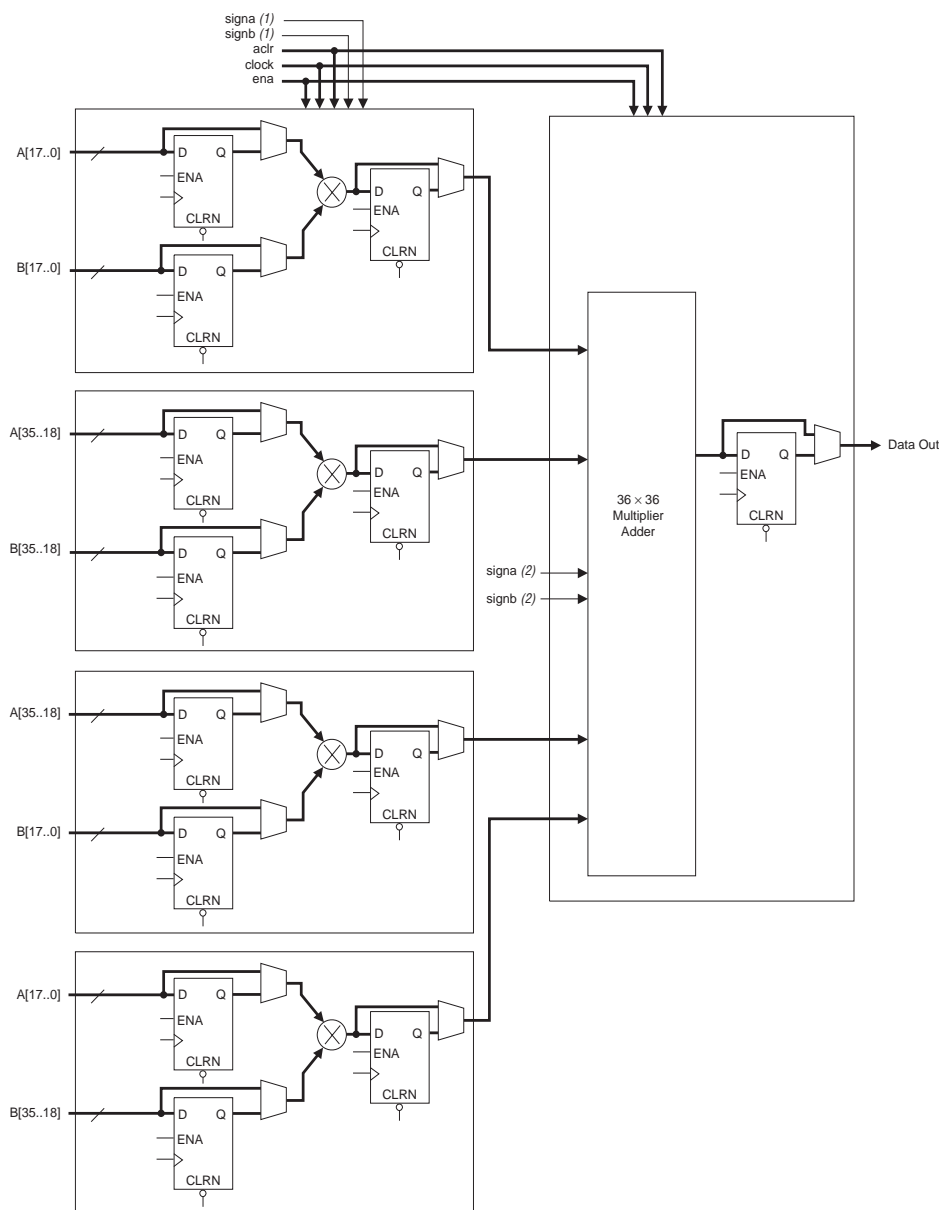
Port A	Port B			
	64K × 9	32K × 18	16K × 36	8K × 72
64K × 9	✓	✓	✓	✓
32K × 18	✓	✓	✓	✓
16K × 36	✓	✓	✓	✓
8K × 72	✓	✓	✓	✓

The read and write operation of the memory is controlled by the **WREN** signal, which sets the ports into either read or write modes. There is no separate read enable (**RE**) signal.

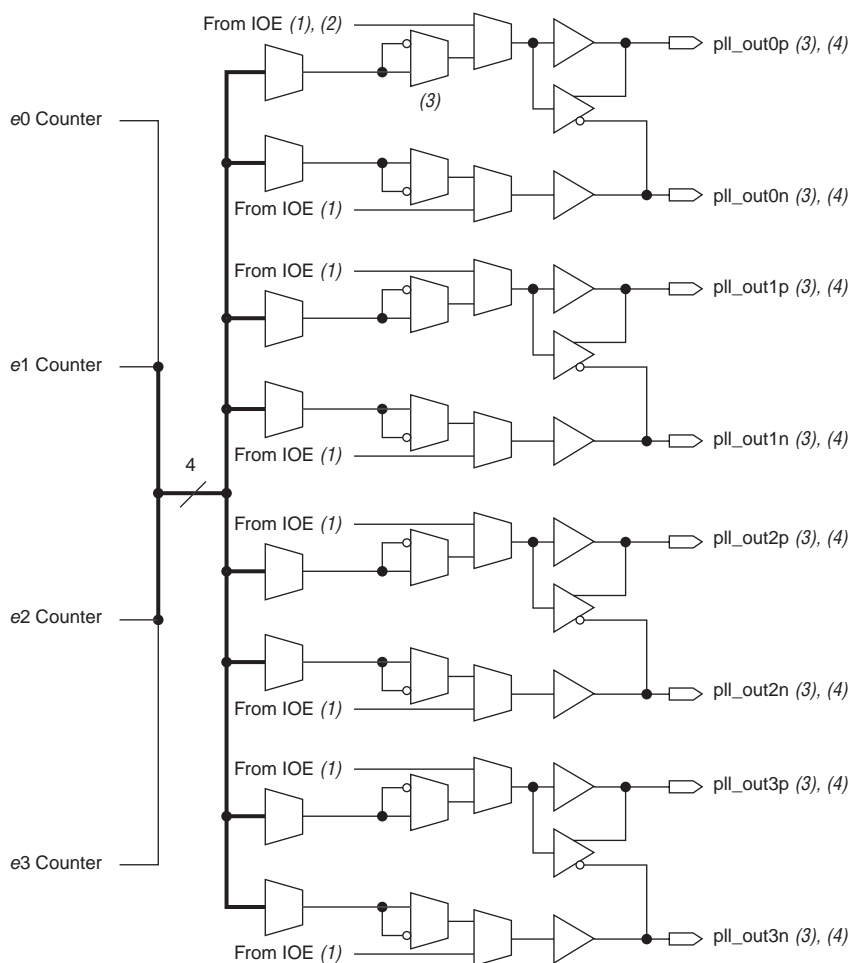
Writing into RAM is controlled by both the **WREN** and byte enable (**byteena**) signals for each port. The default value for the **byteena** signal is high, in which case writing is controlled only by the **WREN** signal. The byte enables are available for the ×18, ×36, and ×72 modes. In the ×144 simple dual-port mode, the two sets of **byteena** signals (**byteena_a** and **byteena_b**) are combined to form the necessary 16 byte enables. Tables 2–10 and 2–11 summarize the byte selection.

Table 2–10. Byte Enable for M-RAM Blocks *Notes (1), (2)*

byteena[3..0]	datain ×18	datain ×36	datain ×72
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

Figure 2–36. 36×36 Multiply Mode**Notes to Figure 2–36:**

- (1) These signals are not registered or registered once to match the pipeline.
- (2) These signals are not registered, registered once, or registered twice for latency to match the pipeline.

Figure 2–55. External Clock Outputs for PLLs 5 & 6**Notes to Figure 2–55:**

- (1) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with IOE outputs.
- (2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.
- (3) EP1S10, EP1S20, and EP1S25 devices in 672-pin BGA and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., pll_out0p, pll_out0n, pll_out1p, and pll_out1n).
- (4) Differential SSTL and HSTL outputs are implemented using two single-ended output buffers, which are programmed to have opposite polarity.

The `pllenable` pin is a dedicated pin that enables/disables PLLs. When the `pllenable` pin is low, the clock output ports are driven by GND and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the `pllenable` signal by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

The `areset` signals are reset/resynchronization inputs for each PLL. The `areset` signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the `areset` signal in designs if any of the following conditions are true:

- PLL Reconfiguration or Clock switchover enables in the design.
- Phase relationships between output clocks need to be maintained after a loss of lock condition

The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value than desired as the PLL locks. If the system cannot tolerate this, the `clkena` signal can disable the output clocks until the PLL locks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or a `clkloss` status signal to trigger `pfdena`.

The `clkena` signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own `clkena` signal. The `clkena` signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the `g` and `l` counters. The `clkena` signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. [Figure 2-57](#) shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a

External Clock Inputs

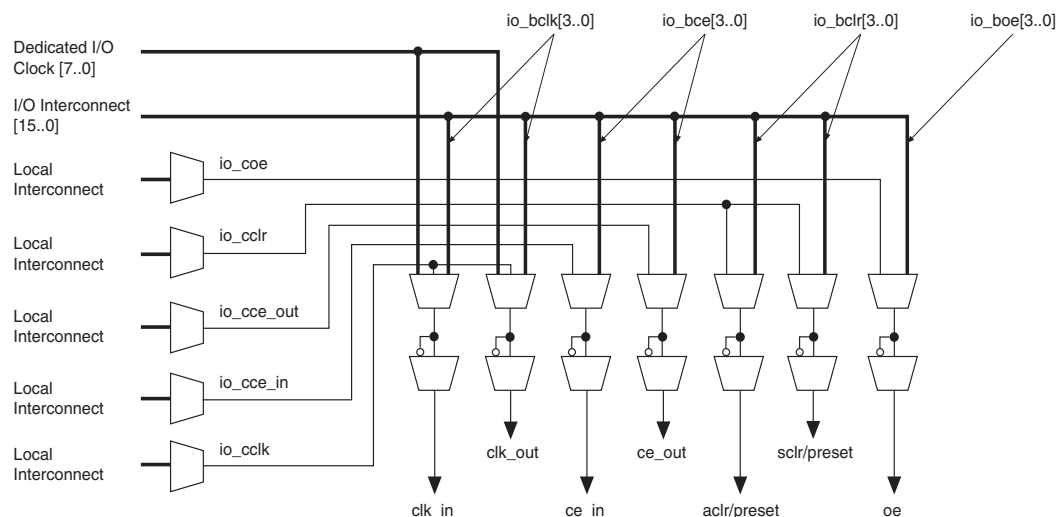
Each fast PLL supports single-ended or differential inputs for source synchronous transmitters or for general-purpose use. Source-synchronous receivers support differential clock inputs. The fast PLL inputs are fed by CLK [0 . . 3], CLK [8 . . 11], and FPLL [7 . . 10] CLK pins, as shown in [Figure 2–50 on page 2–85](#).

[Table 2–22](#) shows the I/O standards supported by fast PLL input pins.

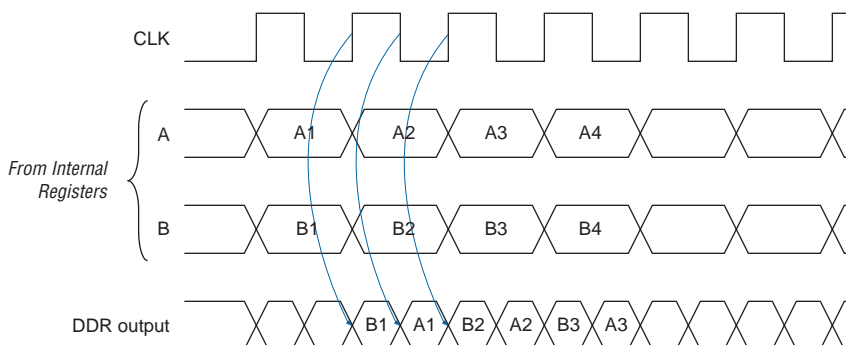
Table 2–22. Fast PLL Port I/O Standards (Part 1 of 2)		
I/O Standard	Input	
	INCLK	PLENABLE
LVTTTL	✓	✓
LVC MOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X 1.0		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	
Differential SSTL		
3.3-V GTL		
3.3-V GTL+	✓	
1.5-V HSTL Class I	✓	
1.5-V HSTL Class II		
1.8-V HSTL Class I	✓	
1.8-V HSTL Class II		
SSTL-18 Class I	✓	
SSTL-18 Class II		
SSTL-2 Class I	✓	

Each IOE contains its own control signal selection for the following control signals: oe, ce_in, ce_out, aclr/preset, sclr/preset, clk_in, and clk_out. Figure 2-63 illustrates the control signal selection.

Figure 2-63. Control Signal Selection per IOE



In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2-64 shows the IOE in bidirectional configuration.

Figure 2–68. Output Timing Diagram in DDR Mode

The Stratix IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

Stratix devices support DDR SDRAM at up to 200 MHz (400-Mbps data rate) through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces up to 200 MHz. Stratix devices also provide preliminary support for reduced latency DRAM II (RLDRAM II) at rates up to 200 MHz through the dedicated phase-shift circuitry.



In addition to the required signals for external memory interfacing, Stratix devices offer the optional clock enable signal. By default the Quartus II software sets the clock enable signal high, which tells the output register to update with new values. The output registers hold their own values if the design sets the clock enable signal low. See [Figure 2–64](#).



To find out more about the DDR SDRAM specification, see the JEDEC web site (www.jedec.org). For information on memory controller megafunctions for Stratix devices, see the Altera web site (www.altera.com). See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices* for more information on DDR SDRAM interface in Stratix. Also see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices* and *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

- 1.8-V HSTL Class I and II
- SSTL-3 Class I and II
- SSTL-2 Class I and II
- SSTL-18 Class I and II
- CTT

Table 2–31 describes the I/O standards supported by Stratix devices.

Table 2–31. Stratix Supported I/O Standards				
I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTTL	Single-ended	N/A	3.3	N/A
LVC MOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X 1.0	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL (1)	Differential	0.75	1.5	0.75
Differential SSTL (2)	Differential	1.25	2.5	1.25
GTL	Voltage-referenced	0.8	N/A	1.20
GTL+	Voltage-referenced	1.0	N/A	1.5
1.5-V HSTL Class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL Class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 Class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 Class I and II	Voltage-referenced	1.25	2.5	1.25
SSTL-3 Class I and II	Voltage-referenced	1.5	3.3	1.5
AGP (1× and 2°)	Voltage-referenced	1.32	3.3	N/A
CTT	Voltage-referenced	1.5	3.3	1.5

Notes to Table 2–31:

- (1) This I/O standard is only available on input and output clock pins.
 (2) This I/O standard is only available on output column clock pins.

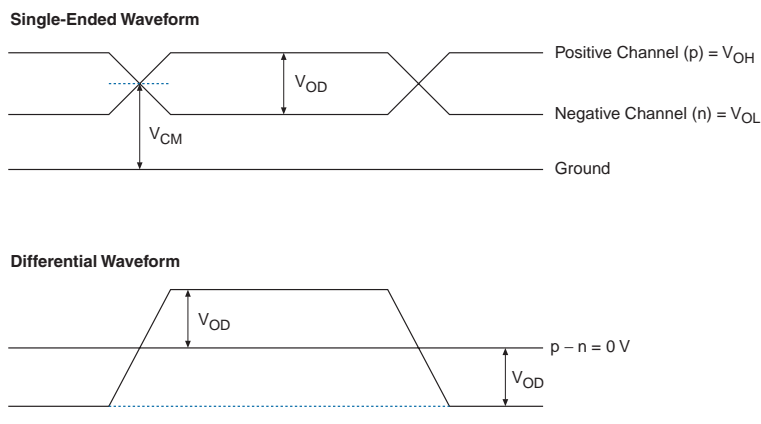
Table 3–1. Stratix JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST (1)	00 0000 0000	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ (1)	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP (1)	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring an Stratix device via the JTAG port with a MasterBlaster™, ByteBlasterMV™, or ByteBlaster™ II download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction will hold nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Note to Table 3–1:

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

Figure 4–2. Transmitter Output Waveforms for Differential I/O Standards



Tables 4–10 through 4–33 recommend operating conditions, DC operating conditions, and capacitance for 1.5-V Stratix devices.

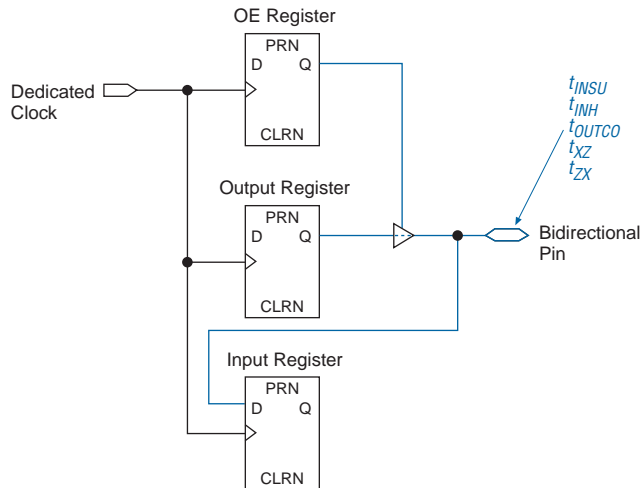
Table 4–10. 3.3-V LVDS I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} (6)	Input differential voltage swing (single-ended)	$0.1 \text{ V} \leq V_{CM} < 1.1 \text{ V}$ $W = 1$ through 10	300		1,000	mV
		$1.1 \text{ V} \leq V_{CM} \leq 1.6 \text{ V}$ $W = 1$	200		1,000	mV
		$1.1 \text{ V} \leq V_{CM} \leq 1.6 \text{ V}$ $W = 2$ through 10	100		1,000	mV
		$1.6 \text{ V} < V_{CM} \leq 1.8 \text{ V}$ $W = 1$ through 10	300		1,000	mV

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4-4 shows the pin-to-pin timing model for bidirectional IOE pin timing. All registers are within the IOE.

Figure 4-4. External Timing in Stratix Devices



All external timing parameters reported in this section are defined with respect to the dedicated clock pin as the starting point. All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the 24-mA current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4-103 through 4-108.

Table 4–118. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[10..7]CLK Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVC MOS	422	390	390	MHz
GTL+	250	200	200	MHz
SSTL-3 Class I	350	300	300	MHz
SSTL-3 Class II	350	300	300	MHz
SSTL-2 Class I	350	300	300	MHz
SSTL-2 Class II	350	300	300	MHz
SSTL-18 Class I	350	300	300	MHz
SSTL-18 Class II	350	300	300	MHz
1.5-V HSTL Class I	350	300	300	MHz
1.8-V HSTL Class I	350	300	300	MHz
CTT	250	200	200	MHz
Differential 1.5-V HSTL C1	350	300	300	MHz
LVPECL (1)	717	640	640	MHz
PCML (1)	375	350	350	MHz
LVDS (1)	717	640	640	MHz
HyperTransport technology (1)	717	640	640	MHz

Table 4–119. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Wire-Bond Packages (Part 1 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz
LVC MOS	422	390	390	MHz
GTL+	250	200	200	MHz
SSTL-3 Class I	350	300	300	MHz
SSTL-3 Class II	350	300	300	MHz
SSTL-2 Class I	350	300	300	MHz
SSTL-2 Class II	350	300	300	MHz

Table 4–120. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Flip-Chip Packages (Part 2 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
SSTL-2 Class II (3)	200	200	167	167	MHz
SSTL-2 Class II (4)	200	200	167	167	MHz
SSTL-2 Class II (5)	150	134	134	134	MHz
SSTL-18 Class I	150	133	133	133	MHz
SSTL-18 Class II	150	133	133	133	MHz
1.5-V HSTL Class I	250	225	200	200	MHz
1.5-V HSTL Class II	225	200	200	200	MHz
1.8-V HSTL Class I	250	225	200	200	MHz
1.8-V HSTL Class II	225	200	200	200	MHz
3.3-V PCI	350	300	250	250	MHz
3.3-V PCI-X 1.0	350	300	250	250	MHz
Compact PCI	350	300	250	250	MHz
AGP 1×	350	300	250	250	MHz
AGP 2×	350	300	250	250	MHz
CTT	200	200	200	200	MHz
Differential 1.5-V HSTL C1	225	200	200	200	MHz
Differential 1.8-V HSTL Class I	250	225	200	200	MHz
Differential 1.8-V HSTL Class II	225	200	200	200	MHz
Differential SSTL-2 (6)	200	200	167	167	MHz
LVPECL (2)	500	500	500	500	MHz
PCML (2)	350	350	350	350	MHz
LVDS (2)	500	500	500	500	MHz
HyperTransport technology (2)	350	350	350	350	MHz

Table 4–133. Fast PLL Specifications for -8 Speed Grades (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{ARESET}	Minimum pulse width on areset signal	10		ns

Notes to Tables 4–131 through 4–133:

- (1) See “Maximum Input & Output Clock Rates” on page 4–76.
- (2) PLLs 7, 8, 9, and 10 in the EP1S80 device support up to 717-MHz input and output.
- (3) Use this equation ($f_{\text{OUT}} = f_{\text{IN}} * ml(n \times \text{post-scale counter})$) in conjunction with the specified f_{INPFD} and f_{VCO} ranges to determine the allowed PLL settings.
- (4) When using the SERDES, high-speed differential I/O mode supports a maximum output frequency of 210 MHz to the global or regional clocks (that is, the maximum data rate 840 Mbps divided by the smallest SERDES J factor of 4).
- (5) Refer to the section “High-Speed I/O Specification” on page 4–87 for more information.
- (6) This parameter is for high-speed differential I/O mode only.
- (7) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16.
- (8) High-speed differential I/O mode supports $W = 1$ to 16 and $J = 4, 7, 8$, or 10.

DLL Specifications

Table 4–134 reports the jitter for the DLL in the DQS phase shift reference circuit.

Table 4–134. DLL Jitter for DQS Phase Shift Reference Circuit

Frequency (MHz)	DLL Jitter (ps)
197 to 200	± 100
160 to 196	± 300
100 to 159	± 500



For more information on DLL jitter, see the *DDR SRAM* section in the *Stratix Architecture* chapter of the *Stratix Device Handbook, Volume 1*.

Table 4–135 lists the Stratix DLL low frequency limit for full phase shift across all PVT conditions. The Stratix DLL can be used below these frequencies, but it will not achieve the full phase shift requested across all