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# Understanding <u>Embedded - FPGAs (Field Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1057
Number of Logic Elements/Cells	10570
Total RAM Bits	920448
Number of I/O	345
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s10f672i7n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1–5. Stratix FineLine BGA Package Sizes										
Dimension	484 Pin	672 Pin	780 Pin	1,020 Pin	1,508 Pin					
Pitch (mm)	1.00	1.00	1.00	1.00	1.00					
Area (mm²)	529	729	841	1,089	1,600					
$\begin{array}{c} \text{Length} \times \text{width} \\ \text{(mm} \times \text{mm)} \end{array}$	23 × 23	27 × 27	29 × 29	33 × 33	40 × 40					

Stratix devices are available in up to four speed grades, -5, -6, -7, and -8, with -5 being the fastest. Table 1–6 shows Stratix device speed-grade offerings.

Table 1–6.	Table 1–6. Stratix Device Speed Grades											
Device	672-Pin BGA	956-Pin BGA	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA					
EP1S10	-6, -7		-5, -6, -7	-6, -7	-5, -6, -7							
EP1S20	-6, -7		-5, -6, -7	-6, -7	-5, -6, -7							
EP1S25	-6, -7			-6, -7, -8	-5, -6, -7	-5, -6, -7						
EP1S30		-5, -6, -7			-5, -6, -7, -8	-5, -6, -7						
EP1S40		-5, -6, -7			-5, -6, -7, -8	-5, -6, -7	-5, -6, -7					
EP1S60		-6, -7				-5, -6, -7	-6, -7					
EP1S80		-6, -7				-5, -6, -7	-5, -6, -7					

With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [7..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack $^{\text{IM}}$  interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

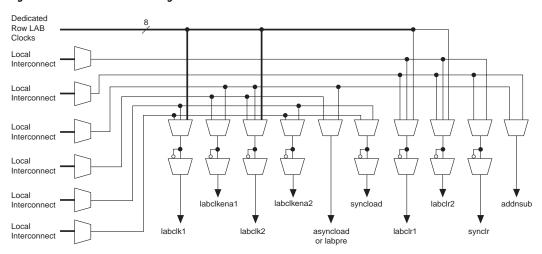


Figure 2-4. LAB-Wide Control Signals

# **Logic Elements**

The smallest unit of logic in the Stratix architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 2–5.

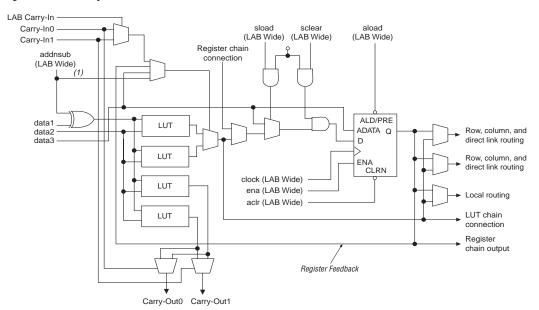


Figure 2-7. LE in Dynamic Arithmetic Mode

*Note to Figure 2–7:* 

(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

#### Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel precomputation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

M512 RAM blocks can have different clocks on its inputs and outputs. The wren, datain, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, rden, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The eight labelk signals or local interconnect can drive the inclock, outclock, wren, rden, inclr, and outclr signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, LEs can also control the wren and rden signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–15 shows the M512 RAM block control signal generation logic.

The RAM blocks within Stratix devices have local interconnects to allow LEs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Up to 10 direct link input connections to the M512 RAM block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through 10 direct link interconnects. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–16 shows the M512 RAM block to logic array interface.

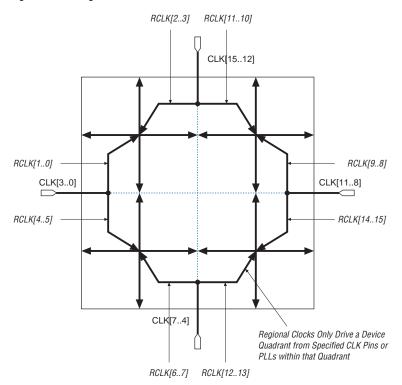


Figure 2-43. Regional Clocks

#### Fast Regional Clock Network

In EP1S25, EP1S20, and EP1S10 devices, there are two fast regional clock networks, FCLK [1..0], within each quadrant, fed by input pins that can connect to fast regional clock networks (see Figure 2–44). In EP1S30 and larger devices, there are two fast regional clock networks within each half-quadrant (see Figure 2–45). Dual-purpose FCLK pins drive the fast clock networks. All devices have eight FCLK pins to drive fast regional clock networks. Any I/O pin can drive a clock or control signal onto any fast regional clock network with the addition of a delay. This signal is driven via the I/O interconnect. The fast regional clock networks can also be driven from internal logic elements.

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each pair of output pins (four pins total) has dedicated VCC and GND pins to reduce the output clock's overall jitter by providing improved isolation from switching I/O pins.

For PLLs 5 and 6, each pin of a single-ended output pair can either be in phase or 180° out of phase. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, 3.3-V PCML, HyperTransport technology, differential HSTL, and differential SSTL. Table 2–20 shows which I/O standards the enhanced PLL clock pins support. When in single-ended or differential mode, the two outputs operate off the same power supply. Both outputs use the same standards in single-ended mode to maintain performance. You can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

Table 2–20. I/O Standards Supported for Enhanced PLL Pins (Part 1 of 2)									
L/O Ctondovd		Output							
I/O Standard	INCLK	FBIN	PLLENABLE	EXTCLK					
LVTTL	<b>✓</b>	<b>✓</b>	<b>✓</b>	✓					
LVCMOS	<b>✓</b>	<b>✓</b>	✓	✓					
2.5 V	<b>✓</b>	<b>✓</b>		✓					
1.8 V	<b>✓</b>	<b>✓</b>		✓					
1.5 V	<b>✓</b>	<b>✓</b>		✓					
3.3-V PCI	<b>✓</b>	<b>✓</b>		✓					
3.3-V PCI-X 1.0	<b>✓</b>	<b>✓</b>		✓					
LVPECL	<b>✓</b>	<b>✓</b>		✓					
3.3-V PCML	<b>✓</b>	<b>✓</b>		✓					
LVDS	<b>✓</b>	<b>✓</b>		✓					
HyperTransport technology	<b>✓</b>	<b>✓</b>		✓					
Differential HSTL	<b>✓</b>			✓					
Differential SSTL				✓					
3.3-V GTL	<b>✓</b>	✓		✓					
3.3-V GTL+	<b>✓</b>	✓		✓					
1.5-V HSTL Class I	<b>✓</b>	✓		✓					

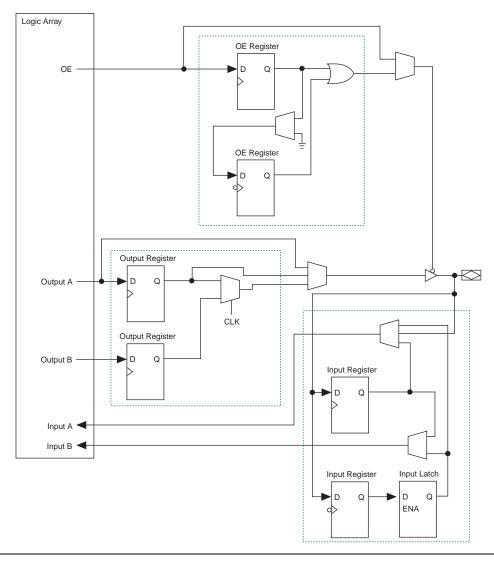


Figure 2-59. Stratix IOE Structure

The IOEs are located in I/O blocks around the periphery of the Stratix device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–60 shows how a row I/O block connects to the logic array. Figure 2–61 shows how a column I/O block connects to the logic array.

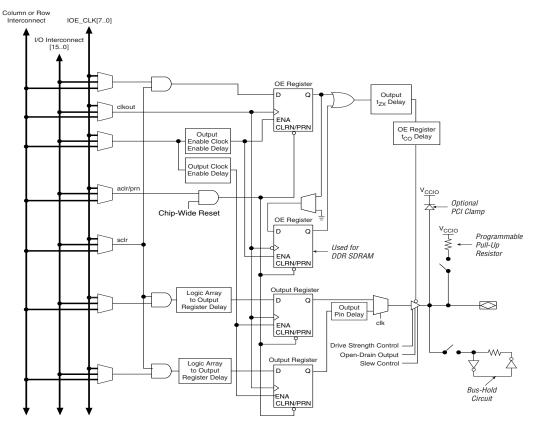


Figure 2–67. Stratix IOE in DDR Output I/O Configuration Notes (1), (2)

*Notes to Figure 2–67:* 

- (1) All input signals to the IOE can be inverted at the IOE.
- (2) The tristate is by default active high. It can, however, be designed to be active low.

Tables 2–25 and 2–26 show the performance specification for DDR SDRAM, RLDRAM II, QDR SRAM, QDRII SRAM, and ZBT SRAM interfaces in EP1S10 through EP1S40 devices and in EP1S60 and EP1S80 devices. The DDR SDRAM and QDR SRAM numbers in Table 2–25 have been verified with hardware characterization with third-party DDR SDRAM and QDR SRAM devices over temperature and voltage extremes.

Table 2–25. External RAM Support in EP1S10 through EP1S40 Devices											
			Maximum Clock Rate (MHz)								
DDR Memory Type	I/O Standard	-5 Speed Grade	-6 Spee	d Grade	ed Grade	-8 Speed Grade					
		Flip-Chip	Flip-Chip	Wire- Bond	Flip- Chip	Wire- Bond	Flip- Chip	Wire- Bond			
DDR SDRAM (1), (2)	SSTL-2	200	167	133	133	100	100	100			
DDR SDRAM - side banks (2), (3), (4)	SSTL-2	150	133	110	133	100	100	100			
RLDRAM II (4)	1.8-V HSTL	200	(5)	(5)	(5)	(5)	(5)	(5)			
QDR SRAM (6)	1.5-V HSTL	167	167	133	133	100	100	100			
QDRII SRAM (6)	1.5-V HSTL	200	167	133	133	100	100	100			
ZBT SRAM (7)	LVTTL	200	200	200	167	167	133	133			

#### Notes to Table 2-25:

- (1) These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).
- (2) For more information on DDR SDRAM, see AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.
- (3) DDR SDRAM is supported on the Stratix device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.
- (4) These performance specifications are preliminary.
- (5) This device does not support RLDRAM II.
- (6) For more information on QDR or QDRII SRAM, see AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices.
- (7) For more information on ZBT SRAM, see AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices.

Table 2-27.	DQS & DQ Bus Mode Support	(Part 2 of 2) Note (	1)	
Device	Package	Number of ×8 Groups	Number of ×16 Groups	Number of ×32 Groups
EP1S25	672-pin BGA 672-pin FineLine BGA	16 (3)	8	4
	780-pin FineLine BGA 1,020-pin FineLine BGA	20	8	4
EP1S30	956-pin BGA 780-pin FineLine BGA 1,020-pin FineLine BGA	20	8	4
EP1S40	956-pin BGA 1,020-pin FineLine BGA 1,508-pin FineLine BGA	20	8	4
EP1S60	956-pin BGA 1,020-pin FineLine BGA 1,508-pin FineLine BGA	20	8	4
EP1S80	956-pin BGA 1,508-pin FineLine BGA 1,923-pin FineLine BGA	20	8	4

#### *Notes to Table 2–27:*

- See the Selectable I/O Standards in Stratix & Stratix GX Devices chapter in the Stratix Device Handbook, Volume 2 for V<sub>RFF</sub> guidelines.
- (2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.
- (3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.
- (4) This package has nine groups in I/O banks 3 and 4 and nine groups in I/O banks 7 and 8.
- (5) These packages have three groups in I/O banks 3 and 4 and four groups in I/O banks 7 and 8.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Two separate single phase-shifting reference circuits are located on the top and bottom of the Stratix device. Each circuit is driven by a system reference clock through the CLK pins that is the same frequency as the DQS signal. Clock pins CLK [15..12] p feed the phase-shift circuitry on the top of the device and clock pins CLK [7..4] p feed the phase-shift circuitry on the bottom of the device. The phase-shifting reference circuit on the top of the device controls the compensated delay elements for all 10 DQS pins located at the top of the device. The phase-shifting reference circuit on the bottom of the device controls the compensated delay elements for all 10 DQS pins located on the bottom of the device. All 10 delay elements (DQS signals) on either the top or bottom of the device

#### **Programmable Pull-Up Resistor**

Each Stratix device I/O pin provides an optional programmable pull-up resistor during user mode. If this feature is enabled for an I/O pin, the pull-up resistor (typically 25 k $\Omega$ ) weakly holds the output to the V<sub>CCIO</sub> level of the output pin's bank. Table 2–30 shows which pin types support the weak pull-up resistor feature.

Table 2–30. Programmable Weak Pull-Up Resistor Support								
Pin Type	Programmable Weak Pull-Up Resistor							
I/O pins	✓							
CLK[150]								
FCLK	~							
FPLL[710]CLK								
Configuration pins								
JTAG pins	<b>√</b> (1)							

*Note to Table 2–30:* 

(1) TDO pins do not support programmable weak pull-up resistors.

#### Advanced I/O Standard Support

Stratix device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP (1× and 2×)
- LVDS
- LVPECL
- 3.3-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output column clock pins only)
- GTL/GTL+
- 1.5-V HSTL Class I and II

- 1.8-V HSTL Class I and II
- SSTL-3 Class I and II
- SSTL-2 Class I and II
- SSTL-18 Class I and II
- CTT

Table 2–31 describes the I/O standards supported by Stratix devices.

Table 2–31. Stratix Supp	orted I/O Standards			
I/O Standard	Туре	Input Reference Voltage (V <sub>REF</sub> ) (V)	Output Supply Voltage (V <sub>CCIO</sub> ) (V)	Board Termination Voltage (V <sub>TT</sub> ) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X 1.0	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL (1)	Differential	0.75	1.5	0.75
Differential SSTL (2)	Differential	1.25	2.5	1.25
GTL	Voltage-referenced	0.8	N/A	1.20
GTL+	Voltage-referenced	1.0	N/A	1.5
1.5-V HSTL Class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL Class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 Class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 Class I and II	Voltage-referenced	1.25	2.5	1.25
SSTL-3 Class I and II	Voltage-referenced	1.5	3.3	1.5
AGP (1× and 2°)	Voltage-referenced	1.32	3.3	N/A
CTT	Voltage-referenced	1.5	3.3	1.5

#### Notes to Table 2–31:

- (1) This I/O standard is only available on input and output clock pins.
- (2) This I/O standard is only available on output column clock pins.

Table 2-40.	EP1S60 Diffe	rential Chai	nnels (Part 2	? of 2) /	lote (1)						
	Transmitter/	Total	Maximum	C	enter F	ast PLI	.s	Corner Fast PLLs (2), (3)			
Package	Receiver	Channels	Speed (Mbps)	PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
1,020-pin FineLine	Transmitter (4)	80 (12) <i>(7)</i>	840	12 (2)	10 (4)	10 (4)	12 (2)	20	20	20	20
BGA			840 (5), (8)	22 (6)	22 (6)	22 (6)	22 (6)	20	20	20	20
	Receiver	80 (10) <i>(7)</i>	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5), (8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)
1,508-pin FineLine	Transmitter (4)	80 (36) <i>(7)</i>	840	12 (8)	10 (10)	10 (10)	12 (8)	20	20	20	20
BGA			840 (5),(8)	22 (18)	22 (18)	22 (18)	22 (18)	20	20	20	20
	Receiver	80 (36) (7)	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5),(8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)

Table 2-41.	Table 2–41. EP1S80 Differential Channels (Part 1 of 2) Note (1)											
	Transmitter/	Total	Maximum	C	enter F	ast PLI	-S	Corr	ner Fas	t PLLs (2	2), (3)	
Package R	Receiver	Channels	Speed (Mbps)	PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10	
956-pin	Transmitter	80 (40)	840	10	10	10	10	20	20	20	20	
BGA	(4)	(7)	840 (5),(8)	20	20	20	20	20	20	20	20	
	Receiver	80	840	20	20	20	20	10	10	10	10	
			840 (5),(8)	40	40	40	40	10	10	10	10	
1,020-pin FineLine		92 (12) <i>(7)</i>	840	10 (2)	10 (4)	10 (4)	10 (2)	20	20	20	20	
BGA			840 (5),(8)	20 (6)	20 (6)	20 (6)	20 (6)	20	20	20	20	
	Receiver	90 (10) <i>(7)</i>	840	20	20	20	20	10 (2)	10 (3)	10 (3)	10 (2)	
			840 (5),(8)	40	40	40	40	10 (2)	10 (3)	10 (3)	10 (2)	

configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix devices to be reconfigured incircuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 2 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to  $V_{\rm CC}$ , the POR time is 2 ms.

The nio\_pullup pin enables a built-in weak pull-up resistor to pull all user I/O pins to  $V_{CCIO}$  before and during device configuration. If nio\_pullup is connected to  $V_{CC}$  during configuration, the weak pull-ups on all user I/O pins are disabled. If connected to ground, the pull-ups are enabled during configuration. The nio\_pullup pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

VCCSEL is a dedicated input that is used to choose whether all dedicated configuration and JTAG input pins can accept 1.5 V/1.8 V or 2.5 V/3.3 V during configuration. A logic low sets 3.3 V/2.5 V, and a logic high sets 1.8 V/1.5 V. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, PLL\_ENA, CONF\_DONE, nSTATUS. The VCCSEL pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

The VCCSEL signal does not control the dual-purpose configuration pins such as the DATA [7..0] and PPA pins (nws, nrs, cs, nrcs, and RDYnbsy). During configuration, these dual-purpose pins will drive out voltage levels corresponding to the  $V_{\rm CCIO}$  supply voltage that powers the I/O bank containing the pin. After configuration, the dual-purpose pins use I/O standards specified in the user design.

TDO and nCEO drive out at the same voltages as the  $V_{CCIO}$  supply that powers the I/O bank containing the pin. Users must select the  $V_{CCIO}$  supply for bank containing TDO accordingly. For example, when using the ByteBlaster MV cable, the  $V_{CCIO}$  for the bank containing TDO must be powered up at 3.3 V.

# **External I/O Delay Parameters**

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density. All of the timing parameters in this section apply to both flip-chip and wire-bond packages.

Tables 4–103 and 4–104 show the input adder delays associated with column and row I/O pins. If an I/O standard is selected other than 3.3-V LVTTL or LVCMOS, add the selected delay to the external  $t_{\rm INSUPLL}$  I/O parameters shown in Tables 4–54 through 4–96.

D	-5 Spec	ed Grade	-6 Spee	ed Grade	-7 Spee	ed Grade	-8 Spee	d Grade	11-24
Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit
LVCMOS		0		0		0		0	ps
3.3-V LVTTL		0		0		0		0	ps
2.5-V LVTTL		19		19		22		26	ps
1.8-V LVTTL		221		232		266		313	ps
1.5-V LVTTL		352		369		425		500	ps
GTL		-45		-48		-55		-64	ps
GTL+		-75		-79		-91		-107	ps
3.3-V PCI		0		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0		0	ps
Compact PCI		0		0		0		0	ps
AGP 1×		0		0		0		0	ps
AGP 2×		0		0		0		0	ps
CTT		120		126		144		170	ps
SSTL-3 Class I		-162		-171		-196		-231	ps
SSTL-3 Class II		-162		-171		-196		-231	ps
SSTL-2 Class I		-202		-213		-244		-287	ps
SSTL-2 Class II		-202		-213		-244		-287	ps
SSTL-18 Class I		78		81		94		110	ps
SSTL-18 Class II		78		81		94		110	ps
1.5-V HSTL Class I		-76		-80		-92		-108	ps
1.5-V HSTL Class II		-76		-80		-92		-108	ps
1.8-V HSTL Class I		-52		-55		-63		-74	ps
1.8-V HSTL Class II		-52		-55		-63		-74	ps

Table 4–121. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	400	350	300	300	MHz
2.5 V	400	350	300	300	MHz
1.8 V	400	350	300	300	MHz
1.5 V	350	300	300	300	MHz
LVCMOS	400	350	300	300	MHz
GTL	200	167	125	125	MHz
GTL+	200	167	125	125	MHz
SSTL-3 Class I	167	150	133	133	MHz
SSTL-3 Class II	167	150	133	133	MHz
SSTL-2 Class I	150	133	133	133	MHz
SSTL-2 Class II	150	133	133	133	MHz
SSTL-18 Class I	150	133	133	133	MHz
SSTL-18 Class II	150	133	133	133	MHz
1.5-V HSTL Class I	250	225	200	200	MHz
1.5-V HSTL Class II	225	225	200	200	MHz
1.8-V HSTL Class I	250	225	200	200	MHz
1.8-V HSTL Class II	225	225	200	200	MHz
3.3-V PCI	250	225	200	200	MHz
3.3-V PCI-X 1.0	225	225	200	200	MHz
Compact PCI	400	350	300	300	MHz
AGP 1×	400	350	300	300	MHz
AGP 2×	400	350	300	300	MHz
CTT	300	250	200	200	MHz
LVPECL (2)	717	717	500	500	MHz
PCML (2)	420	420	420	420	MHz
LVDS (2)	717	717	500	500	MHz
HyperTransport technology (2)	420	420	420	420	MHz



# 5. Reference & Ordering Information

\$51005-2.1

## Software

Stratix® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

## **Device Pin-Outs**

Stratix device pin-outs can be found on the Altera web site (www.altera.com).

# Ordering Information

Figure 5–1 describes the ordering codes for Stratix devices. For more information on a specific package, see the *Package Information for Stratix Devices* chapter.

Global & Hierarchical Clocking 2–73	Packages 4–81
Global & Regional Clock Connections	Wire-Bond
from Side Pins & Fast PLL Outputs 2–85	
from Top Clock Pins & Enhanced PLL	Packages 4-84
Outputs 2–86	Phase & Delay Shifting 2–96
Global Clock External I/O Timing	Phase Delay 2–96
Parameters 4–35	PLL Clock Networks 2–73
Global Clock Network 2–74	Read/Write Clock Mode 2–49
Global Clocking 2–75	in Simple Dual-Port Mode 2–50
Independent Clock Mode 2–44	Regional Clock 2–75
Input/Output Clock Mode	External I/O Timing Parameters 4–34
2–46	Regional Clock Bus 2–79
Simple Dual-Port Mode 2–48	Regional Clock Network 2–75
True Dual-Port Mode 2–47	Spread-Spectrum Clocking 2–98
Maximum Input & Output Clock Rates 4–76	Configuration 3–5
Maximum Input Clock Rate	32-Bit IDCODE 3–3
for CLK	and Testing 3–1
(0, 2, 9, 11) Pins in	Data Sources for Configuration 3–7
Flip-Chip	Local Update Mode 3–12
	Local Update Transition Diagram 3–12
Packages 4–77	Operating Modes 3–5
Wire-Bond	Partial Reconfiguration 3–7
Packages 4–79	Remote Update 3–8
(1, 3, 8, 10) Pins in	Remote Update Transition Diagram 3–11
Flip-Chip	Schemes 3–7
Packages 4–78	SignalTap II Embedded Logic Analyzer 3–5 Stratix FPGAs with JRunner 3–7
Wire-Bond	Control Signals 2–104
Packages 4-80	O
(74) & CLK(1512) Pins in	D
Flip-Chip	U
	DC Switching
Packages 4–76	Absolute Maximum Ratings 4–1
Wire-Bond	Bus Hold Parameters 4–16
Packages 4–78	Capacitance 4–17
Maximum Output Clock Rate	DC & Switching Characteristics 4–1
for PLL	External Timing Parameters 4–33
(1, 2, 3, 4) Pins in	Operating Conditions 4–1 Performance 4–20
Flip-Chip	Power Consumption 4–17
Packages 4–83	Recommended Operating Conditions 4–1
Wire-Bond	DDR
	Double-Data Rate I/O Pins 2–111
Packages 4–85	Device Features
(5, 6, 11, 12) Pins in	EP1S10, EP1S20, EP1S25, EP1S30, 1–3
Flip-Chip	EP1S40, EP1S60, EP1S80, 1–3

Index-2 Altera Corporation

Differential HSTL Specifications 4–15 DSP	Parameters 4–39 Row Pin
Block Diagram	Fast Regional Clock External I/O Timing
Configuration	Parameters 4–40
for 18 x 18-Bit 2–55	Global Clock External I/O Timing
for 9 x 9-Bit 2–56	Parameters 4–41
Block Interconnect Interface 2–71	Regional Clock External I/O Timing
Block Interface 2–70	Parameters 4–41
Block Signal Sources & Destinations 2–73	EP1S25 Devices
Blocks	Column Pin
Arranged in Columns 2–53	Fast Regional Clock External I/O Timing
in Stratix Devices 2–54	Parameters 4–42
Input Register Modes 2-60	Global Clock External I/O Timing
Input Registers 2–58	Parameters 4–43
Multiplier	Regional Clock External I/O Timing
2–60	Parameters 4–42
Block 2–57	Row Pin
Signed Representation 2-60	Fast Regional Clock External I/O Timing
Sub-Block 2–57	Parameters 4–43
Sub-Blocks Using Input Shift Register	Global Clock External I/O Timing
Connections 2–59	Parameters 4–44
Pipeline/Post Multiply Register 2–61	Regional Clock External I/O Timing
	Parameters 4–44
E	EP1S30 Devices
<b>L</b>	Column Pin
EP1S10 Devices	Fast Regional Clock External I/O Timing
Column Pin	Parameters 4–45
Fast Regional Clock External I/O Timing	Global Clock External I/O Timing
Parameters 4–36	Parameters 4–45
Global Clock External I/O Timing Parameters 4–37	Regional Clock External I/O Timing Parameters 4–45
Regional Clock External I/O Timing	Row Pin
Parameters 4–36	Fast Regional Clock External I/O Timing
Row Pin	Parameters 4–46
Fast Regional Clock External I/O Timing	Global Clock External I/O Timing
Parameters 4–37	Parameters 4–47
Global Clock External I/O Timing	Regional Clock External I/O Timing
Parameters 4–38	Parameters 4–47
Regional Clock External I/O Timing	EP1S40 Devices
Parameters 4–38	Column Pin
EP1S20 Devices	Fast Regional Clock External I/O Timing
Column Pin	Parameters 4–48
Fast Regional Clock External I/O Timing	Global Clock External I/O Timing
Parameters 4–39	Parameters 4–49
Global Clock External I/O Timing	Regional Clock External I/O Timing
Parameters 4–40	Parameters 4–48
Regional Clock External I/O Timing	Row Pin

Altera Corporation Index-3

Mode 2–36	Port I/O Standards 2–102
Row & Column Interface Unit	I/O Standards Supported for Enhanced PLL
Signals 2–43	Pins 2–94
Parity Bit Support 2–24	Lock Detect & Programmable Gated
Shift Register	Locked 2–98
Memory Configuration 2–26	PLL Locations 2–84
Support 2–25	Programmable Bandwidth 2–91
Simple Dual-Port & Single-Port Memory	Programmable Delay Chain 2-111
Configurations 2–23	Programmable Duty Cycle 2–98
Stratix IOE in DDR Input I/O	Reconfiguration 2–90
Configuration 2–112	
Stratix IOE in DDR Output I/O	Т
Configuration 2–114	1
TriMatrix Memory 2–21	Testing
True Dual-Port Memory	Temperature Sensing Diode 3–13
Configuration 2–22	Electrical Characteristics 3–14
	External 3–14
0	Temperature vs. Temperature-Sensing Diode
	Voltage 3–15
Ordering Information 5–1	Timing
Device Pin-Outs 5–1	DSP
Packaging Ordering Information 5–2	Block Internal Timing
Reference & Ordering Information 5–1	Microparameter
Output Registers 2–64	Descriptions 4–23
Output Selection Multiplexer 2–64	Microparameters 4–29
	Dual-Port RAM Timing Microparameter
P	Waveform 4–27
P. 1	External Timing in Stratix Devices 4–33
Packaging	High-Speed I/O Timing 4–87
BGA Package Sizes 1–4	High-Speed Timing Specifications & Terminology 4–87
Device Speed Grades 1–5	Internal Parameters 4–22
FineLine BGA Package Sizes 1–5	IOE Internal Timing Microparameter
PCI-X 1.0 Specifications 4–10 Phase Shifting 2–103	Descriptions 4–22
PLL	LE Internal Timing Microparameters 4–28
Advanced Clear & Enable Control 2–98	Logic Elements Internal Timing Microparam-
Dynamically Programmable Counters & De-	eter Descriptions 4–22
lays in Stratix Device Enhanced	Model 4–19
PLLs 2–91	PLL Timing 4–94
Enhanced	Preliminary & Final 4–19
Fast PLLs 2–81	Stratix Device Timing Model Status 4–19
Fast PLL 2–100	Stratix JTAG
Channel Layout EP1S10, EP1S20 or	Timing Parameters & Values 3–4
EP1S25 Devices 2–138	TriMatrix Memory
Channel Layout EP1S30 to EP1S80	TriMatrix Memory Features 2–21
Devices 2–139	•

Index-6 Altera Corporation