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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1057
Number of Logic Elements/Cells	10570
Total RAM Bits	920448
Number of I/O	426
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s10f780i6



Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction

Revised: *July 2005*
Part number: *S51001-3.2*

Chapter 2. Stratix Architecture

Revised: *July 2005*
Part number: *S51002-3.2*

Chapter 3. Configuration & Testing

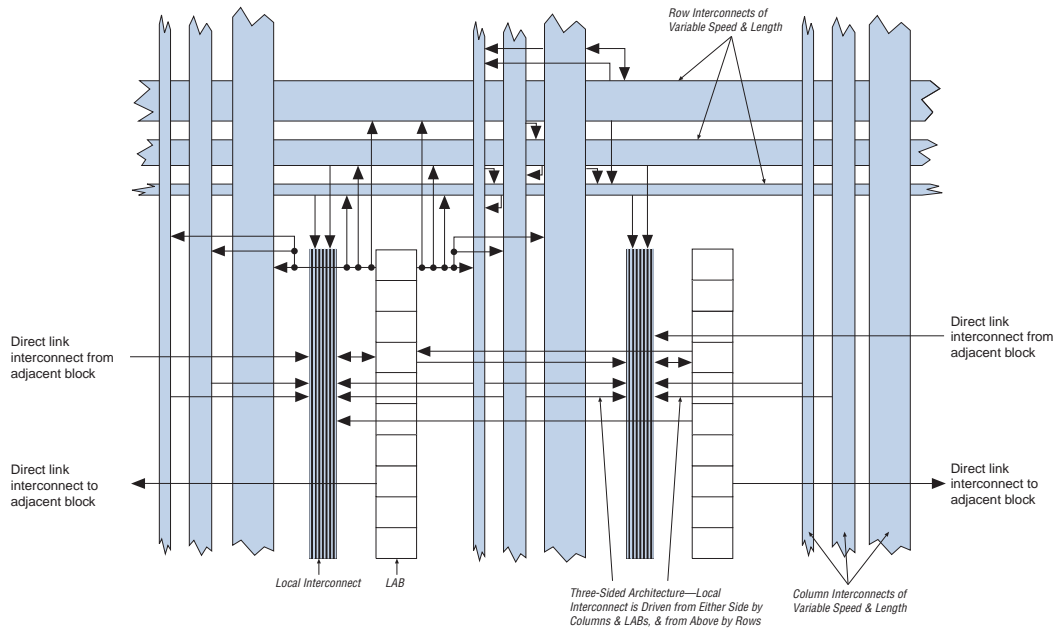
Revised: *July 2005*
Part number: *S51003-1.3*

Chapter 4. DC & Switching Characteristics

Revised: *January 2006*
Part number: *S51004-3.4*

Chapter 5. Reference & Ordering Information

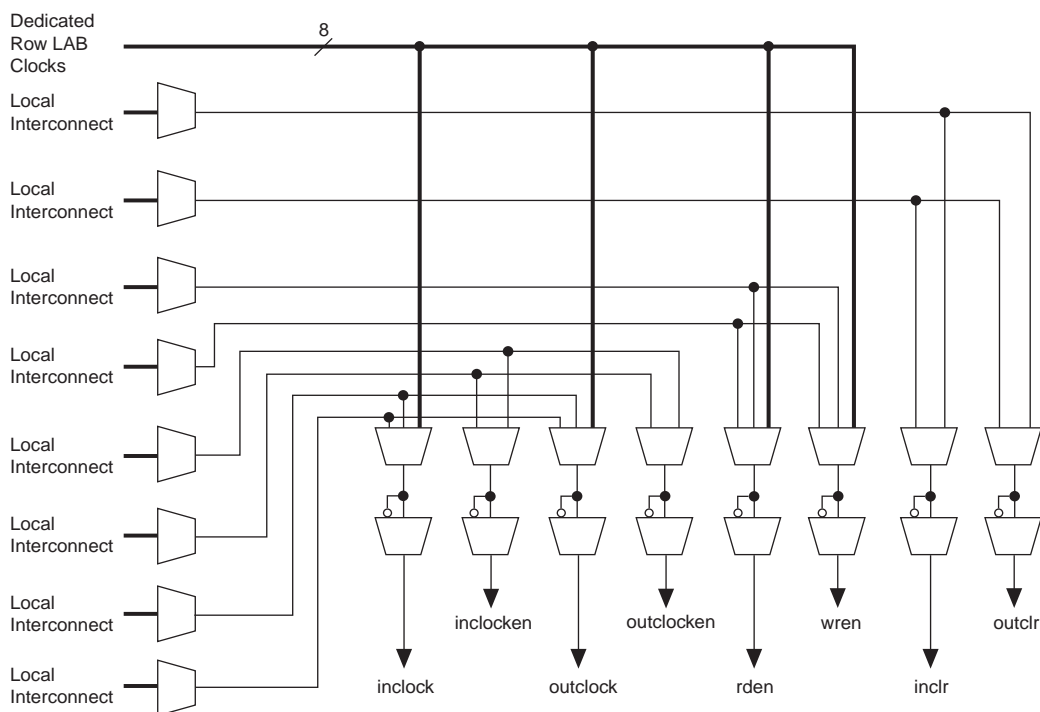
Revised: *September 2004*
Part number: *S51005-2.1*

Figure 2–2. Stratix LAB Structure

LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects.

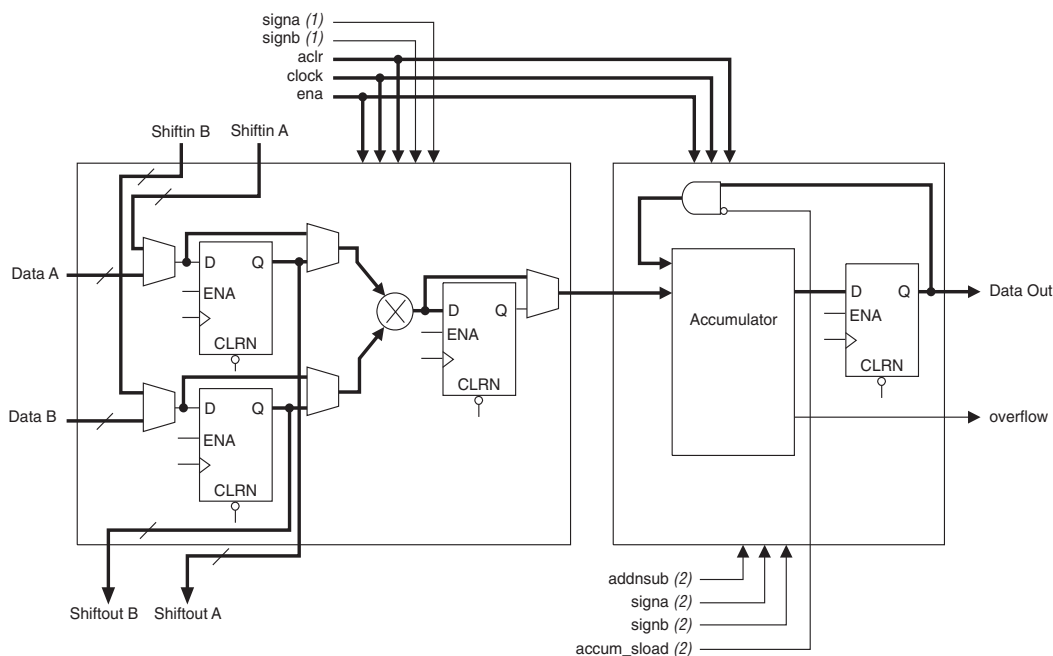
Figure 2–3 shows the direct link connection.

Figure 2–15. M512 RAM Block Control Signals

Multiply-Accumulator Mode

In multiply-accumulator mode (see Figure 2–37), the DSP block drives multiplied results to the adder/subtractor/accumulator block configured as an accumulator. You can implement one or two multiply-accumulators up to 18×18 bits in one DSP block. The first and third multiplier sub-blocks are unused in this mode, because only one multiplier can feed one of two accumulators. The multiply-accumulator output can be up to 52 bits—a maximum of a 36-bit result with 16 bits of accumulation. The `accum_load` and `overflow` signals are only available in this mode. The `addnsb` signal can set the accumulator for decimation and the `overflow` signal indicates underflow condition.

Figure 2–37. Multiply-Accumulate Mode

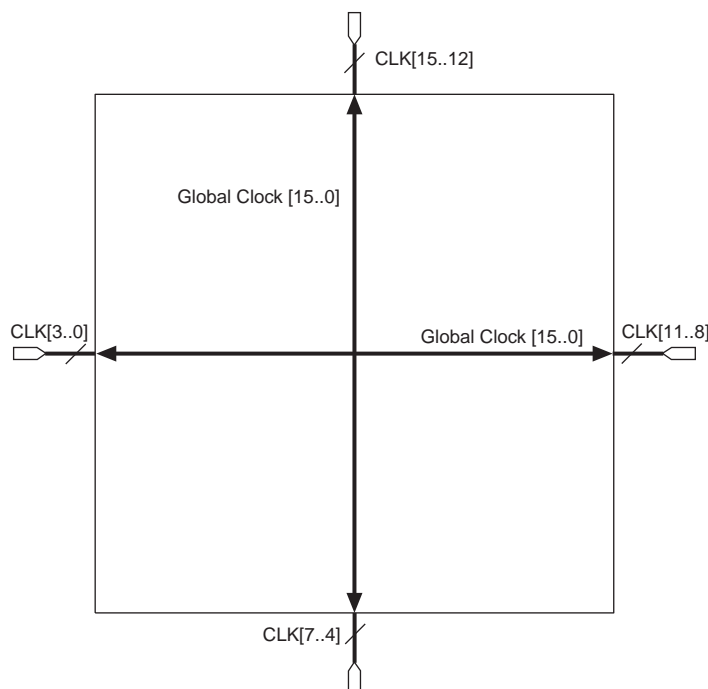


Notes to Figure 2–37:

- (1) These signals are not registered or registered once to match the data path pipeline.
- (2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

Two-Multipliers Adder Mode

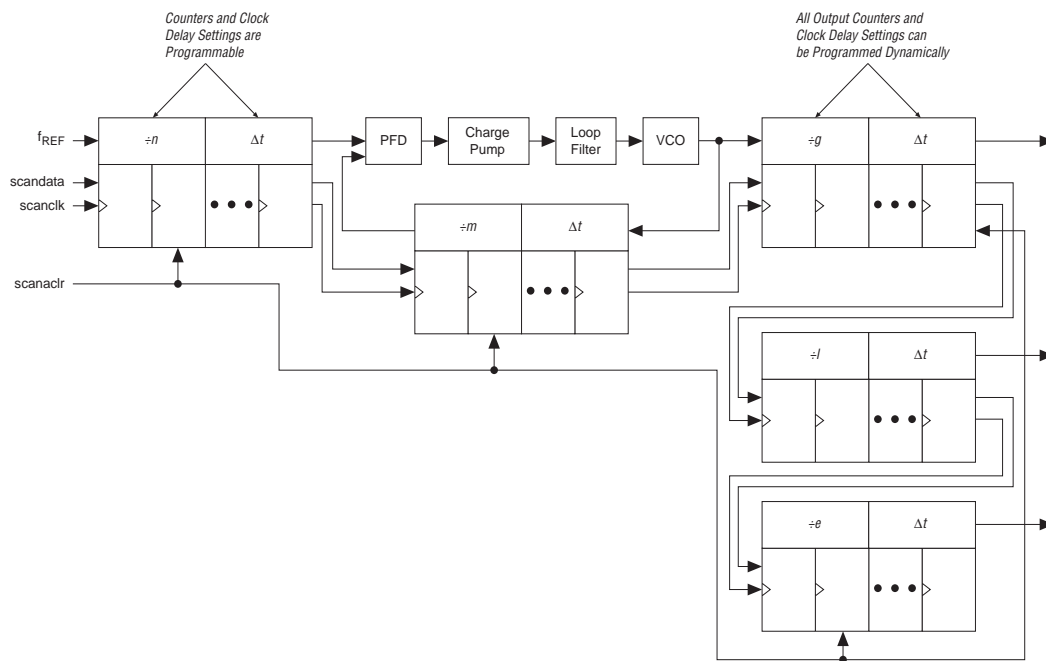
The two-multipliers adder mode uses the adder/subtractor/accumulator block to add or subtract the outputs of the multiplier block, which is useful for applications such as FFT functions and complex FIR filters. A

Figure 2–42. Global Clock *Note (1)***Note to Figure 2–42:**

- (1) The corner fast PLLs can also be driven through the global or regional clock networks. The global or regional clock input to the fast PLL can be driven by an output from another PLL, a pin-driven global or regional clock, or internally-generated global signals.

Regional Clock Network

There are four regional clock networks within each quadrant of the Stratix device that are driven by the same dedicated $\text{CLK}[15..0]$ input pins or from PLL outputs. From a top view of the silicon, $\text{RCLK}[0..3]$ are in the top left quadrant, $\text{RCLK}[8..11]$ are in the top-right quadrant, $\text{RCLK}[4..7]$ are in the bottom-left quadrant, and $\text{RCLK}[12..15]$ are in the bottom-right quadrant. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. RCLK cannot be driven by internal logic. The CLK clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 2–43. See Figures 2–50 and 2–51 for RCLK connections from PLLs and CLK pins.

Figure 2–54. Dynamically Programmable Counters & Delays in Stratix Device Enhanced PLLs

PLL reconfiguration data is shifted into serial registers from the logic array or external devices. The PLL input shift data uses a reference input shift clock. Once the last bit of the serial chain is clocked in, the register chain is synchronously loaded into the PLL configuration bits. The shift circuitry also provides an asynchronous clear for the serial registers.



For more information on PLL reconfiguration, see *AN 282: Implementing PLL Reconfiguration in Stratix & Stratix GX Devices*.

Programmable Bandwidth

You have advanced control of the PLL bandwidth using the programmable control of the PLL loop characteristics, including loop filter and charge pump. The PLL's bandwidth is a measure of its ability to track the input clock and jitter. A high-bandwidth PLL can quickly lock onto a reference clock and react to any changes in the clock. It also will allow a wide band of input jitter spectrum to pass to the output. A low-bandwidth PLL will take longer to lock, but it will attenuate all high-frequency jitter components. The Quartus II software can adjust PLL characteristics to achieve the desired bandwidth. The programmable

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each pair of output pins (four pins total) has dedicated VCC and GND pins to reduce the output clock's overall jitter by providing improved isolation from switching I/O pins.

For PLLs 5 and 6, each pin of a single-ended output pair can either be in phase or 180° out of phase. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, 3.3-V PCML, HyperTransport technology, differential HSTL, and differential SSTL. Table 2–20 shows which I/O standards the enhanced PLL clock pins support. When in single-ended or differential mode, the two outputs operate off the same power supply. Both outputs use the same standards in single-ended mode to maintain performance. You can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

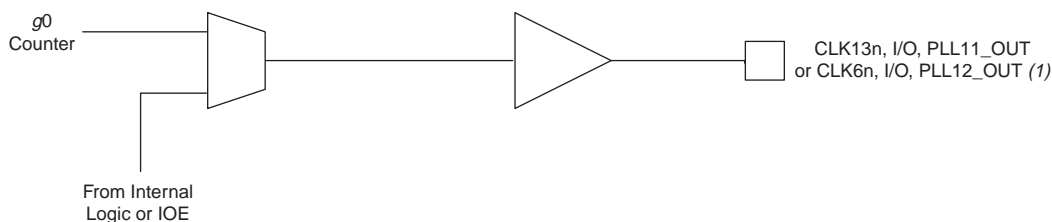
Table 2–20. I/O Standards Supported for Enhanced PLL Pins (Part 1 of 2)

I/O Standard	Input			Output
	INCLK	FBIN	PLENABLE	EXTCLK
LVTTTL	✓	✓	✓	✓
LVC MOS	✓	✓	✓	✓
2.5 V	✓	✓		✓
1.8 V	✓	✓		✓
1.5 V	✓	✓		✓
3.3-V PCI	✓	✓		✓
3.3-V PCI-X 1.0	✓	✓		✓
LVPECL	✓	✓		✓
3.3-V PCML	✓	✓		✓
LVDS	✓	✓		✓
HyperTransport technology	✓	✓		✓
Differential HSTL	✓			✓
Differential SSTL				✓
3.3-V GTL	✓	✓		✓
3.3-V GTL+	✓	✓		✓
1.5-V HSTL Class I	✓	✓		✓

Table 2–20. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2)

I/O Standard	Input			Output
	INCLK	FBIN	PLENABLE	EXTCLK
1.5-V HSTL Class II	✓	✓		✓
1.8-V HSTL Class I	✓	✓		✓
1.8-V HSTL Class II	✓	✓		✓
SSTL-18 Class I	✓	✓		✓
SSTL-18 Class II	✓	✓		✓
SSTL-2 Class I	✓	✓		✓
SSTL-2 Class II	✓	✓		✓
SSTL-3 Class I	✓	✓		✓
SSTL-3 Class II	✓	✓		✓
AGP (1× and 2×)	✓	✓		✓
CTT	✓	✓		✓

Enhanced PLLs 11 and 12 support one single-ended output each (see [Figure 2–56](#)). These outputs do not have their own VCC and GND signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

Figure 2–56. External Clock Outputs for Enhanced PLLs 11 & 12

Note to Figure 2–56:

(1) For PLL 11, this pin is CLK13n; for PLL 12 this pin is CLK7n.

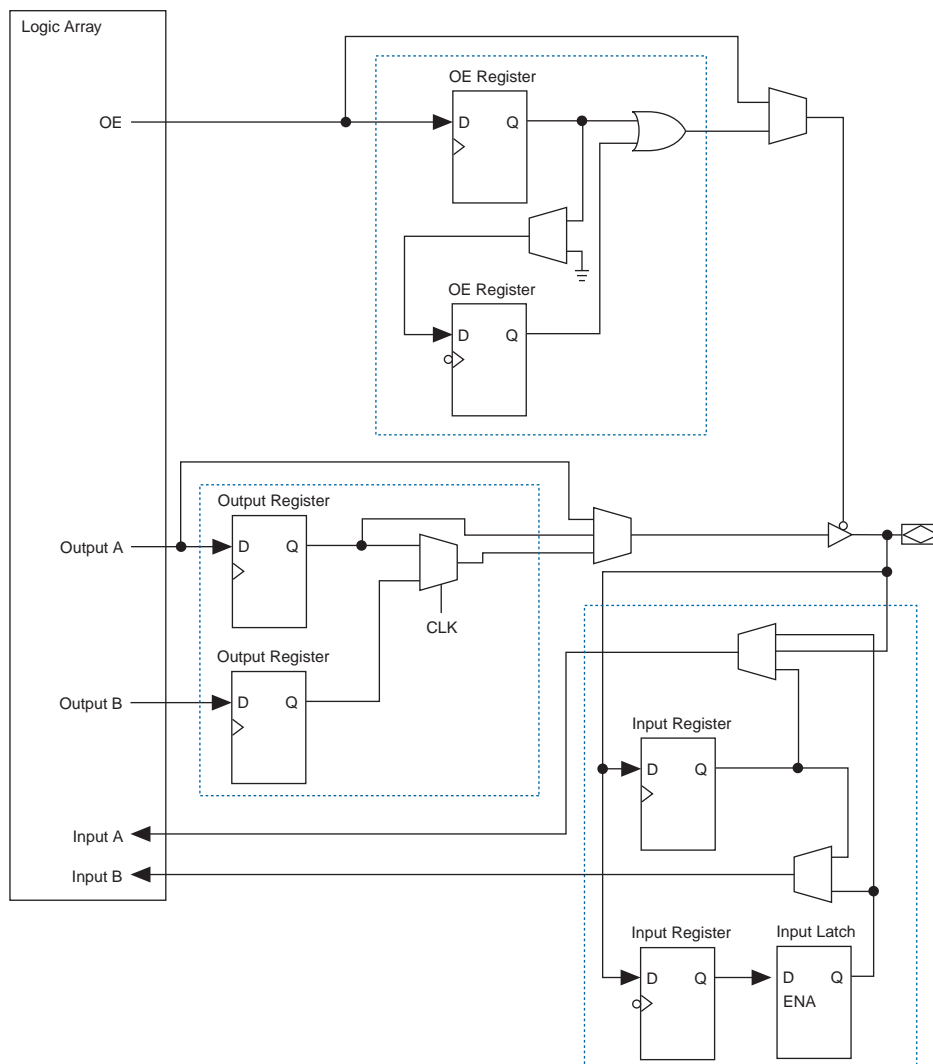
Stratix devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

External Clock Inputs

Each fast PLL supports single-ended or differential inputs for source synchronous transmitters or for general-purpose use. Source-synchronous receivers support differential clock inputs. The fast PLL inputs are fed by CLK [0 . . 3], CLK [8 . . 11], and FPLL [7 . . 10] CLK pins, as shown in [Figure 2–50 on page 2–85](#).

[Table 2–22](#) shows the I/O standards supported by fast PLL input pins.

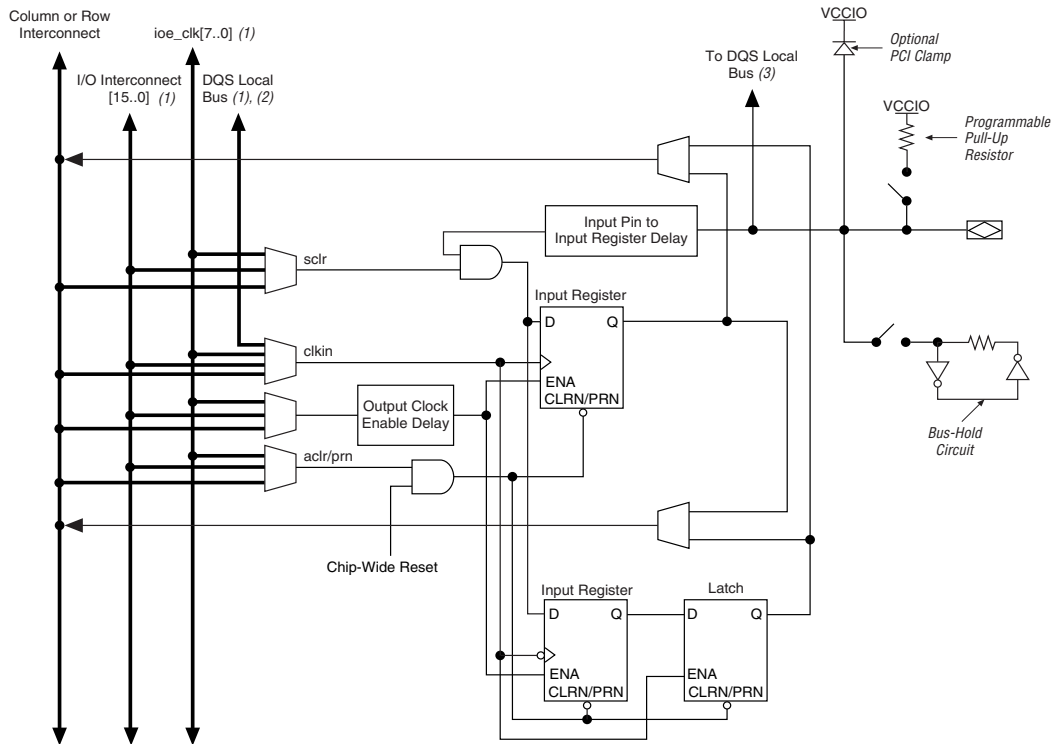
Table 2–22. Fast PLL Port I/O Standards (Part 1 of 2)		
I/O Standard	Input	
	INCLK	PLENABLE
LVTTTL	✓	✓
LVC MOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X 1.0		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	
Differential SSTL		
3.3-V GTL		
3.3-V GTL+	✓	
1.5-V HSTL Class I	✓	
1.5-V HSTL Class II		
1.8-V HSTL Class I	✓	
1.8-V HSTL Class II		
SSTL-18 Class I	✓	
SSTL-18 Class II		
SSTL-2 Class I	✓	

Figure 2–59. Stratix IOE Structure

The IOEs are located in I/O blocks around the periphery of the Stratix device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects.

Figure 2–60 shows how a row I/O block connects to the logic array.

Figure 2–61 shows how a column I/O block connects to the logic array.

Figure 2–65. Stratix IOE in DDR Input I/O Configuration *Note (1)***Notes to Figure 2–65:**

- (1) All input signals to the IOE can be inverted at the IOE.
- (2) This signal connection is only allowed on dedicated DQ function pins.
- (3) This signal is for dedicated DQS function pins only.

Table 2–32 shows I/O standard support for each I/O bank.

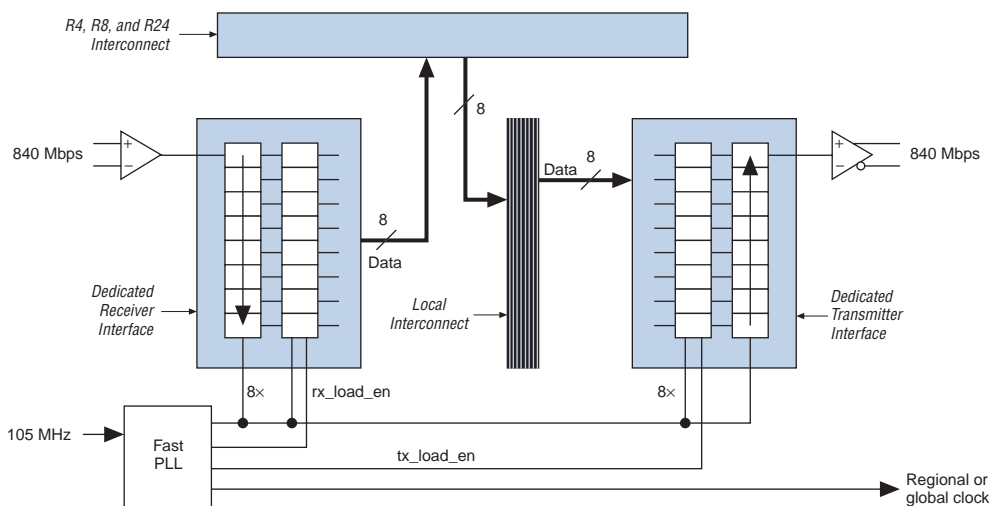
Table 2–32. I/O Support by Bank (Part 1 of 2)			
I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
LVTTTL	✓	✓	✓
LVC MOS	✓	✓	✓
2.5 V	✓	✓	✓
1.8 V	✓	✓	✓
1.5 V	✓	✓	✓
3.3-V PCI	✓		✓
3.3-V PCI-X 1.0	✓		✓
LVPECL		✓	✓
3.3-V PCML		✓	✓
LVDS		✓	✓
HyperTransport technology		✓	✓
Differential HSTL (clock inputs)	✓	✓	
Differential HSTL (clock outputs)			✓
Differential SSTL (clock outputs)			✓
3.3-V GTL	✓		✓
3.3-V GTL+	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓
1.5-V HSTL Class II	✓		✓
1.8-V HSTL Class I	✓	✓	✓
1.8-V HSTL Class II	✓		✓
SSTL-18 Class I	✓	✓	✓
SSTL-18 Class II	✓		✓
SSTL-2 Class I	✓	✓	✓
SSTL-2 Class II	✓	✓	✓
SSTL-3 Class I	✓	✓	✓

- RapidIO
- HyperTransport

Dedicated Circuitry

Stratix devices support source-synchronous interfacing with LVDS, LVPECL, 3.3-V PCML, or HyperTransport signaling at up to 840 Mbps. Stratix devices can transmit or receive serial channels along with a low-speed or high-speed clock. The receiving device PLL multiplies the clock by a integer factor W ($W = 1$ through 32). For example, a HyperTransport application where the data rate is 800 Mbps and the clock rate is 400 MHz would require that W be set to 2. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 7, 8, or 10 and does not have to equal the PLL clock-multiplication W value. For a J factor of 1, the Stratix device bypasses the SERDES block. For a J factor of 2, the Stratix device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. See [Figure 2-73](#).

Figure 2-73. High-Speed Differential I/O Receiver / Transmitter Interface Example



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed differential I/O clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array.

Table 4–36. Stratix Performance (Part 2 of 2) Notes (1), (2)

Applications		Resources Used			Performance				
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Units
TriMatrix memory M-RAM block	True dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	175.74	MHz
	Single port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Single port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
DSP block	9 × 9-bit multiplier (3)	0	0	1	335.0	293.94	255.68	217.24	MHz
	18 × 18-bit multiplier (4)	0	0	1	278.78	237.41	206.52	175.50	MHz
	36 × 36-bit multiplier (4)	0	0	1	148.25	134.71	117.16	99.59	MHz
	36 × 36-bit multiplier (5)	0	0	1	278.78	237.41	206.52	175.5	MHz
	18-bit, 4-tap FIR filter	0	0	1	278.78	237.41	206.52	175.50	MHz
Larger Designs	8-bit, 16-tap parallel FIR filter	58	0	4	141.26	133.49	114.88	100.28	MHz
	8-bit, 1,024-point FFT function	870	5	1	261.09	235.51	205.21	175.22	MHz

Notes to Table 4–36:

- (1) These design performance numbers were obtained using the Quartus II software.
- (2) Numbers not listed will be included in a future version of the data sheet.
- (3) This application uses registered inputs and outputs.
- (4) This application uses registered multiplier input and output stages within the DSP block.
- (5) This application uses registered multiplier input, pipeline, and output stages within the DSP block.

Table 4–49. M4K Block Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{M4KRC}		3,807		4,320		4,967		5,844	ps
t_{M4KWC}		2,556		2,840		3,265		3,842	ps
$t_{M4KWRESU}$	131		149		171		202		ps
$t_{M4KWEREH}$	34		38		43		51		ps
$t_{M4KCLKENSU}$	193		215		247		290		ps
$t_{M4KCLKENH}$	–63		–70		–81		–95		ps
$t_{M4KBESU}$	131		149		171		202		ps
t_{M4KBEH}	34		38		43		51		ps
$t_{M4KDATAASU}$	131		149		171		202		ps
$t_{M4KDATAAH}$	34		38		43		51		ps
$t_{M4KADDRASU}$	131		149		171		202		ps
$t_{M4KADDRAH}$	34		38		43		51		ps
$t_{M4KDATABSU}$	131		149		171		202		ps
$t_{M4KDATA BH}$	34		38		43		51		ps
$t_{M4KADDRBSU}$	131		149		171		202		ps
$t_{M4KADDRBH}$	34		38		43		51		ps
$t_{M4KDATA CO1}$		571		635		729		858	ps
$t_{M4KDATA CO2}$		3,984		4,507		5,182		6,097	ps
$t_{M4KCLKHL}$	1,000		1,111		1,190		1,400		ps
t_{M4KCLR}	170		189		217		255		ps

Table 4–50. M-RAM Block Internal Timing Microparameters (Part 1 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{MRAMRC}		4,364		4,838		5,562		6,544	ps
t_{MRAMWC}		3,654		4,127		4,746		5,583	ps
$t_{MRAMWRESU}$	25		25		28		33		ps
$t_{MRAMWEREH}$	18		20		23		27		ps
$t_{MRAMCLKENSU}$	99		111		127		150		ps
$t_{MRAMCLKENH}$	–48		–53		–61		–72		ps

Table 4-52 shows the external I/O timing parameters when using fast regional clock networks.

Table 4-52. Stratix Fast Regional Clock External I/O Timing Parameters <i>Notes (1), (2)</i>	
Symbol	Parameter
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with fast regional clock fed by FCLK pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with fast regional clock fed by FCLK pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with fast regional clock fed by FCLK pin
t_{xZ}	Synchronous IOE output enable register to output pin disable delay using fast regional clock fed by FCLK pin
t_{ZX}	Synchronous IOE output enable register to output pin enable delay using fast regional clock fed by FCLK pin

Notes to Table 4-52:

- (1) These timing parameters are sample-tested only.
- (2) These timing parameters are for column and row IOE pins. You should use the Quartus II software to verify the external timing for any pin.

Table 4-53 shows the external I/O timing parameters when using regional clock networks.

Table 4-53. Stratix Regional Clock External I/O Timing Parameters (Part 1 of 2) <i>Notes (1), (2)</i>	
Symbol	Parameter
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with regional clock fed by CLK pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with regional clock fed by CLK pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with regional clock fed by CLK pin
t_{INSUPLL}	Setup time for input or bidirectional pin using IOE input register with regional clock fed by Enhanced PLL with default phase setting
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with regional clock fed by Enhanced PLL with default phase setting
t_{OUTCOPLL}	Clock-to-output delay output or bidirectional pin using IOE output register with regional clock Enhanced PLL with default phase setting

Definition of I/O Skew

I/O skew is defined as the absolute value of the worst-case difference in clock-to-out times (t_{CO}) between any two output registers fed by a common clock source.

I/O bank skew is made up of the following components:

- Clock network skews: This is the difference between the arrival times of the clock at the clock input port of the two IOE registers.
- Package skews: This is the package trace length differences between (I/O pad A to I/O pin A) and (I/O pad B to I/O pin B).

Figure 4–5 shows an example of two IOE registers located in the same bank, being fed by a common clock source. The clock can come from an input pin or from a PLL output.

Figure 4–5. I/O Skew within an I/O Bank

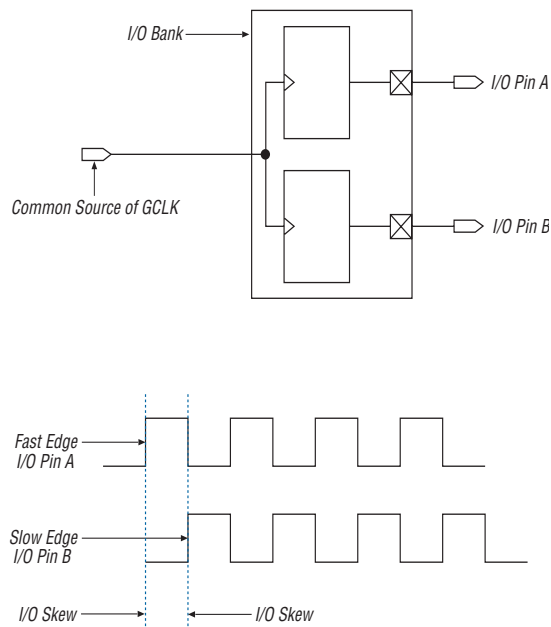


Table 4–119. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
SSTL-18 Class I	350	300	300	MHz
SSTL-18 Class II	350	300	300	MHz
1.5-V HSTL Class I	350	300	300	MHz
1.8-V HSTL Class I	350	300	300	MHz
CTT	250	200	200	MHz
Differential 1.5-V HSTL C1	350	300	300	MHz
LVPECL (1)	645	622	622	MHz
PCML (1)	275	275	275	MHz
LVDS (1)	645	622	622	MHz
HyperTransport technology (1)	500	450	450	MHz

Note to Tables 4–114 through 4–119:

(1) These parameters are only available on row I/O pins.

Tables 4–120 through 4–123 show the maximum output clock rate for column and row pins in Stratix devices.

Table 4–120. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Flip-Chip Packages (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	350	300	250	250	MHz
2.5 V	350	300	300	300	MHz
1.8 V	250	250	250	250	MHz
1.5 V	225	200	200	200	MHz
LVC MOS	350	300	250	250	MHz
GTL	200	167	125	125	MHz
GTL+	200	167	125	125	MHz
SSTL-3 Class I	200	167	167	133	MHz
SSTL-3 Class II	200	167	167	133	MHz
SSTL-2 Class I (3)	200	200	167	167	MHz
SSTL-2 Class I (4)	200	200	167	167	MHz
SSTL-2 Class I (5)	150	134	134	134	MHz

Table 4–123. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVDS (2)	400	311	311	MHz
HyperTransport technology (2)	420	400	400	MHz

Notes to Tables 4–120 through 4–123:

- (1) Differential SSTL-2 outputs are only available on column clock pins.
- (2) These parameters are only available on row I/O pins.
- (3) SSTL-2 in maximum drive strength condition. See Table 4–101 on page 4–62 for more information on exact loading conditions for each I/O standard.
- (4) SSTL-2 in minimum drive strength with ≤ 10 pF output load condition.
- (5) SSTL-2 in minimum drive strength with > 10 pF output load condition.
- (6) Differential SSTL-2 outputs are only supported on column clock pins.

Differential HSTL Specifications 4-15

DSP

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EP1S10 Devices

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Parameters 4-38

EP1S20 Devices

Column Pin

Fast Regional Clock External I/O Timing
Parameters 4-39

Global Clock External I/O Timing
Parameters 4-40

Regional Clock External I/O Timing

Parameters 4-39

Row Pin

Fast Regional Clock External I/O Timing
Parameters 4-40

Global Clock External I/O Timing
Parameters 4-41

Regional Clock External I/O Timing
Parameters 4-41

EP1S25 Devices

Column Pin

Fast Regional Clock External I/O Timing
Parameters 4-42

Global Clock External I/O Timing
Parameters 4-43

Regional Clock External I/O Timing
Parameters 4-42

Row Pin

Fast Regional Clock External I/O Timing
Parameters 4-43

Global Clock External I/O Timing
Parameters 4-44

Regional Clock External I/O Timing
Parameters 4-44

EP1S30 Devices

Column Pin

Fast Regional Clock External I/O Timing
Parameters 4-45

Global Clock External I/O Timing
Parameters 4-45

Regional Clock External I/O Timing
Parameters 4-45

Row Pin

Fast Regional Clock External I/O Timing
Parameters 4-46

Global Clock External I/O Timing
Parameters 4-47

Regional Clock External I/O Timing
Parameters 4-47

EP1S40 Devices

Column Pin

Fast Regional Clock External I/O Timing
Parameters 4-48

Global Clock External I/O Timing
Parameters 4-49

Regional Clock External I/O Timing
Parameters 4-48

Row Pin