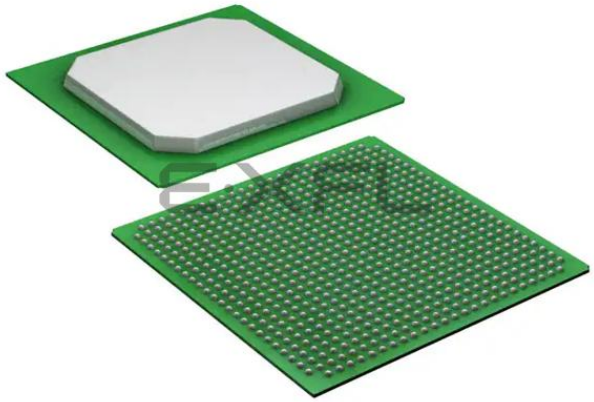

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

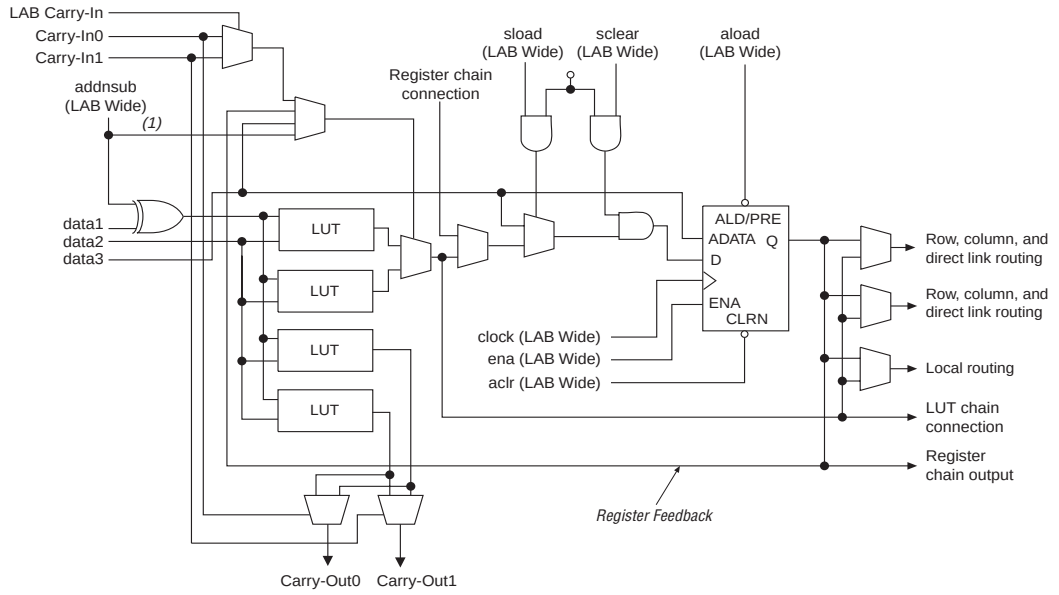
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1846
Number of Logic Elements/Cells	18460
Total RAM Bits	1669248
Number of I/O	426
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s20b672c6

Chapter	Date/Version	Changes Made
4		• Updated Table 4–123 on page 4–85 through Table 4–126 on page 4–92. • Updated Note 3 in Table 4–123 on page 4–85. • Table 4–125 on page 4–88: moved to correct order in chapter, and updated table. • Updated Table 4–126 on page 4–92. • Updated Table 4–127 on page 4–94. • Updated Table 4–128 on page 4–95.
	April 2004, v3.0	• Table 4–129 on page 4–96: updated table and added Note 10. • Updated Table 4–131 and Table 4–132 on page 4–100. • Updated Table 4–110 on page 4–74. • Updated Table 4–123 on page 4–85. • Updated Table 4–124 on page 4–87. through Table 4–126 on page 4–92. • Added Note 10 to Table 4–129 on page 4–96. • Moved Table 4–127 on page 4–94 to correct order in the chapter. • Updated Table 4–131 on page 4–100 through Table 4–132 on page 4–100. • Deleted t_{XZ} and t_{ZX} from Figure 4–4. • Waveform was added to Figure 4–6. • The minimum and maximum duty cycle values in Note 3 of Table 4–8 were moved to a new Table 4–9. • Changes were made to values in SSTL-3 Class I and II rows in Table 4–17. • Note 1 was added to Table 4–34. • Added t_{SU_R} and t_{SU_C} rows in Table 4–38. • Changed Table 4–55 title from “EP1S10 Column Pin Fast Regional Clock External I/O Timing Parameters” to “EP1S10 External I/O Timing on Column Pins Using Fast Regional Clock Networks.” • Changed values in Tables 4–46, 4–48 to 4–51, 4–128, and 4–131. • Added t_{ARESET} row in Tables 4–127 to 4–132. • Deleted -5 Speed Grade column in Tables 4–117 to 4–119 and 4–122 to 4–123. • Fixed differential waveform in Figure 4–1. • Added “Definition of I/O Skew” section. • Added t_{SU} and t_{CO_C} rows and made changes to values in t_{PRE} and t_{CLKHL} rows in Table 4–46. • Values changed in the t_{SU} and t_{H} rows in Table 4–47. • Values changed in the $t_{M4KCLKHL}$ row in Table 4–49. • Values changed in the $t_{MRAMCLKHL}$ row in Table 4–50. • Added Table 4–51 to “Internal Timing Parameters” section. • The timing information is preliminary in Tables 4–55 through 4–96. • Table 4–111 was separated into 3 tables: Tables 4–111 to 4–113.
	November 2003, v2.2	• Updated Tables 4–127 through 4–129.

Figure 2–7. LE in Dynamic Arithmetic Mode



Note to Figure 2–7:
(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Table 2–2 shows the Stratix device's routing scheme.

Table 2–2. Stratix Device Routing Scheme

Source	Destination																
	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R8 Interconnect	R24 Interconnect	C4 Interconnect	C8 Interconnect	C16 Interconnect	LE	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
LUT Chain											✓						
Register Chain											✓						
Local Interconnect											✓	✓	✓	✓	✓	✓	✓
Direct Link Interconnect			✓														
R4 Interconnect			✓		✓		✓	✓		✓							
R8 Interconnect			✓			✓			✓								
R24 Interconnect					✓		✓	✓		✓							
C4 Interconnect			✓		✓			✓									
C8 Interconnect			✓			✓			✓								
C16 Interconnect					✓		✓	✓		✓							
LE	✓	✓	✓	✓	✓	✓		✓	✓								
M512 RAM Block			✓	✓	✓	✓		✓	✓								
M4K RAM Block			✓	✓	✓	✓		✓	✓								
M-RAM Block								✓	✓								
DSP Blocks			✓	✓	✓	✓		✓	✓								
Column IOE				✓				✓	✓	✓							
Row IOE				✓		✓	✓	✓	✓	✓							

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2–7 summarizes the byte selection.

Table 2–7. Byte Enable for M4K Blocks Notes (1), (2)

byteena[3..0]	datain ×18	datain ×36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Notes to Table 2–7:
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

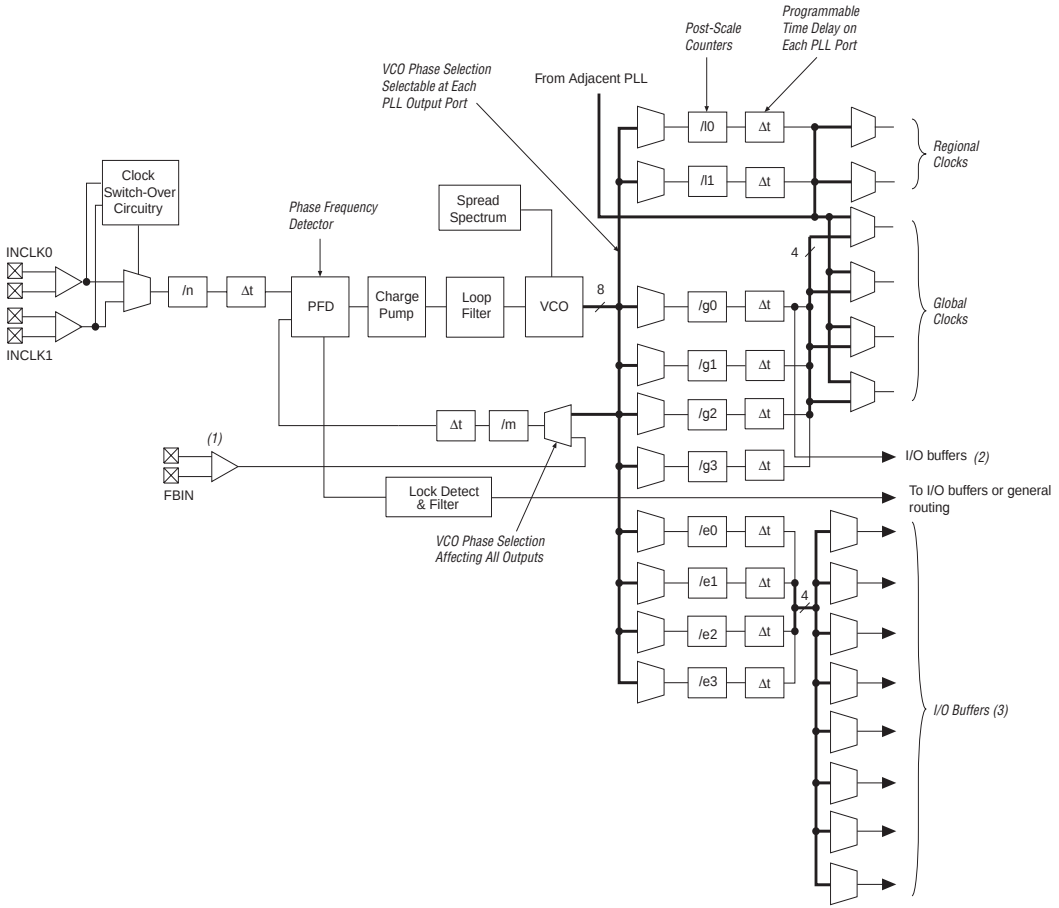
The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The eight `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–17.

The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2–18 shows the M4K RAM block to logic array interface.

Enhanced PLLs

Stratix devices contain up to four enhanced PLLs with advanced clock management features. Figure 2–52 shows a diagram of the enhanced PLL.

Figure 2–52. Stratix Enhanced PLL



Notes to Figure 2–52:

(1) External feedback is available in PLLs 5 and 6.
(2) This single-ended external output is available from the *g*0 counter for PLLs 11 and 12.
(3) These four counters and external outputs are available in PLLs 5 and 6.
(4) This connection is only available on EP1S40 and larger Stratix devices. For example, PLLs 5 and 11 are adjacent and PLLs 6 and 12 are adjacent. The EP1S40 device in the 780-pin FineLine BGA package does not support PLLs 11 and 12.

The variation due to process, voltage, and temperature is about ±15% on the delay settings. PLL reconfiguration can control the clock delay shift elements, but not the VCO phase shift multiplexers, during system operation.

Spread-Spectrum Clocking

Stratix device enhanced PLLs use spread-spectrum technology to reduce electromagnetic interference generation from a system by distributing the energy over a broader frequency range. The enhanced PLL typically provides 0.5% down spread modulation using a triangular profile. The modulation frequency is programmable. Enabling spread-spectrum for a PLL affects all of its outputs.

Lock Detect

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. You may need to gate the lock signal for use as a system control. The lock signal from the locked port can drive the logic array or an output pin.

Whenever the PLL loses lock (for example, `inclk` jitter, clock switchover, PLL reconfiguration, power supply noise, and so on), the PLL must be reset with the `areset` signal to guarantee correct phase relationship between the PLL output clocks. If the phase relationship between the input clock versus output clock, and between different output clocks from the PLL is not important in the design, then the PLL need not be reset.

See the *Stratix FPGA Errata Sheet* for more information on implementing the gated lock signal in a design.

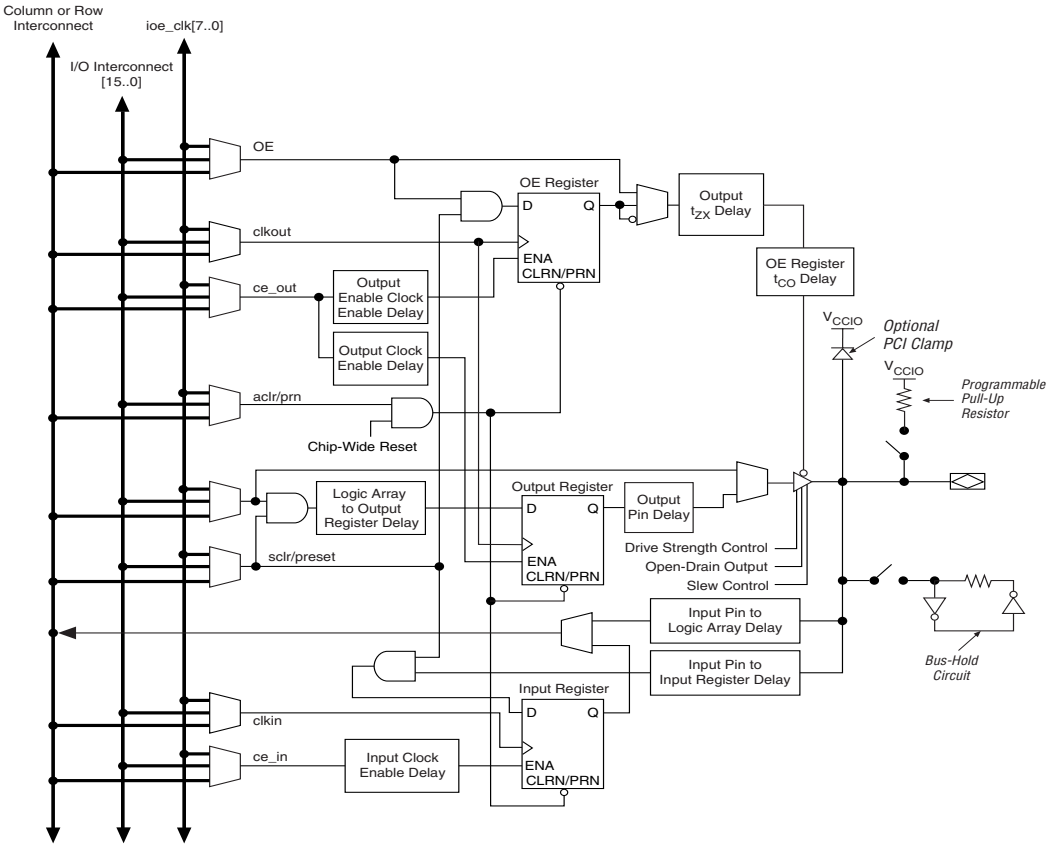
Programmable Duty Cycle

The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

Figure 2–64. Stratix IOE in Bidirectional I/O Configuration Note (1)

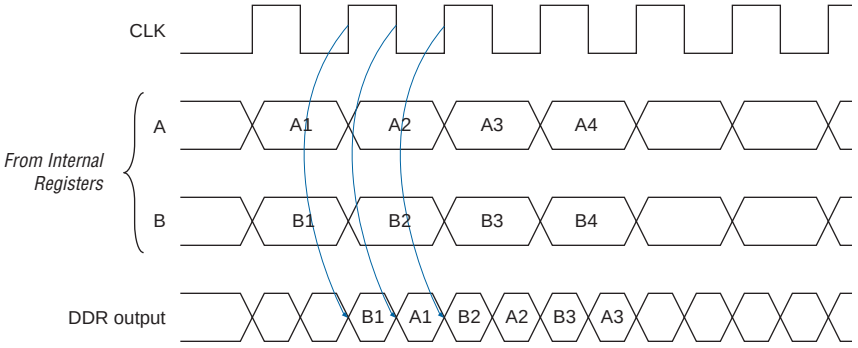


Note to Figure 2–64:
(1) All input signals to the IOE can be inverted at the IOE.

The Stratix device IOE includes programmable delays that can be activated to ensure zero hold times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output

Figure 2–68. Output Timing Diagram in DDR Mode



The Stratix IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

Stratix devices support DDR SDRAM at up to 200 MHz (400-Mbps data rate) through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces up to 200 MHz. Stratix devices also provide preliminary support for reduced latency DRAM II (RLDRAM II) at rates up to 200 MHz through the dedicated phase-shift circuitry.

In addition to the required signals for external memory interfacing, Stratix devices offer the optional clock enable signal. By default the Quartus II software sets the clock enable signal high, which tells the output register to update with new values. The output registers hold their own values if the design sets the clock enable signal low. See Figure 2–64.

To find out more about the DDR SDRAM specification, see the JEDEC web site (**www.jedec.org**). For information on memory controller megafunctions for Stratix devices, see the Altera web site (**www.altera.com**). See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices* for more information on DDR SDRAM interface in Stratix. Also see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices* and *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

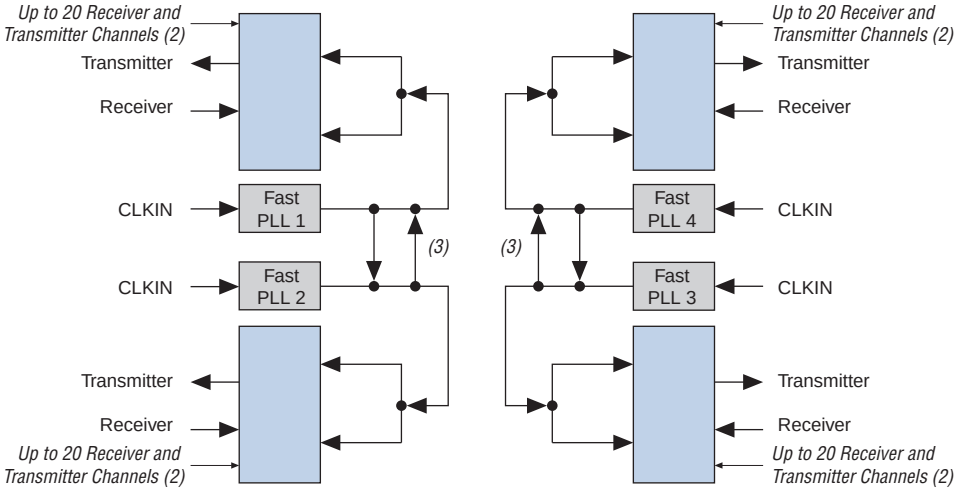
Table 2–37 shows the number of channels that each fast PLL can clock in EP1S10, EP1S20, and EP1S25 devices. Tables 2–38 through Table 2–41 show this information for EP1S30, EP1S40, EP1S60, and EP1S80 devices.

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 1 of 2) Note (1)

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S10	484-pin FineLine BGA	Transmitter (2)	20	840 (4)	5	5	5	5
				840 (3)	10	10	10	10
		Receiver	20	840 (4)	5	5	5	5
				840 (3)	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter (2)	36	624 (4)	9	9	9	9
				624 (3)	18	18	18	18
		Receiver	36	624 (4)	9	9	9	9
				624 (3)	18	18	18	18
	780-pin FineLine BGA	Transmitter (2)	44	840 (4)	11	11	11	11
				840 (3)	22	22	22	22
		Receiver	44	840 (4)	11	11	11	11
				840 (3)	22	22	22	22
EP1S20	484-pin FineLine BGA	Transmitter (2)	24	840 (4)	6	6	6	6
				840 (3)	12	12	12	12
		Receiver	20	840 (4)	5	5	5	5
				840 (3)	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter (2)	48	624 (4)	12	12	12	12
				624 (3)	24	24	24	24
		Receiver	50	624 (4)	13	12	12	13
				624 (3)	25	25	25	25
	780-pin FineLine BGA	Transmitter (2)	66	840 (4)	17	16	16	17
				840 (3)	33	33	33	33
		Receiver	66	840 (4)	17	16	16	17
				840 (3)	33	33	33	33

The Quartus II MegaWizard® Plug-In Manager only allows the implementation of up to 20 receiver or 20 transmitter channels for each fast PLL. These channels operate at up to 840 Mbps. The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–74 shows the fast PLL and channel layout in EP1S10, EP1S20, and EP1S25 devices. Figure 2–75 shows the fast PLL and channel layout in the EP1S30 to EP1S80 devices.

Figure 2–74. Fast PLL & Channel Layout in the EP1S10, EP1S20 or EP1S25 Devices *Note (1)*



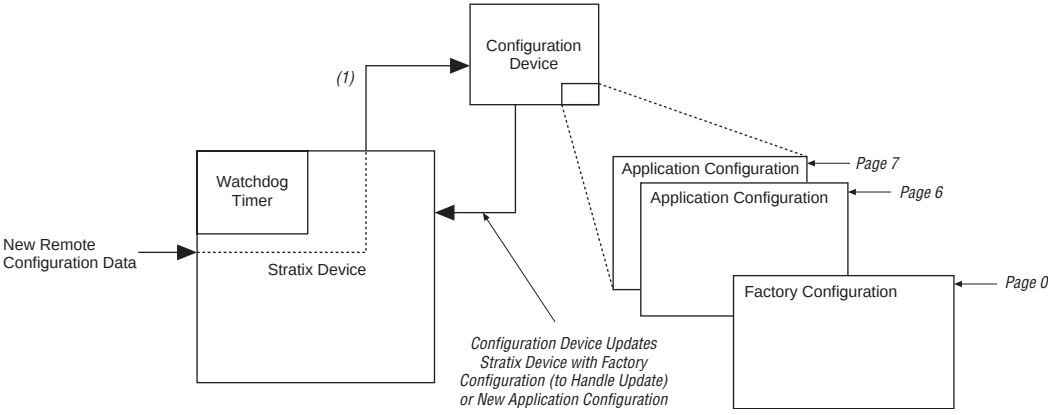
Notes to Figure 2–74:

(1) Wire-bond packages support up to 624 Mbps.

(2) See Table 2–41 for the number of channels each device supports.

(3) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant, those clocked channels support up to 840 Mbps for "high" speed channels and 462 Mbps for "low" speed channels, as labeled in the device pin-outs at **www.altera.com**.

Figure 3–2. Stratix Device Remote Update



Note to Figure 3–2:

(1) When the Stratix device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

Table 4–45. IOE Internal TSU Microparameter by Device Density (Part 2 of 2)

Device	Symbol	-5		-6		-7		-8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
EP1S40	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	376		380		380		380		ps
EP1S60	t_{SU_R}	276		280		280		280		ps
	t_{SU_C}	276		280		280		280		ps
EP1S80	t_{SU_R}	426		430		430		430		ps
	t_{SU_C}	76		80		80		80		ps

Table 4–46. IOE Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_H	68		71		82		96		ps
t_{CO_R}		171		179		206		242	ps
t_{CO_C}		171		179		206		242	ps
$t_{PIN2COMBOUT\_R}$		1,234		1,295		1,490		1,753	ps
$t_{PIN2COMBOUT\_C}$		1,087		1,141		1,312		1,544	ps
$t_{COMBIN2PIN\_R}$		3,894		4,089		4,089		4,089	ps
$t_{COMBIN2PIN\_C}$		4,299		4,494		4,494		4,494	ps
t_{CLR}	276		289		333		392		ps
t_{PRE}	260		273		313		369		ps
t_{CLKHL}	1,000		1,111		1,190		1,400		ps

Table 4–47. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	0		0		0		0		ps
t_H	67		75		86		101		ps
t_{CO}		142		158		181		214	ps
$t_{INREG2PIPE9}$		2,613		2,982		3,429		4,035	ps
$t_{INREG2PIPE18}$		3,390		3,993		4,591		5,402	ps

Table 4–47. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PIPE2OUTREG2ADD}$		2,002		2,203		2,533		2,980	ps
$t_{PIPE2OUTREG4ADD}$		2,899		3,189		3,667		4,314	ps
t_{PD9}		3,709		4,081		4,692		5,520	ps
t_{PD18}		4,795		5,275		6,065		7,135	ps
t_{PD36}		7,495		8,245		9,481		11,154	ps
t_{CLR}	450		500		575		676		ps
t_{CLKHL}	1,350		1,500		1,724		2,029		ps

Table 4–48. M512 Block Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{M512RC}		3,340		3,816		4,387		5,162	ps
t_{M512WC}		3,138		3,590		4,128		4,860	ps
$t_{M512WERESU}$	110		123		141		166		ps
$t_{M512WEREH}$	34		38		43		51		ps
$t_{M512CLKENSU}$	215		215		247		290		ps
$t_{M512CLKENH}$	–70		–70		–81		–95		ps
$t_{M512DATASU}$	110		123		141		166		ps
$t_{M512DATAH}$	34		38		43		51		ps
$t_{M512WADDRSU}$	110		123		141		166		ps
$t_{M512WADDRH}$	34		38		43		51		ps
$t_{M512RADDRSU}$	110		123		141		166		ps
$t_{M512RADDRH}$	34		38		43		51		ps
$t_{M512DATACO1}$		424		472		541		637	ps
$t_{M512DATACO2}$		3,366		3,846		4,421		5,203	ps
$t_{M512CLKHL}$	1,000		1,111		1,190		1,400		ps
$t_{M512CLR}$	170		189		217		255		ps

Table 4–53. Stratix Regional Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)	
Symbol	**Parameter**
t_{XZPLL}	Synchronous IOE output enable register to output pin disable delay using regional clock fed by Enhanced PLL with default phase setting
t_{ZXPLL}	Synchronous IOE output enable register to output pin enable delay using regional clock fed by Enhanced PLL with default phase setting

Notes to Table 4–53:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column and row IOE pins. You should use the Quartus II software to verify the external timing for any pin.

Table 4–54 shows the external I/O timing parameters when using global clock networks.

Table 4–54. Stratix Global Clock External I/O Timing Parameters Notes (1), (2)	
Symbol	**Parameter**
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by `CLK` pin
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock Enhanced PLL with default phase setting
t_{XZPLL}	Synchronous IOE output enable register to output pin disable delay using global clock fed by Enhanced PLL with default phase setting
t_{ZXPLL}	Synchronous IOE output enable register to output pin enable delay using global clock fed by Enhanced PLL with default phase setting

Notes to Table 4–54:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column and row IOE pins. You should use the Quartus II software to verify the external timing for any pin.

Table 4–77. EP1S30 External I/O Timing on Row Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.322		2.467		2.828		3.342		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.731	5.408	2.731	5.843	2.731	6.360	2.731	7.036	ns
t_{XZ}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
t_{ZX}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
$t_{INSUPLL}$	1.291		1.283		1.469		1.832		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.192	2.539	1.192	2.737	1.192	2.786	1.192	2.742	ns
t_{XZPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns
t_{ZXPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns

Table 4–78. EP1S30 External I/O Timing on Row Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.995		2.089		2.398		2.830		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.917	5.735	2.917	6.221	2.917	6.790	2.917	7.548	ns
t_{XZ}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
t_{ZX}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
$t_{INSUPLL}$	1.337		1.312		1.508		1.902		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.164	2.493	1.164	2.708	1.164	2.747	1.164	2.672	ns
t_{XZPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns
t_{ZXPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns

Table 4–89. EP1S60 External I/O Timing on Row Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.775		2.990		3.407		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.867	5.644	2.867	6.057	2.867	6.600	NA	NA	ns
t_{XZ}	2.894	5.698	2.894	6.113	2.894	6.668	NA	NA	ns
t_{ZX}	2.894	5.698	2.894	6.113	2.894	6.668	NA	NA	ns
$t_{INSUPLL}$	1.523		1.577		1.791		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.174	2.507	1.174	2.643	1.174	2.664	NA	NA	ns
t_{XZPLL}	1.201	2.561	1.201	2.699	1.201	2.732	NA	NA	ns
t_{ZXPLL}	1.201	2.561	1.201	2.699	1.201	2.732	NA	NA	ns

Table 4–90. EP1S60 External I/O Timing on Row Pins Using Global Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.232		2.393		2.721		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.182	6.187	3.182	6.654	3.182	7.286	NA	NA	ns
t_{XZ}	3.209	6.241	3.209	6.710	3.209	7.354	NA	NA	ns
t_{ZX}	3.209	6.241	3.209	6.710	3.209	7.354	NA	NA	ns
$t_{INSUPLL}$	1.651		1.612		1.833		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.154	2.469	1.154	2.608	1.154	2.622	NA	NA	ns
t_{XZPLL}	1.181	2.523	1.181	2.664	1.181	2.690	NA	NA	ns
t_{ZXPLL}	1.181	2.523	1.181	2.664	1.181	2.690	NA	NA	ns

Note to Tables 4–85 to 4–90:

(1) Only EP1S25, EP1S30, and EP1S40 devices have the -8 speed grade.

Skew on Input Pins

Table 4–99 shows the package skews that were considered to get the worst case I/O skew value. You can use these values, for example, when calculating the timing budget on the input (read) side of a memory interface.

Table 4–99. Package Skew on Input Pins

Package Parameter	Worst-Case Skew (ps)
Pins in the same I/O bank	50
Pins in top/bottom (vertical I/O) banks	50
Pins in left/right side (horizontal I/O) banks	50
Pins across the entire device	100

PLL Counter & Clock Network Skews

Table 4–100 shows the clock skews between different clock outputs from the Stratix device PLL.

Table 4–100. PLL Counter & Clock Network Skews

Parameter	Worst-Case Skew (ps)
Clock skew between two external clock outputs driven by the same counter	100
Clock skew between two external clock outputs driven by the different counters with the same settings	150
Dual-purpose PLL dedicated clock output used as I/O pin vs. regular I/O pin	270 *(1)*
Clock skew between any two outputs of the PLL that drive global clock networks	150

Note to Table 4–100:

(1) The Quartus II software models 270 ps of delay on the PLL dedicated clock output (`PLL6_OUT[3..0]p/n` and `PLL5_OUT[3..0]p/n`) pins both when used as clocks and when used as I/O pins.

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination and loading for each I/O standard. The timing information is specified from the input clock pin up to the output pin of

Table 4–123. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVDS *(2)*	400	311	311	MHz
HyperTransport technology *(2)*	420	400	400	MHz

Notes to Tables 4–120 through 4–123:

(1) Differential SSTL-2 outputs are only available on column clock pins.
(2) These parameters are only available on row I/O pins.
(3) SSTL-2 in maximum drive strength condition. See Table 4–101 on page 4–62 for more information on exact loading conditions for each I/O standard.
(4) SSTL-2 in minimum drive strength with ≤10pF output load condition.
(5) SSTL-2 in minimum drive strength with > 10pF output load condition.
(6) Differential SSTL-2 outputs are only supported on column clock pins.

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 3 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SW	PCML (*J* = 4, 7, 8, 10)	750			750			800			800			ps
	PCML (*J* = 2)	900			900			1,200			1,200			ps
	PCML (*J* = 1)	1,500			1,500			1,700			1,700			ps
	LVDS and LVPECL (*J* = 1)	500			500			550			550			ps
	LVDS, LVPECL, HyperTransport technology (*J* = 2 through 10)	440			440			500			500			ps
Input jitter tolerance (peak-to-peak)	All			250			250			250			250	ps
Output jitter (peak-to-peak)	All			160			160			200			200	ps
Output t_{RISE}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	120	170	200	120	170	200	ps
	LVPECL	90	130	150	90	130	150	100	135	150	100	135	150	ps
	PCML	80	110	135	80	110	135	80	110	135	80	110	135	ps
Output t_{FALL}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	110	170	200	110	170	200	ps
	LVPECL	90	130	160	90	130	160	100	135	160	100	135	160	ps
	PCML	105	140	175	105	140	175	110	145	175	110	145	175	ps