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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs






The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1846
Number of Logic Elements/Cells	18460
Total RAM Bits	1669248
Number of I/O	426
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s20f672c7

Typographic Conventions

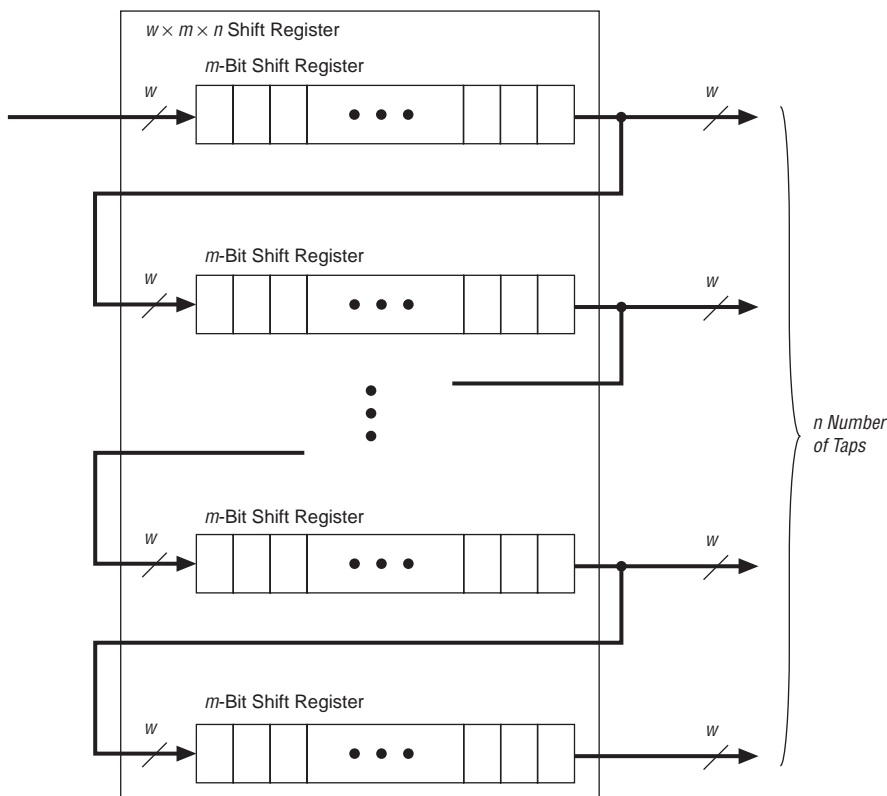
This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: Save As dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: f_{MAX} , lqdesigns directory, d: drive, chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Designs</i> .
<i>Italic type</i>	Internal timing parameters and variables are shown in italic type. Examples: <i>t_{PIA}</i> , <i>n + 1</i> . Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <file name>, <project name>.pof file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
“Subheading Title”	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.”
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, e.g., resetn. Anything that must be typed exactly as it appears is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets are used in a list of items when the sequence of the items is not important.
	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Chapter	Date/Version	Changes Made
2	July 2005 v3.2	<ul style="list-style-type: none"> Added “Clear Signals” section. Updated “Power Sequencing & Hot Socketing” section. Format changes.
	September 2004, v3.1	<ul style="list-style-type: none"> Updated fast regional clock networks description on page 2–73. Deleted the word preliminary from the “specification for the maximum time to relock is 100 μs” on page 2–90. Added information about differential SSTL and HSTL outputs in “External Clock Outputs” on page 2–92. Updated notes in Figure 2–55 on page 2–93. Added information about <i>m</i> counter to “Clock Multiplication & Division” on page 2–101. Updated Note 1 in Table 2–58 on page 2–101. Updated description of “Clock Multiplication & Division” on page 2–88. Updated Table 2–22 on page 2–102. Added references to AN 349 and AN 329 to “External RAM Interfacing” on page 2–115. Table 2–25 on page 2–116: updated the table, updated Notes 3 and 4. Notes 4, 5, and 6, are now Notes 5, 6, and 7, respectively. Updated Table 2–26 on page 2–117. Added information about PCI Compliance to page 2–120. Table 2–32 on page 2–126: updated the table and deleted Note 1. Updated reference to device pin-outs now being available on the web on page 2–130. Added Notes 4 and 5 to Table 2–36 on page 2–130. Updated Note 3 in Table 2–37 on page 2–131. Updated Note 5 in Table 2–41 on page 2–135.
	April 2004, v3.0	<ul style="list-style-type: none"> Added note 3 to rows 11 and 12 in Table 2–18. Deleted “Stratix and Stratix GX Device PLL Availability” table. Added I/O standards row in Table 2–28 that support max and min strength. Row <code>clk [1,3,8,10]</code> was removed from Table 2–30. Added checkmarks in Enhanced column for LVPECL, 3.3-V PCML, LVDS, and HyperTransport technology rows in Table 2–32. Removed the Left and Right I/O Banks row in Table 2–34. Changed RCLK values in Figures 2–50 and 2–51. External RAM Interfacing section replaced.
	November 2003, v2.2	<ul style="list-style-type: none"> Added 672-pin BGA package information in Table 2–37. Removed support for series and parallel on-chip termination. Termination Technology renamed differential on-chip termination. Updated the number of channels per PLL in Tables 2–38 through 2–42. Updated Figures 2–65 and 2–67.
	October 2003, v2.1	<ul style="list-style-type: none"> Updated DDR I information. Updated Table 2–22. Added Tables 2–25, 2–29, 2–30, and 2–72. Updated Figures 2–59, 2–65, and 2–67. Updated the Lock Detect section.

Chapter	Date/Version	Changes Made
2	July 2003, v2.0	<ul style="list-style-type: none"> Added reference on page 2-73 to Figures 2-50 and 2-51 for RCLK connections. Updated ranges for EPLL post-scale and pre-scale dividers on page 2-85. Updated PLL Reconfiguration frequency from 25 to 22 MHz on page 2-87. New requirement to assert are set signal each PLL when it has to re-acquire lock on either a new clock after loss of lock (page 2-96). Updated max input frequency for CLK [1, 3, 8, 10] from 462 to 500, Table 2-24. Renamed impedance matching to series termination throughout. Updated naming convention for DQS pins on page 2-112 to match pin tables. Added DDR SDRAM Performance Specification on page 2-117. Added external reference resistor values for terminator technology (page 2-136). Added Terminator Technology Specification on pages 2-137 and 2-138. Updated Tables 2-45 to 2-49 to reflect PLL cross-bank support for high speed differential channels at full speed. Wire bond package performance specification for “high” speed channels was increased to 624 Mbps from 462 Mbps throughout chapter.
3	July 2005, v1.3	<ul style="list-style-type: none"> Updated “Operating Modes” section. Updated “Temperature Sensing Diode” section. Updated “IEEE Std. 1149.1 (JTAG) Boundary-Scan Support” section. Updated “Configuration” section.
	January 2005, v1.2	<ul style="list-style-type: none"> Updated limits for JTAG chain of devices.
	September 2004, v1.1	<ul style="list-style-type: none"> Added new section, “Stratix Automated Single Event Upset (SEU) Detection” on page 3–12. Updated description of “Custom-Built Circuitry” on page 3–13.
	April 2003, v1.0	<ul style="list-style-type: none"> No new changes in <i>Stratix Device Handbook</i> v2.0.
4	January 2006, v3.4	<ul style="list-style-type: none"> Added Table 4–135.
	July 2005, v3.3	<ul style="list-style-type: none"> Updated Tables 4–6 and 4–30. Updated Tables 4–103 through 4–108. Updated Tables 4–114 through 4–124. Updated Table 4–129. Added Table 4–130.

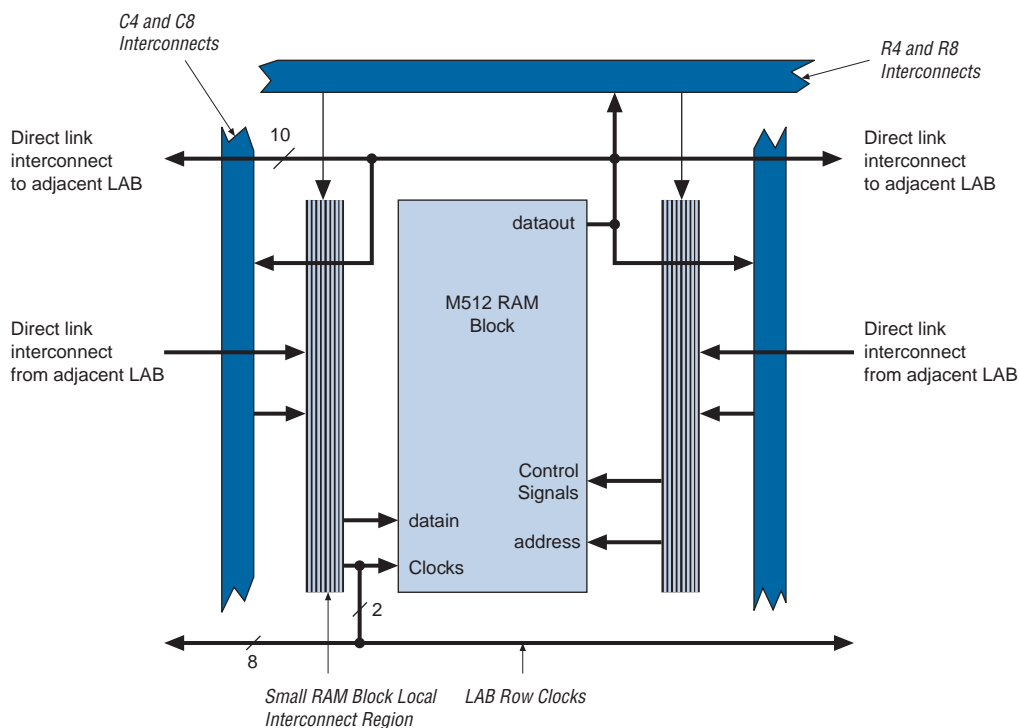
Chapter	Date/Version	Changes Made
4	October 2003, v2.1	<ul style="list-style-type: none"> Added -8 speed grade information. Updated performance information in Table 4–36. Updated timing information in Tables 4–55 through 4–96. Updated delay information in Tables 4–103 through 4–108. Updated programmable delay information in Tables 4–100 and 4–103.
	July 2003, v2.0	<ul style="list-style-type: none"> Updated clock rates in Tables 4–114 through 4–123. Updated speed grade information in the introduction on page 4-1. Corrected figures 4-1 & 4-2 and Table 4-9 to reflect how VID and VOD are specified. Added note 6 to Table 4-32. Updated Stratix Performance Table 4-35. Updated EP1S60 and EP1S80 timing parameters in Tables 4-82 to 4-93. The Stratix timing models are final for all devices. Updated Stratix IOE programmable delay chains in Tables 4-100 to 4-101. Added single-ended I/O standard output pin delay adders for loading in Table 4-102. Added spec for FPLL[10..7]CLK pins in Tables 4-104 and 4-107. Updated high-speed I/O specification for J=2 in Tables 4-114 and 4-115. Updated EPLL specification and fast PLL specification in Tables 4-116 to 4-120.
5	September 2004, v2.1	<ul style="list-style-type: none"> Updated reference to device pin-outs on page 5–1 to indicate that device pin-outs are no longer included in this manual and are now available on the Altera web site.
	April 2003, v1.0	<ul style="list-style-type: none"> No new changes in Stratix Device Handbook v2.0.

Figure 2–14. Shift Register Memory Configuration

Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The large number of M512 blocks are ideal for designs with many shallow first-in first-out (FIFO) buffers. M4K blocks provide additional resources for channelized functions that do not require large amounts of storage. The M-RAM blocks provide a large single block of RAM ideal for data packet storage. The different-sized blocks allow Stratix devices to efficiently support variable-sized memory in designs.

The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

Figure 2–16. M512 RAM Block LAB Row Interface

M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

There are 16 dedicated clock pins (CLK [15 . . 0]) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in [Figure 2–42](#). Enhanced and fast PLL outputs can also drive the global and regional clock networks.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources within the device—I/Os, LEs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. [Figure 2–42](#) shows the 16 dedicated CLK pins driving global clock networks.

Clock Multiplication & Division

Each Stratix device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times \text{post-scale counter})$ scaling factors. The input clock is divided by a pre-scale divider, n , and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{\text{IN}} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale counter, n , and one multiply counter, m , per PLL, with a range of 1 to 512 on each. There are two post-scale counters (l) for regional clock output ports, four counters (g) for global clock output ports, and up to four counters (e) for external clock outputs, all ranging from 1 to 1024 with a 50% duty cycle setting. The post-scale counters range from 1 to 512 with any non-50% duty cycle setting. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix device enhanced PLLs support a flexible clock switchover capability. [Figure 2–53](#) shows a block diagram of the switchover circuit. The switchover circuit is configurable, so you can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

VCO period from up to eight taps for individual fine step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse shift selection in steps of one VCO period. The combination of coarse and fine shifts allows phase shifting for the entire input clock period.

The equation to determine the precision of the phase shifting in degrees is: $45^\circ \div \text{post-scale counter value}$. Therefore, the maximum step size is 45° , and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

Clock Delay

In addition to the phase shift feature, the ability to fine tune the Δt clock delay provides advanced time delay shift control on each of the four PLL outputs. There are time delays for each post-scale counter (e , g , or l) from the PLL, the n counter, and m counter. Each of these can shift in 250-ps increments for a range of 3.0 ns. The m delay shifts all outputs earlier in time, while n delay shifts all outputs later in time. Individual delays on post-scale counters (e , g , and l) provide positive delay for each output. Table 2-21 shows the combined delay for each output for normal or zero delay buffer mode where Δt_e , Δt_g , or Δt_l is unique for each PLL output.

The t_{OUTPUT} for a single output can range from -3 ns to $+6$ ns. The total delay shift difference between any two PLL outputs, however, must be less than ± 3 ns. For example, shifts on two outputs of -1 and $+2$ ns is allowed, but not -1 and $+2.5$ ns because these shifts would result in a difference of 3.5 ns. If the design uses external feedback, the Δt_e delay will remove delay from outputs, represented by a negative sign (see Table 2-21). This effect occurs because the Δt_e delay is then part of the feedback loop.

Table 2-21. Output Clock Delay for Enhanced PLLs

Normal or Zero Delay Buffer Mode	External Feedback Mode
$\Delta t_{e\text{OUTPUT}} = \Delta t_n - \Delta t_m + \Delta t_e$	$\Delta t_{e\text{OUTPUT}} = \Delta t_n - \Delta t_m - \Delta t_e$ (1)
$\Delta t_{g\text{OUTPUT}} = \Delta t_n - \Delta t_m + \Delta t_g$	$\Delta t_{g\text{OUTPUT}} = \Delta t_n - \Delta t_m + \Delta t_g$
$\Delta t_{l\text{OUTPUT}} = \Delta t_n - \Delta t_m + \Delta t_l$	$\Delta t_{l\text{OUTPUT}} = \Delta t_n - \Delta t_m + \Delta t_l$

Note to Table 2-21:

(1) Δt_e removes delay from outputs in external feedback mode.

The `pllenable` pin is a dedicated pin that enables/disables PLLs. When the `pllenable` pin is low, the clock output ports are driven by GND and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the `pllenable` signal by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

The `areset` signals are reset/resynchronization inputs for each PLL. The `areset` signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the `areset` signal in designs if any of the following conditions are true:

- PLL Reconfiguration or Clock switchover enables in the design.
- Phase relationships between output clocks need to be maintained after a loss of lock condition

The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it rellocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value than desired as the PLL locks. If the system cannot tolerate this, the `clkena` signal can disable the output clocks until the PLL locks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or a `clkloss` status signal to trigger `pfdena`.

The `clkena` signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own `clkena` signal. The `clkena` signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the `g` and `l` counters. The `clkena` signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. [Figure 2-57](#) shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 2 of 2) *Note (1)*

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S25	672-pin FineLine BGA 672-pin BGA	Transmitter (2)	56	624 (4)	14	14	14	14
				624 (3)	28	28	28	28
		Receiver	58	624 (4)	14	15	15	14
				624 (3)	29	29	29	29
	780-pin FineLine BGA	Transmitter (2)	70	840 (4)	18	17	17	18
				840 (3)	35	35	35	35
		Receiver	66	840 (4)	17	16	16	17
				840 (3)	33	33	33	33
	1,020-pin FineLine BGA	Transmitter (2)	78	840 (4)	19	20	20	19
				840 (3)	39	39	39	39
		Receiver	78	840 (4)	19	20	20	19
				840 (3)	39	39	39	39

Notes to Table 2–37:

- (1) The first row for each transmitter or receiver reports the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP1S10 device, PLL 1 can drive a maximum of five channels at 840 Mbps or a maximum of 10 channels at 840 Mbps. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.
- (2) The number of channels listed includes the transmitter clock output (tx_outclock) channel. If the design requires a DDR clock, it can use an extra data channel.
- (3) These channels span across two I/O banks per side of the device. When a center PLL clocks channels in the opposite bank on the same side of the device it is called cross-bank PLL support. Both center PLLs can clock cross-bank channels simultaneously if, for example, PLL_1 is clocking all receiver channels and PLL_2 is clocking all transmitter channels. You cannot have two adjacent PLLs simultaneously clocking cross-bank receiver channels or two adjacent PLLs simultaneously clocking transmitter channels. Cross-bank allows for all receiver channels on one side of the device to be clocked on one clock while all transmitter channels on the device are clocked on the other center PLL. Crossbank PLLs are supported at full-speed, 840 Mbps. For wire-bond devices, the full-speed is 624 Mbps.
- (4) These values show the channels available for each PLL without crossing another bank.

When you span two I/O banks using cross-bank support, you can route only two load enable signals total between the PLLs. When you enable rx_data_align, you use both rxloadena and txloadena of a PLL. That leaves no loadena for the second PLL.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All Stratix® devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix devices can also use the JTAG port for configuration together with either the Quartus® II software or hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc).

Stratix devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the CONFIG_IO instruction. You can use this ability for JTAG testing before configuration when some of the Stratix pins drive or receive from other devices on the board using voltage-referenced standards. Since the Stratix device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows you to fully test the I/O connection to other devices.

The enhanced PLL reconfiguration bits are part of the JTAG chain before configuration and after power-up. After device configuration, the PLL reconfiguration bits are not part of the JTAG chain.

The JTAG pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The TDO pin voltage is determined by the V_{CCIO} of the bank where it resides. The VCCSEL pin selects whether the JTAG inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Stratix devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix devices support the JTAG instructions shown in [Table 3-1](#).

The Quartus II software has an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. In the Settings dialog box in the Assignments menu, click **Device & Pin Options**, then **General**, and then turn on the **Auto Usercode** option.

Table 4–11. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)		300		600	mV
V_{ICM}	Input common mode voltage		1.5		3.465	V
V_{OD}	Output differential voltage (single-ended)		300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low				50	mV
V_{OCM}	Output common mode voltage		2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low				50	mV
V_T	Output termination voltage			V_{CCIO}		V
R_1	Output external pull-up resistors		45	50	55	Ω
R_2	Output external pull-up resistors		45	50	55	Ω

Table 4–12. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)		300		1,000	mV
V_{ICM}	Input common mode voltage		1		2	V
V_{OD}	Output differential voltage (single-ended)	$R_L = 100 \Omega$	525	700	970	mV
V_{OCM}	Output common mode voltage	$R_L = 100 \Omega$	1.5	1.7	1.9	V
R_L	Receiver differential input resistor		90	100	110	Ω

Table 4–15. PCI-X 1.0 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{CCIO}	Output supply voltage		3.0		3.6	V
V _{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V _{IL}	Low-level input voltage		–0.5		$0.35 \times V_{CCIO}$	V
V _{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V _{OH}	High-level output voltage	I _{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V _{OL}	Low-level output voltage	I _{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 4–16. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{TT}	Termination voltage		1.35	1.5	1.65	V
V _{REF}	Reference voltage		0.88	1.0	1.12	V
V _{IH}	High-level input voltage		V _{REF} + 0.1			V
V _{IL}	Low-level input voltage				V _{REF} – 0.1	V
V _{OL}	Low-level output voltage	I _{OL} = 34 mA (3)			0.65	V

Table 4–17. GTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{TT}	Termination voltage		1.14	1.2	1.26	V
V _{REF}	Reference voltage		0.74	0.8	0.86	V
V _{IH}	High-level input voltage		V _{REF} + 0.05			V
V _{IL}	Low-level input voltage				V _{REF} – 0.05	V
V _{OL}	Low-level output voltage	I _{OL} = 40 mA (3)			0.4	V

Table 4–43. Routing Delay Internal Timing Microparameter Descriptions (Part 2 of 2)

Symbol	Parameter
t_{C4}	Delay for a C4 line with average loading; covers a distance of four LAB rows.
t_{C8}	Delay for a C8 line with average loading; covers a distance of eight LAB rows.
t_{C16}	Delay for a C16 line with average loading; covers a distance of 16 LAB rows.
t_{LOCAL}	Local interconnect delay, for connections within a LAB, and for the final routing hop of connections to LABs, DSP blocks, RAM blocks and I/Os.

Table 4–44. LE Internal Timing Microparameters

Parameter	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	10		10		11		13		ps
t_H	100		100		114		135		ps
t_{CO}		156		176		202		238	ps
t_{LUT}		366		459		527		621	ps
t_{CLR}	100		100		114		135		ps
t_{PRE}	100		100		114		135		ps
t_{CLKHL}	1000		1111		1190		1400		ps

Table 4–45. IOE Internal TSU Microparameter by Device Density (Part 1 of 2)

Device	Symbol	-5		-6		-7		-8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
EP1S10	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	176		80		80		80		ps
EP1S20	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	76		80		80		80		ps
EP1S25	t_{SU_R}	276		280		280		280		ps
	t_{SU_C}	276		280		280		280		ps
EP1S30	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	176		180		180		180		ps

Table 4–69. EP1S25 External I/O Timing on Column Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.371		1.471		1.657		1.916		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.809	5.516	2.809	5.890	2.809	6.429	2.809	7.155	ns
t_{XZ}	2.749	5.390	2.749	5.758	2.749	6.305	2.749	7.040	ns
t_{ZX}	2.749	5.390	2.749	5.758	2.749	6.305	2.749	7.040	ns
t_{INSUPLL}	1.271		1.327		1.491		1.677		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
t_{OUTCOPLL}	1.124	2.396	1.124	2.492	1.124	2.522	1.124	2.602	ns
t_{XZPLL}	1.064	2.270	1.064	2.360	1.064	2.398	1.064	2.487	ns
t_{ZXPLL}	1.064	2.270	1.064	2.360	1.064	2.398	1.064	2.487	ns

Table 4–70. EP1S25 External I/O Timing on Row Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.429		2.631		2.990		3.503		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.376	4.821	2.376	5.131	2.376	5.538	2.376	6.063	ns
t_{XZ}	2.403	4.875	2.403	5.187	2.403	5.606	2.403	6.145	ns
t_{ZX}	2.403	4.875	2.403	5.187	2.403	5.606	2.403	6.145	ns

Table 4–110. Stratix IOE Programmable Delays on Row Pins *Note (1)*

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off		3,970		4,367		5,022		5,908	ps
	Small		3,390		3,729		4,288		5,045	ps
	Medium		2,810		3,091		3,554		4,181	ps
	Large		173		181		208		245	ps
	On		173		181		208		245	ps
Decrease input delay to input register	Off		3,900		4,290		4,933		5,804	ps
	On		0		0		0		0	ps
Decrease input delay to output register	Off		1,240		1,364		1,568		1,845	ps
	On		0		0		0		0	ps
Increase delay to output pin	Off		0		0		0		0	ps
	On		397		417		417		417	ps
Increase delay to output enable pin	Off		0		0		0		0	ps
	On		348		383		441		518	ps
Increase output clock enable delay	Off		0		0		0		0	ps
	Small		180		198		227		267	ps
	Large		260		286		328		386	ps
	On		260		286		328		386	ps
Increase input clock enable delay	Off		0		0		0		0	ps
	Small		180		198		227		267	ps
	Large		260		286		328		386	ps
	On		260		286		328		386	ps
Increase output enable clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase t_{ZX} delay to output pin	Off		0		0		0		0	ps
	On		1,993		2,092		2,092		2,092	ps

Note to Table 4–109 and Table 4–110:

- (1) The delay chain delays vary for different device densities. These timing values only apply to EP1S30 and EP1S40 devices. Reference the timing information reported by the Quartus II software for other devices.

Table 4–117. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
GTL+	250	200	200	MHz
SSTL-3 Class I	300	250	250	MHz
SSTL-3 Class II	300	250	250	MHz
SSTL-2 Class I	300	250	250	MHz
SSTL-2 Class II	300	250	250	MHz
SSTL-18 Class I	300	250	250	MHz
SSTL-18 Class II	300	250	250	MHz
1.5-V HSTL Class I	300	180	180	MHz
1.5-V HSTL Class II	300	180	180	MHz
1.8-V HSTL Class I	300	180	180	MHz
1.8-V HSTL Class II	300	180	180	MHz
3.3-V PCI	422	390	390	MHz
3.3-V PCI-X 1.0	422	390	390	MHz
Compact PCI	422	390	390	MHz
AGP 1×	422	390	390	MHz
AGP 2×	422	390	390	MHz
CTT	250	180	180	MHz
Differential 1.5-V HSTL C1	300	180	180	MHz
LVPECL (1)	422	400	400	MHz
PCML (1)	215	200	200	MHz
LVDS (1)	422	400	400	MHz
HyperTransport technology (1)	422	400	400	MHz

Table 4–118. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[10..7]CLK Pins in Wire-Bond Packages (Part 1 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 3 of 4) Notes (1), (2)														
Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SW	PCML ($J = 4, 7, 8, 10$)	750			750			800			800			ps
	PCML ($J = 2$)	900			900			1,200			1,200			ps
	PCML ($J = 1$)	1,500			1,500			1,700			1,700			ps
	LVDS and LVPECL ($J = 1$)	500			500			550			550			ps
	LVDS, LVPECL, HyperTransport technology ($J = 2$ through 10)	440			440			500			500			ps
Input jitter tolerance (peak-to-peak)	All			250			250			250			250	ps
Output jitter (peak-to-peak)	All			160			160			200			200	ps
Output t_{RISE}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	120	170	200	120	170	200	ps
	LVPECL	90	130	150	90	130	150	100	135	150	100	135	150	ps
	PCML	80	110	135	80	110	135	80	110	135	80	110	135	ps
Output t_{FALL}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	110	170	200	110	170	200	ps
	LVPECL	90	130	160	90	130	160	100	135	160	100	135	160	ps
	PCML	105	140	175	105	140	175	110	145	175	110	145	175	ps

