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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1846
Number of Logic Elements/Cells	18460
Total RAM Bits	1669248
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s20f780c5

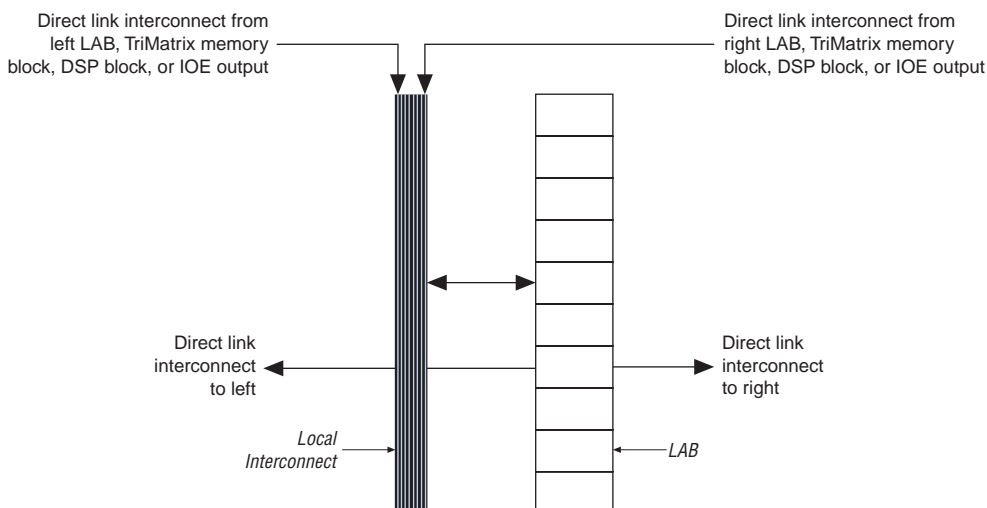


Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

- Chapter 1. Introduction
Revised: *July 2005*
Part number: *S51001-3.2*
- Chapter 2. Stratix Architecture
Revised: *July 2005*
Part number: *S51002-3.2*
- Chapter 3. Configuration & Testing
Revised: *July 2005*
Part number: *S51003-1.3*
- Chapter 4. DC & Switching Characteristics
Revised: *January 2006*
Part number: *S51004-3.4*
- Chapter 5. Reference & Ordering Information
Revised: *September 2004*
Part number: *S51005-2.1*

Chapter	Date/Version	Changes Made
2	July 2003, v2.0	<ul style="list-style-type: none"> Added reference on page 2-73 to Figures 2-50 and 2-51 for RCLK connections. Updated ranges for EPLL post-scale and pre-scale dividers on page 2-85. Updated PLL Reconfiguration frequency from 25 to 22 MHz on page 2-87. New requirement to assert are set signal each PLL when it has to re-acquire lock on either a new clock after loss of lock (page 2-96). Updated max input frequency for CLK [1, 3, 8, 10] from 462 to 500, Table 2-24. Renamed impedance matching to series termination throughout. Updated naming convention for DQS pins on page 2-112 to match pin tables. Added DDR SDRAM Performance Specification on page 2-117. Added external reference resistor values for terminator technology (page 2-136). Added Terminator Technology Specification on pages 2-137 and 2-138. Updated Tables 2-45 to 2-49 to reflect PLL cross-bank support for high speed differential channels at full speed. Wire bond package performance specification for “high” speed channels was increased to 624 Mbps from 462 Mbps throughout chapter.
3	July 2005, v1.3	<ul style="list-style-type: none"> Updated “Operating Modes” section. Updated “Temperature Sensing Diode” section. Updated “IEEE Std. 1149.1 (JTAG) Boundary-Scan Support” section. Updated “Configuration” section.
	January 2005, v1.2	<ul style="list-style-type: none"> Updated limits for JTAG chain of devices.
	September 2004, v1.1	<ul style="list-style-type: none"> Added new section, “Stratix Automated Single Event Upset (SEU) Detection” on page 3–12. Updated description of “Custom-Built Circuitry” on page 3–13.
	April 2003, v1.0	<ul style="list-style-type: none"> No new changes in <i>Stratix Device Handbook</i> v2.0.
4	January 2006, v3.4	<ul style="list-style-type: none"> Added Table 4–135.
	July 2005, v3.3	<ul style="list-style-type: none"> Updated Tables 4–6 and 4–30. Updated Tables 4–103 through 4–108. Updated Tables 4–114 through 4–124. Updated Table 4–129. Added Table 4–130.

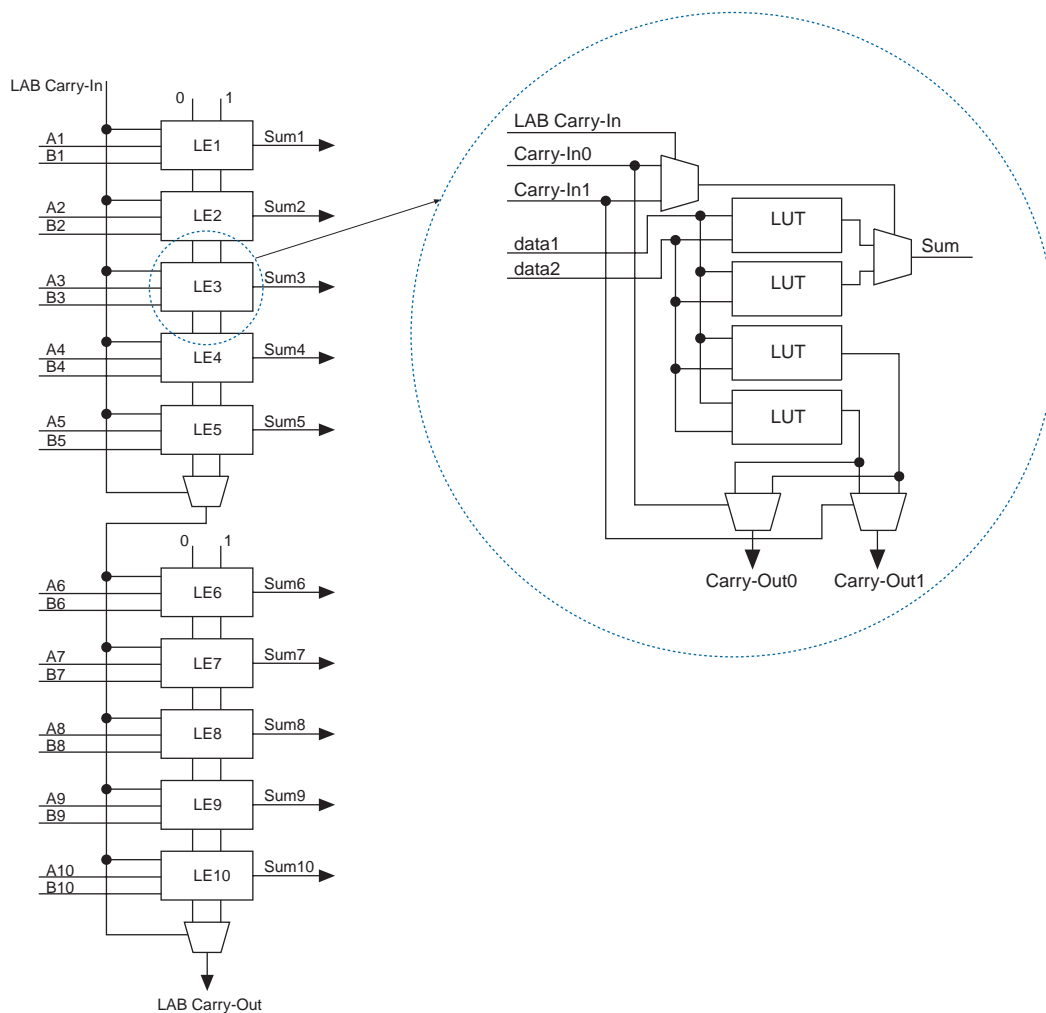
Figure 2–3. Direct Link Connection

LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

Figure 2–8. Carry Select Chain

Clear & Preset Logic Control

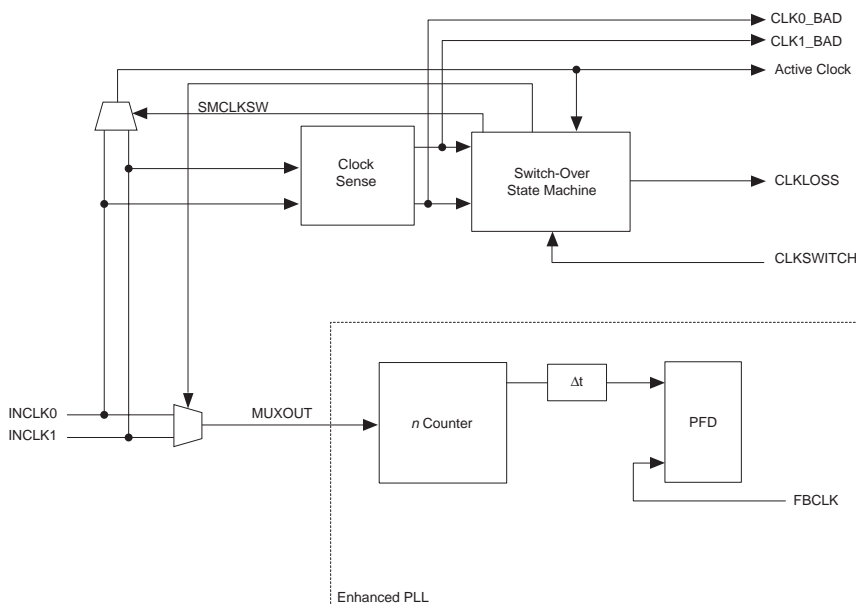
LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix devices support simultaneous preset/

Table 2–19 shows the enhanced PLL and fast PLL features in Stratix devices.

Table 2–19. Stratix PLL Features		
Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	$m/(n \times \text{post-scale counter})$ (1)	$m/(\text{post-scale counter})$ (2)
Phase shift	Down to 156.25-ps increments (3), (4)	Down to 125-ps increments (3), (4)
Delay shift	250-ps increments for ± 3 ns	
Clock switchover	✓	
PLL reconfiguration	✓	
Programmable bandwidth	✓	
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	3 (5)
Number of external clock outputs	Four differential/eight singled-ended or one single-ended (6)	(7)
Number of feedback clock inputs	2 (8)	

Notes to Table 2–19:

- (1) For enhanced PLLs, m , n , range from 1 to 512 and post-scale counters g , l , e range from 1 to 1024 with 50% duty cycle. With a non-50% duty cycle the post-scale counters g , l , e range from 1 to 512.
- (2) For fast PLLs, m and post-scale counters range from 1 to 32.
- (3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
- (4) For degree increments, Stratix devices can shift all output frequencies in increments of at least 45° . Smaller degree increments are possible depending on the frequency and divide parameters.
- (5) PLLs 7, 8, 9, and 10 have two output ports per PLL. PLLs 1, 2, 3, and 4 have three output ports per PLL.
- (6) Every Stratix device has two enhanced PLLs (PLLs 5 and 6) with either eight single-ended outputs or four differential outputs each. Two additional enhanced PLLs (PLLs 11 and 12) in EP1S80, EP1S60, and EP1S40 devices each have one single-ended output. Devices in the 780 pin FineLine BGA packages do not support PLLs 11 and 12.
- (7) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
- (8) Every Stratix device has two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–53. Clock Switchover Circuitry

There are two possible ways to use the clock switchover feature.

- Use automatic switchover circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of [Figure 2–53](#). In this case, the secondary clock becomes the reference clock for the PLL.
- Use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than $\pm 20\%$. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. You can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

bandwidth is tuned by varying the charge pump current, loop filter resistor value, high frequency capacitor value, and m counter value. You can manually adjust these values if desired. Bandwidth is programmable from 200 kHz to 1.5 MHz.

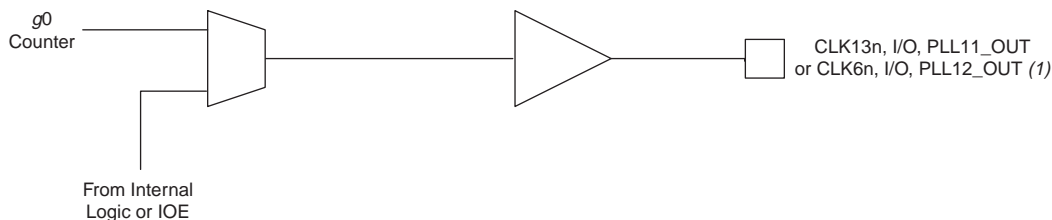
External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). Differential SSTL and HSTL outputs are implemented using 2 single-ended output buffers which are programmed to have opposite polarity. In Quartus II software, simply assign the appropriate differential I/O standard and the software will implement the inversion. See [Figure 2–55](#).

Table 2–20. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2)

I/O Standard	Input			Output
	INCLK	FBIN	PLENABLE	EXTCLK
1.5-V HSTL Class II	✓	✓		✓
1.8-V HSTL Class I	✓	✓		✓
1.8-V HSTL Class II	✓	✓		✓
SSTL-18 Class I	✓	✓		✓
SSTL-18 Class II	✓	✓		✓
SSTL-2 Class I	✓	✓		✓
SSTL-2 Class II	✓	✓		✓
SSTL-3 Class I	✓	✓		✓
SSTL-3 Class II	✓	✓		✓
AGP (1× and 2×)	✓	✓		✓
CTT	✓	✓		✓

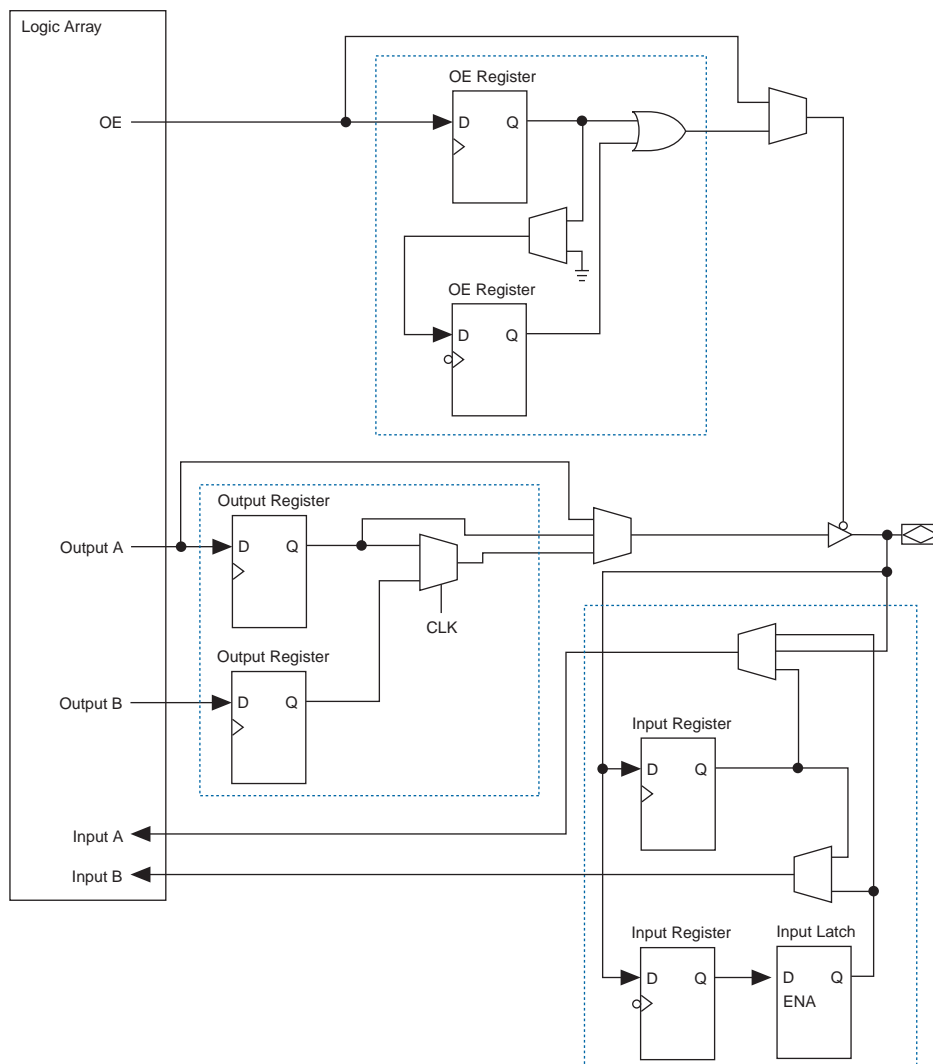
Enhanced PLLs 11 and 12 support one single-ended output each (see [Figure 2–56](#)). These outputs do not have their own VCC and GND signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

Figure 2–56. External Clock Outputs for Enhanced PLLs 11 & 12

Note to Figure 2–56:

(1) For PLL 11, this pin is CLK13n; for PLL 12 this pin is CLK7n.

Stratix devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

Figure 2–59. Stratix IOE Structure

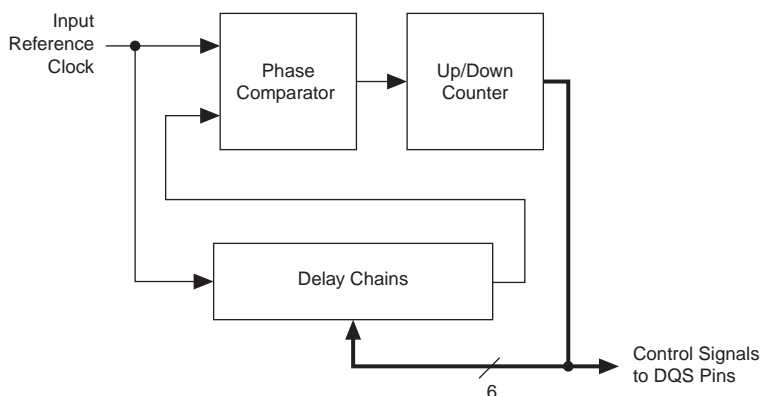
The IOEs are located in I/O blocks around the periphery of the Stratix device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects.

Figure 2–60 shows how a row I/O block connects to the logic array.

Figure 2–61 shows how a column I/O block connects to the logic array.

shift by the same degree amount. For example, all 10 DQS pins on the top of the device can be shifted by 90° and all 10 DQS pins on the bottom of the device can be shifted by 72° . The reference circuits require a maximum of 256 system reference clock cycles to set the correct phase on the DQS delay elements. Figure 2–69 illustrates the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–69. Simplified Diagram of the DQS Phase-Shift Circuitry



See the *External Memory Interfaces* chapter in the *Stratix Device Handbook, Volume 2* for more information on external memory interfaces.

Programmable Drive Strength

The output buffer for each Stratix device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTTL and LVCMOS standard has several levels of drive strength that the user can control. SSTL-3 Class I and II, SSTL-2 Class I and II, HSTL Class I and II, and 3.3-V GTL+ support a minimum setting, the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.



For more information on I/O standards supported by Stratix devices, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook, Volume 2*.

Stratix devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in [Figure 2–70](#). The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in [Table 2–31](#) except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. [Table 2–32](#) shows I/O standard support for each I/O bank.

The transmitter external clock output is transmitted on a data channel. The `txclk` pin for each bank is located in between data transmitter pins. For $\times 1$ clocks (e.g., 622 Mbps, 622 MHz), the high-speed PLL clock bypasses the SERDES to drive the output pins. For half-rate clocks (e.g., 622 Mbps, 311 MHz) or any other even-numbered factor such as 1/4, 1/7, 1/8, or 1/10, the SERDES automatically generates the clock in the Quartus II software.

For systems that require more than four or eight high-speed differential I/O clock domains, a SERDES bypass implementation is possible using IOEs.

Byte Alignment

For high-speed source synchronous interfaces such as POS-PHY 4, XSBI, RapidIO, and HyperTransport technology, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols since the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving LE resources. An input signal to each fast PLL can stall deserializer parallel data outputs by one bit period. You can use an LE-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Power Sequencing & Hot Socketing

Because Stratix devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the `VCCIO` and `VCCINT` power supplies may be powered in any order.

Although you can power up or down the `VCCIO` and `VCCINT` power supplies in any sequence, you should not power down any I/O banks that contain configuration pins while leaving other I/O banks powered on. For power up and power down, all supplies (`VCCINT` and all `VCCIO` power planes) must be powered up and down within 100 ms of each other. This prevents I/O pins from driving out.

Signals can be driven into Stratix devices before and during power up without damaging the device. In addition, Stratix devices do not drive out during power up. Once operating conditions are reached and the device is configured, Stratix devices operate as specified by the user. For more information, see *Hot Socketing* in the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2*.

Operating Conditions

Stratix® devices are offered in both commercial and industrial grades. Industrial devices are offered in -6 and -7 speed grades and commercial devices are offered in -5 (fastest), -6, -7, and -8 speed grades. This section specifies the operation conditions for operating junction temperature, V_{CCINT} and V_{CCIO} voltage levels, and input voltage requirements. The voltage specifications in this section are specified at the pins of the device (and not the power supply). If the device operates outside these ranges, then all DC and AC specifications are not guaranteed. Furthermore, the reliability of the device may be affected. The timing parameters in this chapter apply to both commercial and industrial temperature ranges unless otherwise stated.

Tables 4–1 through 4–8 provide information on absolute maximum ratings.

Table 4–1. Stratix Device Absolute Maximum Ratings Notes (1), (2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage (3)		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias		135	°C

Table 4–2. Stratix Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(4)	1.425	1.575	V

Table 4–20. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		$V_{REF} + 0.18$		3.0	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		$V_{REF} - 0.18$	V
$V_{IH(AC)}$	High-level AC input voltage		$V_{REF} + 0.35$			V
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.35$	V
V_{OH}	High-level output voltage	$I_{OH} = -8.1 \text{ mA}$ (3)	$V_{TT} + 0.57$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8.1 \text{ mA}$ (3)			$V_{TT} - 0.57$	V

Table 4–21. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		$V_{REF} - 0.18$	V
$V_{IH(AC)}$	High-level AC input voltage		$V_{REF} + 0.35$			V
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.35$	V
V_{OH}	High-level output voltage	$I_{OH} = -16.4 \text{ mA}$ (3)	$V_{TT} + 0.76$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16.4 \text{ mA}$ (3)			$V_{TT} - 0.76$	V

Table 4–22. SSTL-3 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
$V_{IH(DC)}$	High-level DC input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		$V_{REF} - 0.2$	V
$V_{IH(AC)}$	High-level AC input voltage		$V_{REF} + 0.4$			V

Table 4–25. 3.3-V AGP 1× Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{OH}	High-level output voltage	I _{OUT} = –0.5 mA	0.9 × V _{CCIO}		3.6	V
V _{OL}	Low-level output voltage	I _{OUT} = 1.5 mA			0.1 × V _{CCIO}	V

Table 4–26. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V _{REF}	Input reference voltage		0.68	0.75	0.9	V
V _{TT}	Termination voltage		0.7	0.75	0.8	V
V _{IH} (DC)	DC high-level input voltage		V _{REF} + 0.1			V
V _{IL} (DC)	DC low-level input voltage		–0.3		V _{REF} – 0.1	V
V _{IH} (AC)	AC high-level input voltage		V _{REF} + 0.2			V
V _{IL} (AC)	AC low-level input voltage				V _{REF} – 0.2	V
V _{OH}	High-level output voltage	I _{OH} = –8 mA (3)	V _{CCIO} – 0.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA (3)			0.4	V

Table 4–27. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V _{REF}	Input reference voltage		0.68	0.75	0.9	V
V _{TT}	Termination voltage		0.7	0.75	0.8	V
V _{IH} (DC)	DC high-level input voltage		V _{REF} + 0.1			V
V _{IL} (DC)	DC low-level input voltage		–0.3		V _{REF} – 0.1	V
V _{IH} (AC)	AC high-level input voltage		V _{REF} + 0.2			V
V _{IL} (AC)	AC low-level input voltage				V _{REF} – 0.2	V
V _{OH}	High-level output voltage	I _{OH} = –16 mA (3)	V _{CCIO} – 0.4			V
V _{OL}	Low-level output voltage	I _{OL} = 16 mA (3)			0.4	V

Table 4–36. Stratix Performance (Part 2 of 2) Notes (1), (2)

Applications		Resources Used			Performance				
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Units
TriMatrix memory M-RAM block	True dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	175.74	MHz
	Single port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Single port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
DSP block	9 × 9-bit multiplier (3)	0	0	1	335.0	293.94	255.68	217.24	MHz
	18 × 18-bit multiplier (4)	0	0	1	278.78	237.41	206.52	175.50	MHz
	36 × 36-bit multiplier (4)	0	0	1	148.25	134.71	117.16	99.59	MHz
	36 × 36-bit multiplier (5)	0	0	1	278.78	237.41	206.52	175.5	MHz
	18-bit, 4-tap FIR filter	0	0	1	278.78	237.41	206.52	175.50	MHz
Larger Designs	8-bit, 16-tap parallel FIR filter	58	0	4	141.26	133.49	114.88	100.28	MHz
	8-bit, 1,024-point FFT function	870	5	1	261.09	235.51	205.21	175.22	MHz

Notes to Table 4–36:

- (1) These design performance numbers were obtained using the Quartus II software.
- (2) Numbers not listed will be included in a future version of the data sheet.
- (3) This application uses registered inputs and outputs.
- (4) This application uses registered multiplier input and output stages within the DSP block.
- (5) This application uses registered multiplier input, pipeline, and output stages within the DSP block.

Table 4–57. EP1S10 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.647		1.692		1.940		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.619	5.184	2.619	5.515	2.619	5.999	NA	NA	ns
t_{xZ}	2.559	5.058	2.559	5.383	2.559	5.875	NA	NA	ns
t_{ZX}	2.559	5.058	2.559	5.383	2.559	5.875	NA	NA	ns
t_{INSUPLL}	1.239		1.229		1.374		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
t_{OUTCOPLL}	1.109	2.372	1.109	2.436	1.109	2.492	NA	NA	ns
t_{xZPLL}	1.049	2.246	1.049	2.304	1.049	2.368	NA	NA	ns
t_{ZXPLL}	1.049	2.246	1.049	2.304	1.049	2.368	NA	NA	ns

Table 4–58. EP1S10 External I/O Timing on Row Pin Using Fast Regional Clock Network *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.212		2.403		2.759		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.391	4.838	2.391	5.159	2.391	5.569	NA	NA	ns
t_{xZ}	2.418	4.892	2.418	5.215	2.418	5.637	NA	NA	ns
t_{ZX}	2.418	4.892	2.418	5.215	2.418	5.637	NA	NA	ns

Tables 4–73 through 4–78 show the external timing parameters on column and row pins for EP1S30 devices.

Table 4–73. EP1S30 External I/O Timing on Column Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.502		2.680		3.062		3.591		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.473	4.965	2.473	5.329	2.473	5.784	2.473	6.392	ns
t_{XZ}	2.413	4.839	2.413	5.197	2.413	5.660	2.413	6.277	ns
t_{ZX}	2.413	4.839	2.413	5.197	2.413	5.660	2.413	6.277	ns

Table 4–74. EP1S30 External I/O Timing on Column Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.286		2.426		2.769		3.249		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.641	5.225	2.641	5.629	2.641	6.130	2.641	6.796	ns
t_{XZ}	2.581	5.099	2.581	5.497	2.581	6.006	2.581	6.681	ns
t_{ZX}	2.581	5.099	2.581	5.497	2.581	6.006	2.581	6.681	ns
t_{INSUPLL}	1.200		1.185		1.344		1.662		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
t_{OUTCOPLL}	1.108	2.367	1.108	2.534	1.108	2.569	1.108	2.517	ns
t_{XZPLL}	1.048	2.241	1.048	2.402	1.048	2.445	1.048	2.402	ns
t_{ZXPLL}	1.048	2.241	1.048	2.402	1.048	2.445	1.048	2.402	ns

Table 4–75. EP1S30 External I/O Timing on Column Pins Using Global Clock Networks (Part 1 of 2)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.935		2.029		2.310		2.709		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.814	5.532	2.814	5.980	2.814	6.536	2.814	7.274	ns

Table 4–105. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
CTT		973		1,021		1,021		1,021	ps
SSTL-3 Class I		719		755		755		755	ps
SSTL-3 Class II		146		153		153		153	ps
SSTL-2 Class I		678		712		712		712	ps
SSTL-2 Class II		223		234		234		234	ps
SSTL-18 Class I		1,032		1,083		1,083		1,083	ps
SSTL-18 Class II		447		469		469		469	ps
1.5-V HSTL Class I		660		693		693		693	ps
1.5-V HSTL Class II		537		564		564		564	ps
1.8-V HSTL Class I		304		319		319		319	ps
1.8-V HSTL Class II		231		242		242		242	ps

Table 4–106. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,518		1,594		1,594		1,594	ps
	4 mA		746		783		783		783	ps
	8 mA		96		100		100		100	ps
	12 mA		0		0		0		0	ps
3.3-V LVTTTL	4 mA		1,518		1,594		1,594		1,594	ps
	8 mA		1,038		1,090		1,090		1,090	ps
	12 mA		521		547		547		547	ps
	16 mA		414		434		434		434	ps
	24 mA		0		0		0		0	ps
2.5-V LVTTTL	2 mA		2,032		2,133		2,133		2,133	ps
	8 mA		699		734		734		734	ps
	12 mA		374		392		392		392	ps
	16 mA		165		173		173		173	ps
1.8-V LVTTTL	2 mA		3,714		3,899		3,899		3,899	ps
	8 mA		1,055		1,107		1,107		1,107	ps
	12 mA		830		871		871		871	ps

