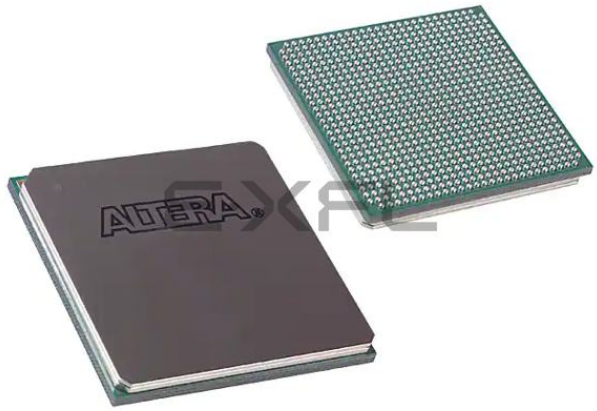

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1846
Number of Logic Elements/Cells	18460
Total RAM Bits	1669248
Number of I/O	586
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s20f780c6n

Chapter	Date/Version	Changes Made
4	January 2005, 3.2	• Updated rise and fall input values.
	September 2004, v3.1	• Updated Note 3 in Table 4–8 on page 4–4. • Updated Table 4–10 on page 4–6. • Updated Table 4–20 on page 4–12 through Table 4–23 on page 4–13. Added rows $V_{IL(AC)}$ and $V_{IH(AC)}$ to each table. • Updated Table 4–26 on page 4–14 through Table 4–29 on page 4–15. • Updated Table 4–31 on page 4–16. • Updated description of "External Timing Parameters" on page 4–33. • Updated Table 4–36 on page 4–20. • Added signals t_{OUTCO}, T_{XZ}, and T_{ZX} to Figure 4–4 on page 4–33. • Added rows $t_{M512CLKENSU}$ and $t_{M512CLKENH}$ to Table 4–40 on page 4–24. • Added rows $t_{M4CLKENSU}$ and $t_{M4CLKENH}$ to Table 4–41 on page 4–24. • Updated Note 2 in Table 4–54 on page 4–35. • Added rows $t_{MRAMCLKENSU}$ and $t_{MRAMCLKENH}$ to Table 4–42 on page 4–25. • Updated Table 4–46 on page 4–29. • Updated Table 4–47 on page 4–29.

Features

The Stratix family offers the following features:

- 10,570 to 79,040 LEs; see Table 1–1
- Up to 7,427,520 RAM bits (928,440 bytes) available without reducing logic resources
- TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (faster than 300 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 22 clocking resources per device region
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support on up to 116 channels with up to 80 channels optimized for 840 megabits per second (Mbps)
- Support for high-speed networking and communications bus standards including RapidIO, UTOPIA IV, CSIX, HyperTransport™ technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
- Differential on-chip termination support for LVDS
- Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
- Support for 66-MHz PCI (64 and 32 bit) in -6 and faster speed-grade devices, support for 33-MHz PCI (64 and 32 bit) in -8 and faster speed-grade devices
- Support for 133-MHz PCI-X 1.0 in -5 speed-grade devices
- Support for 100-MHz PCI-X 1.0 in -6 and faster speed-grade devices
- Support for 66-MHz PCI-X 1.0 in -7 speed-grade devices
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions
- Support for remote configuration updates

Table 2–2 shows the Stratix device's routing scheme.

Table 2–2. Stratix Device Routing Scheme

Source	Destination																
	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R8 Interconnect	R24 Interconnect	C4 Interconnect	C8 Interconnect	C16 Interconnect	LE	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
LUT Chain											✓						
Register Chain											✓						
Local Interconnect											✓	✓	✓	✓	✓	✓	✓
Direct Link Interconnect			✓														
R4 Interconnect			✓		✓		✓	✓		✓							
R8 Interconnect			✓			✓			✓								
R24 Interconnect					✓		✓	✓		✓							
C4 Interconnect			✓		✓			✓									
C8 Interconnect			✓			✓			✓								
C16 Interconnect					✓		✓	✓		✓							
LE	✓	✓	✓	✓	✓	✓		✓	✓								
M512 RAM Block			✓	✓	✓	✓		✓	✓								
M4K RAM Block			✓	✓	✓	✓		✓	✓								
M-RAM Block								✓	✓								
DSP Blocks			✓	✓	✓	✓		✓	✓								
Column IOE				✓				✓	✓	✓							
Row IOE				✓		✓	✓	✓	✓	✓							

M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

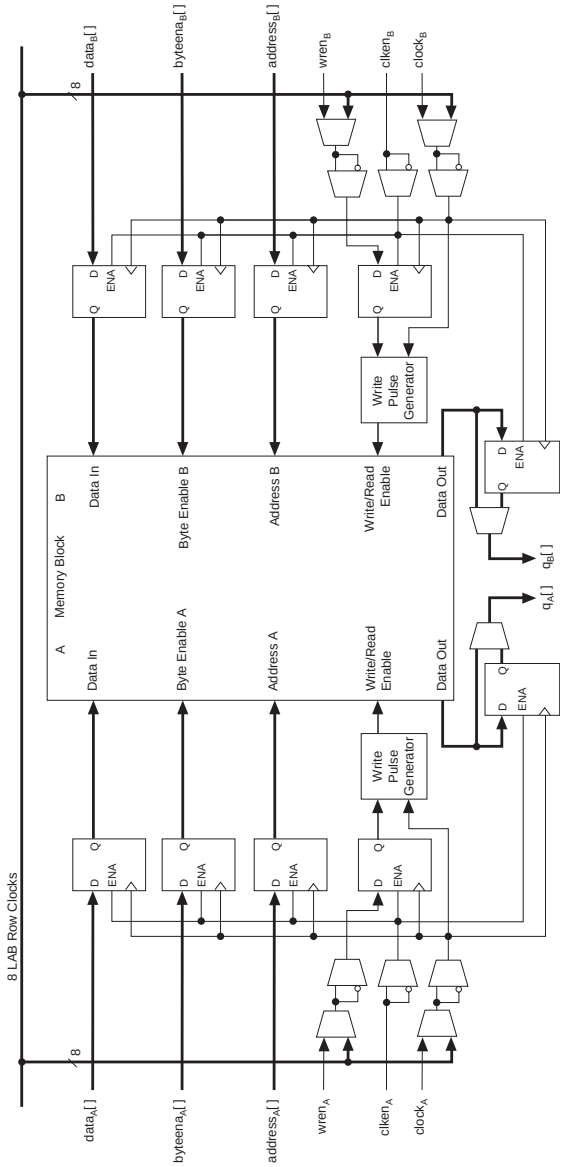
- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO RAM

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed. The memory address and output width can be configured as 64K × 8 (or 64K × 9 bits), 32K × 16 (or 32K × 18 bits), 16K × 32 (or 16K × 36 bits), 8K × 64 (or 8K × 72 bits), and 4K × 128 (or 4K × 144 bits). The 4K × 128 configuration is unavailable in true dual-port mode because there are a total of 144 data output drivers in the block. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–8 and 2–9 summarize the possible M-RAM block configurations:

Table 2–8. M-RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port				
	64K × 9	32K × 18	16K × 36	8K × 72	4K × 144
64K × 9	✓	✓	✓	✓	
32K × 18	✓	✓	✓	✓	
16K × 36	✓	✓	✓	✓	
8K × 72	✓	✓	✓	✓	
4K × 144					✓

Figure 2–24. Independent Clock Mode Notes (1), (2)



Notes to Figure 2–24

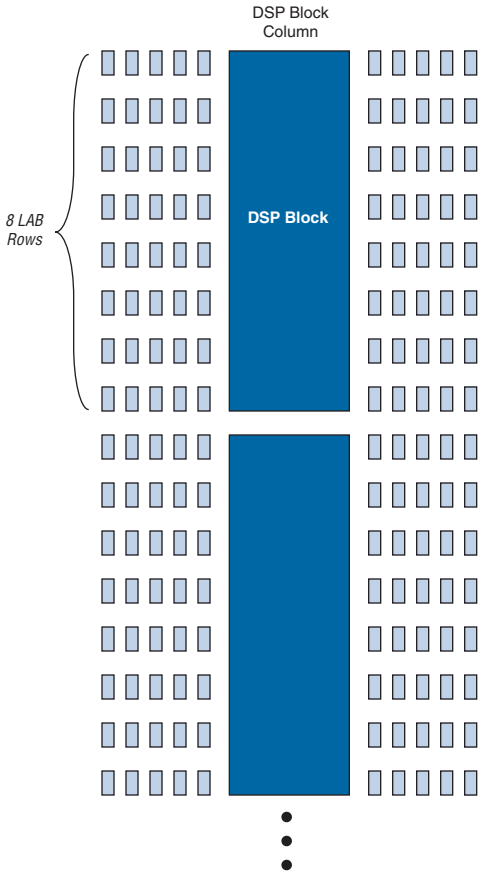
(1) All registers shown have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–25 and 2–26 show the memory block in input/output clock mode.

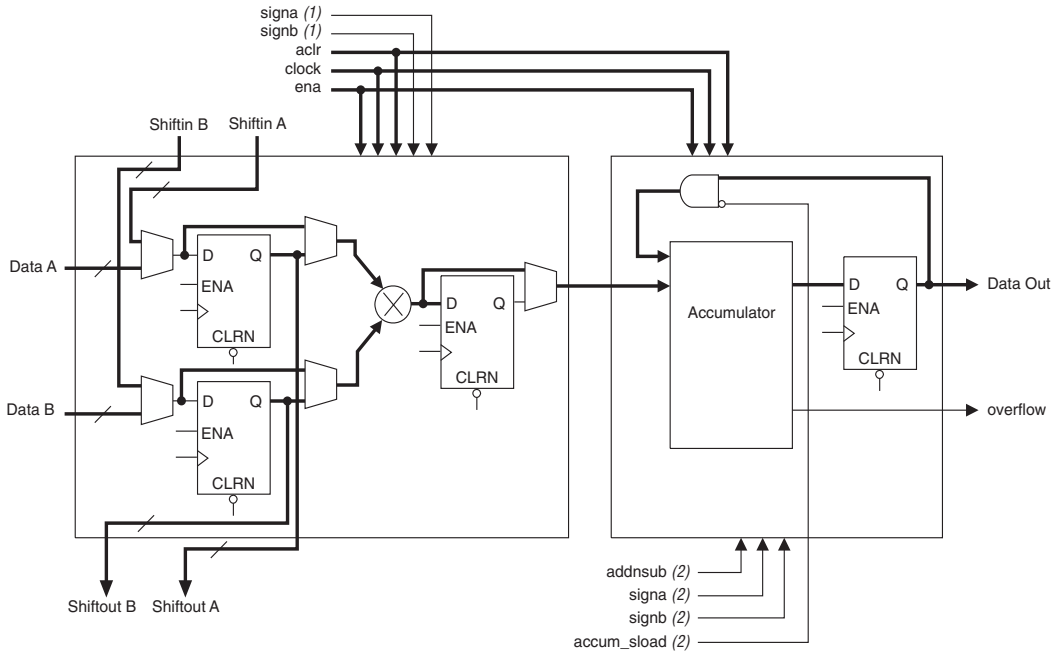
Figure 2–29. DSP Blocks Arranged in Columns



Multiply-Accumulator Mode

In multiply-accumulator mode (see Figure 2–37), the DSP block drives multiplied results to the adder/subtractor/accumulator block configured as an accumulator. You can implement one or two multiply-accumulators up to 18 × 18 bits in one DSP block. The first and third multiplier sub-blocks are unused in this mode, because only one multiplier can feed one of two accumulators. The multiply-accumulator output can be up to 52 bits—a maximum of a 36-bit result with 16 bits of accumulation. The `accum_sload` and `overflow` signals are only available in this mode. The `addnsub` signal can set the accumulator for decimation and the `overflow` signal indicates underflow condition.

Figure 2–37. Multiply-Accumulate Mode



Notes to Figure 2–37:
(1) These signals are not registered or registered once to match the data path pipeline.
(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

Two-Multipliers Adder Mode

The two-multipliers adder mode uses the adder/subtractor/accumulator block to add or subtract the outputs of the multiplier block, which is useful for applications such as FFT functions and complex FIR filters. A

VCO period from up to eight taps for individual fine step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse shift selection in steps of one VCO period. The combination of coarse and fine shifts allows phase shifting for the entire input clock period.

The equation to determine the precision of the phase shifting in degrees is: 45° ÷ post-scale counter value. Therefore, the maximum step size is 45°, and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

Clock Delay

In addition to the phase shift feature, the ability to fine tune the Δt clock delay provides advanced time delay shift control on each of the four PLL outputs. There are time delays for each post-scale counter (*e*, *g*, or *l*) from the PLL, the *n* counter, and *m* counter. Each of these can shift in 250-ps increments for a range of 3.0 ns. The *m* delay shifts all outputs earlier in time, while *n* delay shifts all outputs later in time. Individual delays on post-scale counters (*e*, *g*, and *l*) provide positive delay for each output. Table 2–21 shows the combined delay for each output for normal or zero delay buffer mode where Δt_e, Δt_g, or Δt_l is unique for each PLL output.

The t_{OUTPUT} for a single output can range from –3 ns to +6 ns. The total delay shift difference between any two PLL outputs, however, must be less than ±3 ns. For example, shifts on two outputs of –1 and +2 ns is allowed, but not –1 and +2.5 ns because these shifts would result in a difference of 3.5 ns. If the design uses external feedback, the Δt_e delay will remove delay from outputs, represented by a negative sign (see Table 2–21). This effect occurs because the Δt_e delay is then part of the feedback loop.

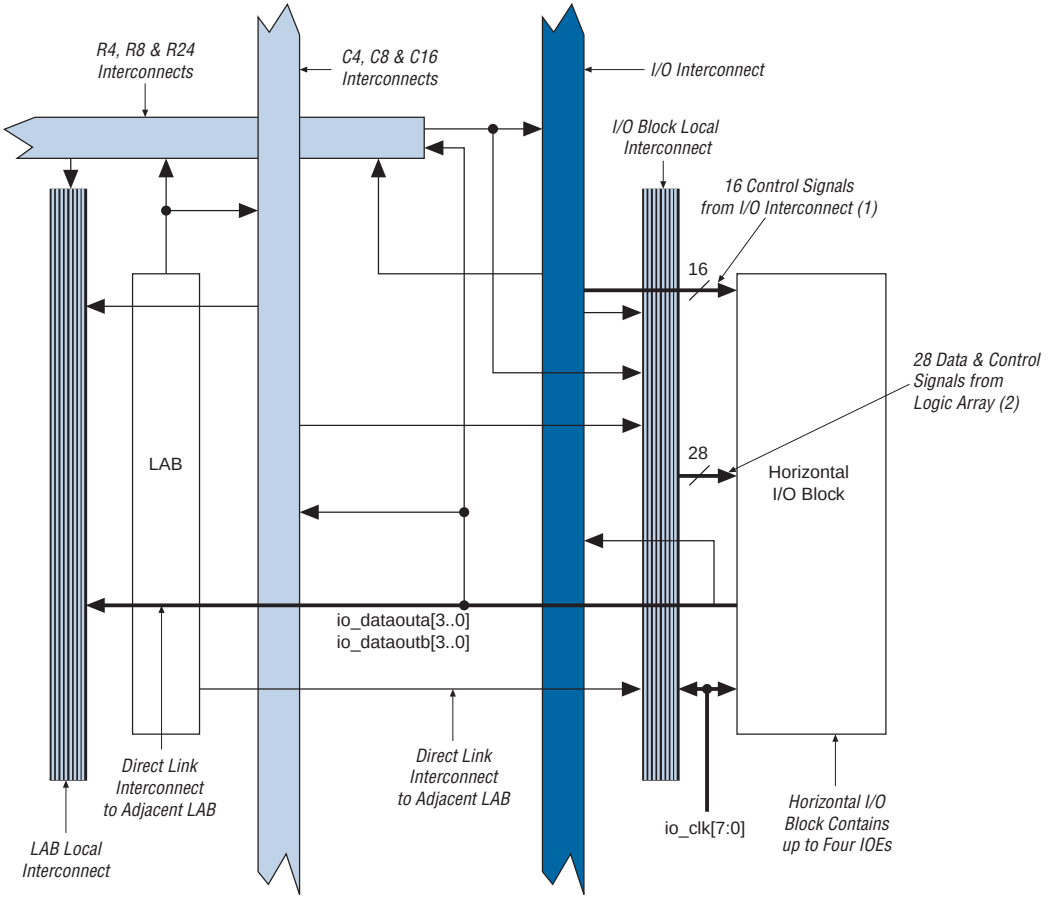
Table 2–21. Output Clock Delay for Enhanced PLLs

Normal or Zero Delay Buffer Mode	External Feedback Mode
$\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_e$ $\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$ $\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$	$\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m - \Delta t_e$ *(1)* $\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$ $\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$

Note to Table 2–21:

(1) Δt_e removes delay from outputs in external feedback mode.

Figure 2–60. Row I/O Block Connection to the Interconnect

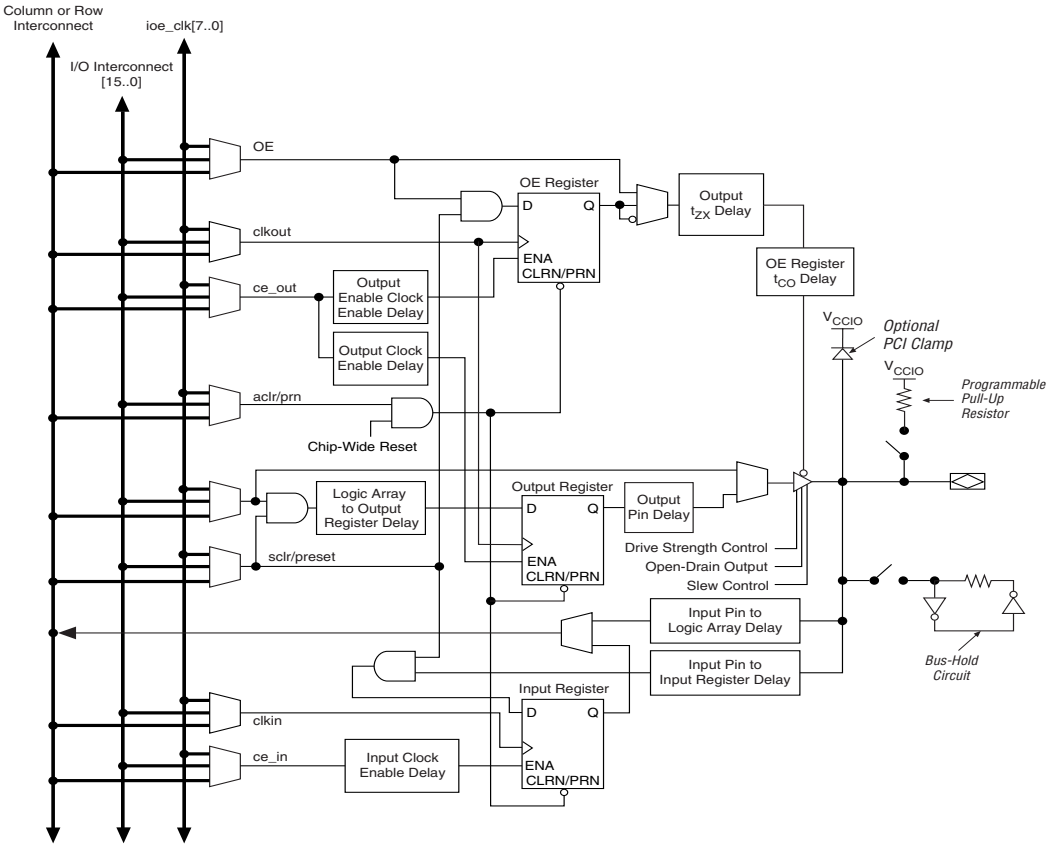


Notes to Figure 2–60:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_clk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 28 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_coe[3..0]`, four input clock enables `io_cce_in[3..0]`, four output clock enables `io_cce_out[3..0]`, four clocks `io_cclk[3..0]`, and four clear signals `io_cclr[3..0]`.

Figure 2–64. Stratix IOE in Bidirectional I/O Configuration Note (1)



Note to Figure 2–64:
(1) All input signals to the IOE can be inverted at the IOE.

The Stratix device IOE includes programmable delays that can be activated to ensure zero hold times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 2 of 2) Note (1)

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S25	672-pin FineLine BGA 672-pin BGA	Transmitter (2)	56	624 (4)	14	14	14	14
				624 (3)	28	28	28	28
		Receiver	58	624 (4)	14	15	15	14
				624 (3)	29	29	29	29
	780-pin FineLine BGA	Transmitter (2)	70	840 (4)	18	17	17	18
				840 (3)	35	35	35	35
		Receiver	66	840 (4)	17	16	16	17
				840 (3)	33	33	33	33
	1,020-pin FineLine BGA	Transmitter (2)	78	840 (4)	19	20	20	19
				840 (3)	39	39	39	39
		Receiver	78	840 (4)	19	20	20	19
				840 (3)	39	39	39	39

Notes to Table 2–37:

(1) The first row for each transmitter or receiver reports the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP1S10 device, PLL 1 can drive a maximum of five channels at 840 Mbps or a maximum of 10 channels at 840 Mbps. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

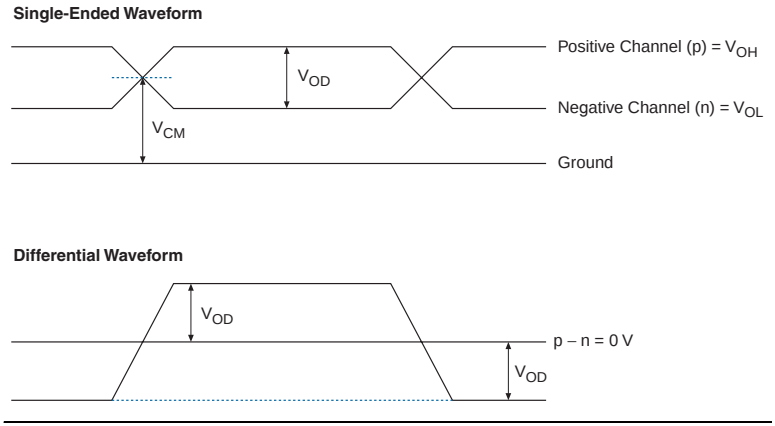
(2) The number of channels listed includes the transmitter clock output (`tx_outclock`) channel. If the design requires a DDR clock, it can use an extra data channel.

(3) These channels span across two I/O banks per side of the device. When a center PLL clocks channels in the opposite bank on the same side of the device it is called cross-bank PLL support. Both center PLLs can clock cross-bank channels simultaneously if, for example, PLL_1 is clocking all receiver channels and PLL_2 is clocking all transmitter channels. You cannot have two adjacent PLLs simultaneously clocking cross-bank receiver channels or two adjacent PLLs simultaneously clocking transmitter channels. Cross-bank allows for all receiver channels on one side of the device to be clocked on one clock while all transmitter channels on the device are clocked on the other center PLL. Crossbank PLLs are supported at full-speed, 840 Mbps. For wire-bond devices, the full-speed is 624 Mbps.

(4) These values show the channels available for each PLL without crossing another bank.

When you span two I/O banks using cross-bank support, you can route only two load enable signals total between the PLLs. When you enable `rx_data_align`, you use both `rxloadena` and `txloadena` of a PLL. That leaves no `loadena` for the second PLL.

Figure 4–2. Transmitter Output Waveforms for Differential I/O Standards



Tables 4–10 through 4–33 recommend operating conditions, DC operating conditions, and capacitance for 1.5-V Stratix devices.

Table 4–10. 3.3-V LVDS I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} *(6)*	Input differential voltage swing (single-ended)	0.1 V ≤V_{CM} < 1.1 V *W* = 1 through 10	300		1,000	mV
		1.1 V ≤V_{CM} ≤1.6 V *W* = 1	200		1,000	mV
		1.1 V ≤V_{CM} ≤1.6 V *W* = 2 through10	100		1,000	mV
		1.6 V < V_{CM} ≤1.8 V *W* = 1 through 10	300		1,000	mV

Table 4–20. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.18		3.0	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.35			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(3)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(3)*			V_{TT} – 0.57	V

Table 4–21. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.35			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(3)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(3)*			V_{TT} – 0.76	V

Table 4–22. SSTL-3 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.2	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.4			V

Table 4–52 shows the external I/O timing parameters when using fast regional clock networks.

Table 4–52. Stratix Fast Regional Clock External I/O Timing Parameters Notes (1), (2)

Symbol	Parameter
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with fast regional clock fed by FCLK pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with fast regional clock fed by FCLK pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with fast regional clock fed by FCLK pin
t_{XZ}	Synchronous IOE output enable register to output pin disable delay using fast regional clock fed by FCLK pin
t_{ZX}	Synchronous IOE output enable register to output pin enable delay using fast regional clock fed by FCLK pin

Notes to Table 4–52:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column and row IOE pins. You should use the Quartus II software to verify the external timing for any pin.

Table 4–53 shows the external I/O timing parameters when using regional clock networks.

Table 4–53. Stratix Regional Clock External I/O Timing Parameters (Part 1 of 2) Notes (1), (2)

Symbol	Parameter
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with regional clock fed by CLK pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with regional clock fed by CLK pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with regional clock fed by CLK pin
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with regional clock fed by Enhanced PLL with default phase setting
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with regional clock fed by Enhanced PLL with default phase setting
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with regional clock Enhanced PLL with default phase setting

Tables 4–67 through 4–72 show the external timing parameters on column and row pins for EP1S25 devices.

Table 4–67. EP1S25 External I/O Timing on Column Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.412		2.613		2.968		3.468		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.196	4.475	2.196	4.748	2.196	5.118	2.196	5.603	ns
t_{XZ}	2.136	4.349	2.136	4.616	2.136	4.994	2.136	5.488	ns
t_{ZX}	2.136	4.349	2.136	4.616	2.136	4.994	2.136	5.488	ns

Table 4–68. EP1S25 External I/O Timing on Column Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.535		1.661		1.877		2.125		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.739	5.396	2.739	5.746	2.739	6.262	2.739	6.946	ns
t_{XZ}	2.679	5.270	2.679	5.614	2.679	6.138	2.679	6.831	ns
t_{ZX}	2.679	5.270	2.679	5.614	2.679	6.138	2.679	6.831	ns
$t_{INSUPLL}$	0.934		0.980		1.092		1.231		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.316	2.733	1.316	2.839	1.316	2.921	1.316	3.110	ns
t^{XZPLL}	1.256	2.607	1.256	2.707	1.256	2.797	1.256	2.995	ns
t_{ZXPLL}	1.256	2.607	1.256	2.707	1.256	2.797	1.256	2.995	ns

Tables 4–79 through 4–84 show the external timing parameters on column and row pins for EP1S40 devices.

Table 4–79. EP1S40 External I/O Timing on Column Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.696		2.907		3.290		2.899		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.506	5.015	2.506	5.348	2.506	5.809	2.698	7.286	ns
t_{XZ}	2.446	4.889	2.446	5.216	2.446	5.685	2.638	7.171	ns
t_{ZX}	2.446	4.889	2.446	5.216	2.446	5.685	2.638	7.171	ns

Table 4–80. EP1S40 External I/O Timing on Column Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.413		2.581		2.914		2.938		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.668	5.254	2.668	5.628	2.668	6.132	2.869	7.307	ns
t_{XZ}	2.608	5.128	2.608	5.496	2.608	6.008	2.809	7.192	ns
t_{ZX}	2.608	5.128	2.608	5.496	2.608	6.008	2.809	7.192	ns
$t_{INSUPLL}$	1.385		1.376		1.609		1.837		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.117	2.382	1.117	2.552	1.117	2.504	1.117	2.542	ns
t_{XZPLL}	1.057	2.256	1,057	2.420	1.057	2.380	1.057	2.427	ns
t_{ZXPLL}	1.057	2.256	1,057	2.420	1.057	2.380	1.057	2.427	ns

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 4 of 4) Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{DUTY}	LVDS (J = 2 through 10)	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (J =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100			100	µs

Notes to Table 4–125:

(1) When J = 4, 7, 8, and 10, the SERDES block is used.

(2) When J = 2 or J = 1, the SERDES is bypassed.

Table 4–128. Enhanced PLL Specifications for -6 Speed Grades (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SCANCLK}$	scanclk frequency *(5)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(7)* *(11)*	*(9)*		100	µs
t_{LOCK}	Time required to lock from end of device configuration *(11)*	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		800 *(8)*	MHz
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	30		150	kHz
% spread	Percentage spread for spread spectrum frequency *(10)*	0.4	0.5	0.6	%
t_{ARESET}	Minimum pulse width on areset signal	10			ns

Table 4–129. Enhanced PLL Specifications for -7 Speed Grade (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	3 *(1)*, *(2)*		565	MHz
f_{INPFD}	Input frequency to PFD	3		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			±200 *(3)*	ps
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(3)*	ps
t_{FCOMP}	External feedback clock compensation time *(4)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		420	MHz
f_{OUT_EXT}	Output frequency for external clock *(3)*	0.3		434	MHz

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