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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	473
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-BGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep1s25b672c7">https://www.e-xfl.com/product-detail/intel/ep1s25b672c7</a>





# Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction

Revised: *July 2005*  
Part number: *S51001-3.2*

Chapter 2. Stratix Architecture

Revised: *July 2005*  
Part number: *S51002-3.2*

Chapter 3. Configuration & Testing

Revised: *July 2005*  
Part number: *S51003-1.3*

Chapter 4. DC & Switching Characteristics

Revised: *January 2006*  
Part number: *S51004-3.4*

Chapter 5. Reference & Ordering Information

Revised: *September 2004*  
Part number: *S51005-2.1*

asynchronous load, and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Stratix devices provide a chip-wide reset pin (DEV\_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

## MultiTrack Interconnect

In the Stratix architecture, connections between LEs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory within the same row. These row resources include:

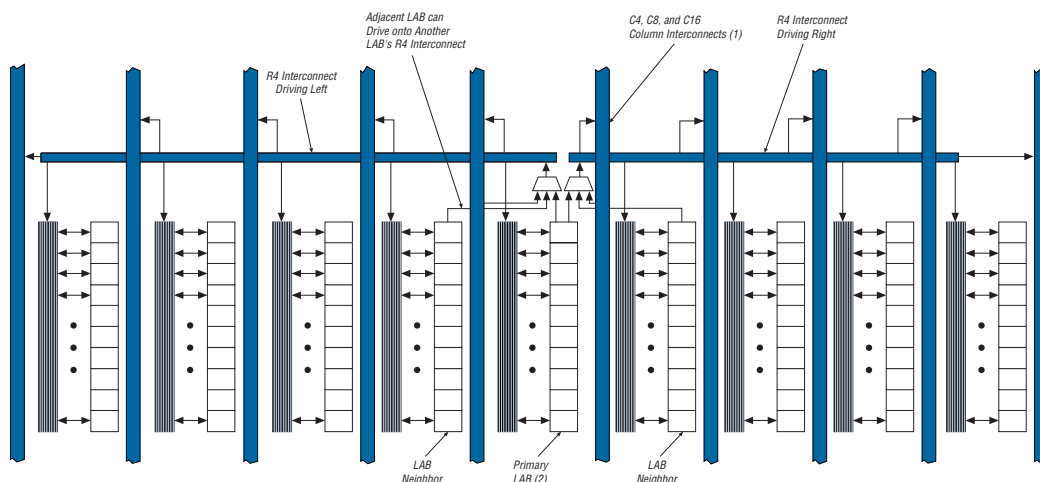
- Direct link interconnects between LABs and adjacent blocks.
- R4 interconnects traversing four blocks to the right or left.
- R8 interconnects traversing eight blocks to the right or left.
- R24 row interconnects for high-speed access across the length of the device.

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. Only one side of a M-RAM block interfaces with direct link and row interconnects. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast

row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–9 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and horizontal IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

**Figure 2–9. R4 Interconnect Connections**



**Notes to Figure 2–9:**

- (1) C4 interconnects can drive R4 interconnects.
- (2) This pattern is repeated for every LAB in the LAB row.

The R8 interconnects span eight LABs, M512 or M4K RAM blocks, or DSP blocks to the right or left from a source LAB. These resources are used for fast row connections in an eight-LAB region. Every LAB has its own set of R8 interconnects to drive either left or right. R8 interconnect connections between LABs in a row are similar to the R4 connections shown in Figure 2–9, with the exception that they connect to eight LABs to the right or left, not four. Like R4 interconnects, R8 interconnects can drive and be driven by all types of architecture blocks. R8 interconnects

### *M-RAM Block*

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO RAM

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed. The memory address and output width can be configured as  $64\text{K} \times 8$  (or  $64\text{K} \times 9$  bits),  $32\text{K} \times 16$  (or  $32\text{K} \times 18$  bits),  $16\text{K} \times 32$  (or  $16\text{K} \times 36$  bits),  $8\text{K} \times 64$  (or  $8\text{K} \times 72$  bits), and  $4\text{K} \times 128$  (or  $4\text{K} \times 144$  bits). The  $4\text{K} \times 128$  configuration is unavailable in true dual-port mode because there are a total of 144 data output drivers in the block. Mixed-width configurations are also possible, allowing different read and write widths. [Tables 2-8](#) and [2-9](#) summarize the possible M-RAM block configurations:

<b>Table 2-8. M-RAM Block Configurations (Simple Dual-Port)</b>					
<b>Read Port</b>	<b>Write Port</b>				
	<b><math>64\text{K} \times 9</math></b>	<b><math>32\text{K} \times 18</math></b>	<b><math>16\text{K} \times 36</math></b>	<b><math>8\text{K} \times 72</math></b>	<b><math>4\text{K} \times 144</math></b>
$64\text{K} \times 9$	✓	✓	✓	✓	
$32\text{K} \times 18$	✓	✓	✓	✓	
$16\text{K} \times 36$	✓	✓	✓	✓	
$8\text{K} \times 72$	✓	✓	✓	✓	
$4\text{K} \times 144$					✓

clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in [Table 2–17](#).

<b>Table 2–17. DSP Block Signal Sources &amp; Destinations</b>			
<b>LAB Row at Interface</b>	<b>Control Signals Generated</b>	<b>Data Inputs</b>	<b>Data Outputs</b>
1	signa	A1 [17..0]	OA [17..0]
2	aclr0 accum_sload0	B1 [17..0]	OB [17..0]
3	addnsb1 clock0 ena0	A2 [17..0]	OC [17..0]
4	aclr1 clock1 ena1	B2 [17..0]	OD [17..0]
5	aclr2 clock2 ena2	A3 [17..0]	OE [17..0]
6	sign_b clock3 ena3	B3 [17..0]	OF [17..0]
7	clear3 accum_sload1	A4 [17..0]	OG [17..0]
8	addnsb3	B4 [17..0]	OH [17..0]

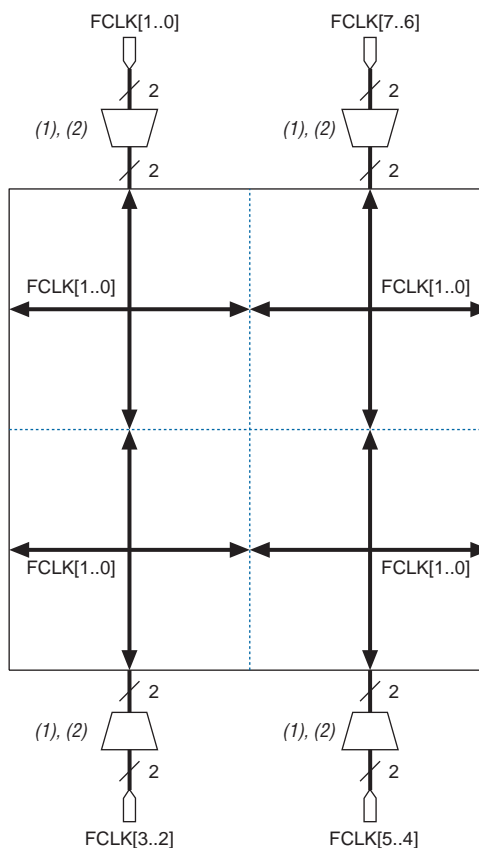
## PLLs & Clock Networks

Stratix devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

### Global & Hierarchical Clocking

Stratix devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), and 8 dedicated fast regional clock networks (for EP1S10, EP1S20, and EP1S25 devices), and 16 dedicated fast regional clock networks (for EP1S30 EP1S40, and EP1S60, and EP1S80 devices). These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within Stratix devices.

**Figure 2–44. EP1S25, EP1S20 & EP1S10 Device Fast Clock Pin Connections to Fast Regional Clocks**



**Notes to Figure 2–44:**

- (1) This is a set of two multiplexers.
- (2) In addition to the FCLK pin inputs, there is also an input from the I/O interconnect.



During switchover, the PLL VCO continues to run and will either slow down or speed up, generating frequency drift on the PLL outputs. The clock switchover transitions without any glitches. After the switch, there is a finite resynchronization period to lock onto new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock relates to the PLL configuration and may be adjusted by using the programmable bandwidth feature of the PLL. The specification for the maximum time to relock is 100  $\mu$ s.

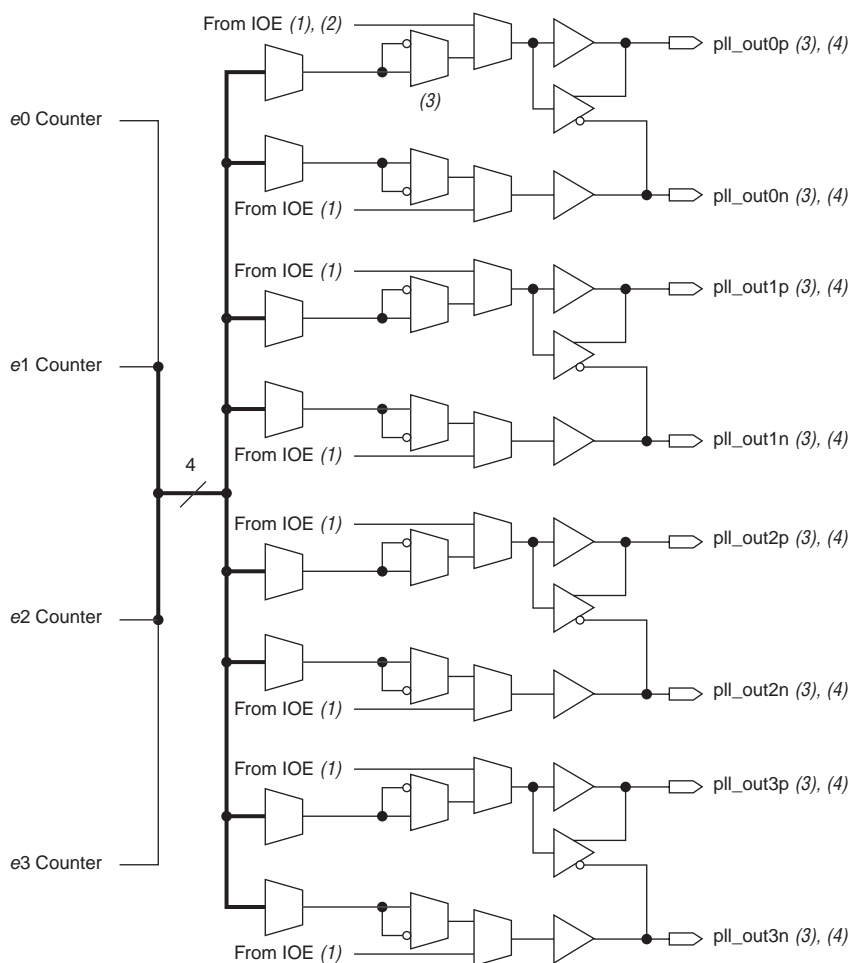


For more information on clock switchover, see *AN 313, Implementing Clock Switchover in Stratix & Stratix GX Devices*.

### *PLL Reconfiguration*

The PLL reconfiguration feature enables system logic to change Stratix device enhanced PLL counters and delay elements without reloading a Programmer Object File (.pof). This provides considerable flexibility for frequency synthesis, allowing real-time PLL frequency and output clock delay variation. You can sweep the PLL output frequencies and clock delay in prototype environments. The PLL reconfiguration feature can also dynamically or intelligently control system clock speeds or  $t_{CO}$  delays in end systems.

Clock delay elements at each PLL output port implement variable delay. [Figure 2-54](#) shows a diagram of the overall dynamic PLL control feature for the counters and the clock delay elements. The configuration time is less than 20  $\mu$ s for the enhanced PLL using a input shift clock rate of 22 MHz. The charge pump, loop filter components, and phase shifting using VCO phase taps cannot be dynamically adjusted.

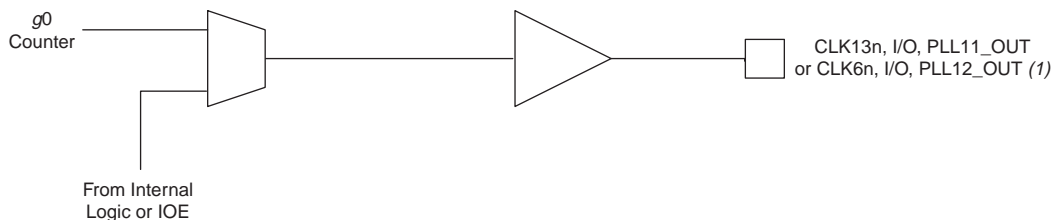
**Figure 2–55. External Clock Outputs for PLLs 5 & 6****Notes to Figure 2–55:**

- (1) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with IOE outputs.
- (2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.
- (3) EP1S10, EP1S20, and EP1S25 devices in 672-pin BGA and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., pll\_out0p, pll\_out0n, pll\_out1p, and pll\_out1n).
- (4) Differential SSTL and HSTL outputs are implemented using two single-ended output buffers, which are programmed to have opposite polarity.

**Table 2–20. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2)**

I/O Standard	Input			Output
	INCLK	FBIN	PLENABLE	EXTCLK
1.5-V HSTL Class II	✓	✓		✓
1.8-V HSTL Class I	✓	✓		✓
1.8-V HSTL Class II	✓	✓		✓
SSTL-18 Class I	✓	✓		✓
SSTL-18 Class II	✓	✓		✓
SSTL-2 Class I	✓	✓		✓
SSTL-2 Class II	✓	✓		✓
SSTL-3 Class I	✓	✓		✓
SSTL-3 Class II	✓	✓		✓
AGP (1× and 2×)	✓	✓		✓
CTT	✓	✓		✓

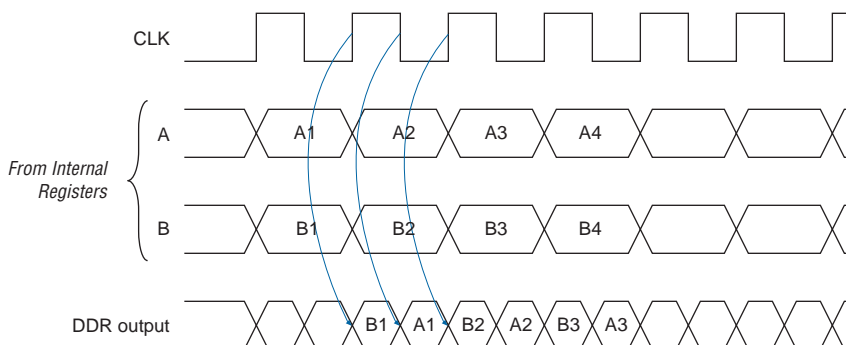
Enhanced PLLs 11 and 12 support one single-ended output each (see [Figure 2–56](#)). These outputs do not have their own VCC and GND signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

**Figure 2–56. External Clock Outputs for Enhanced PLLs 11 & 12**

**Note to Figure 2–56:**

(1) For PLL 11, this pin is CLK13n; for PLL 12 this pin is CLK7n.

Stratix devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

**Figure 2–68. Output Timing Diagram in DDR Mode**

The Stratix IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

## External RAM Interfacing

Stratix devices support DDR SDRAM at up to 200 MHz (400-Mbps data rate) through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces up to 200 MHz. Stratix devices also provide preliminary support for reduced latency DRAM II (RLDRAM II) at rates up to 200 MHz through the dedicated phase-shift circuitry.



In addition to the required signals for external memory interfacing, Stratix devices offer the optional clock enable signal. By default the Quartus II software sets the clock enable signal high, which tells the output register to update with new values. The output registers hold their own values if the design sets the clock enable signal low. See [Figure 2–64](#).



To find out more about the DDR SDRAM specification, see the JEDEC web site ([www.jedec.org](http://www.jedec.org)). For information on memory controller megafunctions for Stratix devices, see the Altera web site ([www.altera.com](http://www.altera.com)). See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices* for more information on DDR SDRAM interface in Stratix. Also see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices* and *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

### Bus Hold

Each Stratix device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Table 2–29 shows bus hold support for different pin types.

<i>Table 2–29. Bus Hold Support</i>	
Pin Type	Bus Hold
I/O pins	✓
CLK [15 . . 0]	
CLK [0, 1, 2, 3, 8, 9, 10, 11]	
FCLK	✓
FPLL [7 . . 10] CLK	

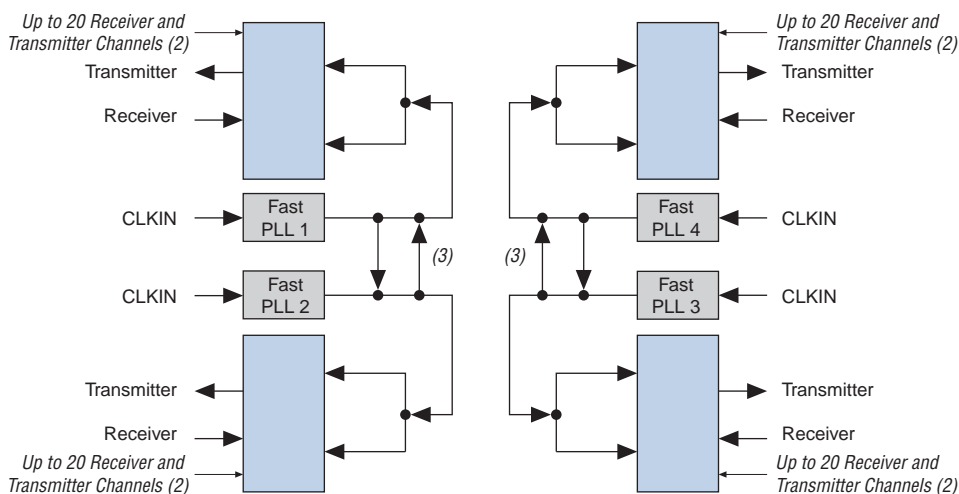
The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than  $V_{CCIO}$  to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when using open-drain outputs with the GTL+ I/O standard or when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance ( $R_{BH}$ ) of approximately 7 k $\Omega$  to weakly pull the signal level to the last-driven state. See the *DC & Switching Characteristics* chapter of the *Stratix Device Handbook, Volume 1* for the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each  $V_{CCIO}$  voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

The Quartus II MegaWizard® Plug-In Manager only allows the implementation of up to 20 receiver or 20 transmitter channels for each fast PLL. These channels operate at up to 840 Mbps. The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per LAB row. [Figure 2-74](#) shows the fast PLL and channel layout in EP1S10, EP1S20, and EP1S25 devices. [Figure 2-75](#) shows the fast PLL and channel layout in the EP1S30 to EP1S80 devices.

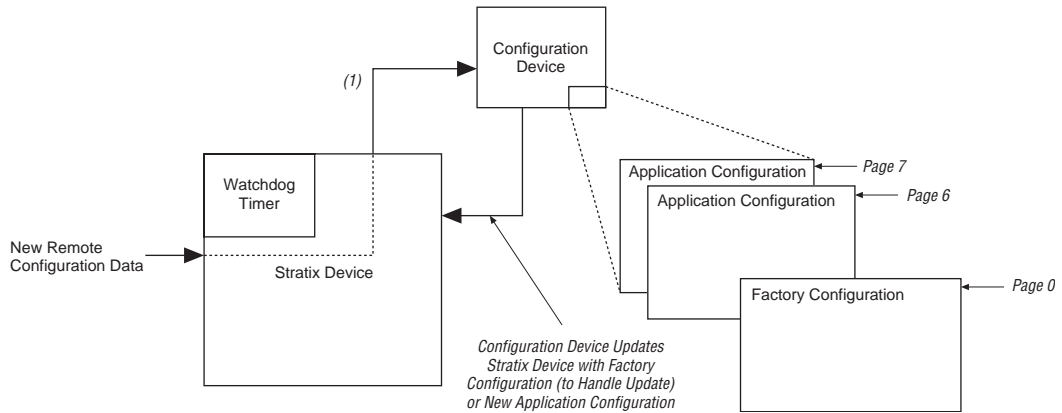
**Figure 2-74. Fast PLL & Channel Layout in the EP1S10, EP1S20 or EP1S25 Devices** *Note (1)*



**Notes to Figure 2-74:**

- (1) Wire-bond packages support up to 624 Mbps.
- (2) See [Table 2-41](#) for the number of channels each device supports.
- (3) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant, those clocked channels support up to 840 Mbps for “high” speed channels and 462 Mbps for “low” speed channels, as labeled in the device pin-outs at [www.altera.com](http://www.altera.com).

**Figure 3–2. Stratix Device Remote Update**



**Note to Figure 3–2:**

- (1) When the Stratix device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

**Table 4–18. SSTL-18 Class I Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	Output supply voltage		1.65	1.8	1.95	V
$V_{REF}$	Reference voltage		0.8	0.9	1.0	V
$V_{TT}$	Termination voltage		$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
$V_{IH(DC)}$	High-level DC input voltage		$V_{REF} + 0.125$			V
$V_{IL(DC)}$	Low-level DC input voltage				$V_{REF} - 0.125$	V
$V_{IH(AC)}$	High-level AC input voltage		$V_{REF} + 0.275$			V
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.275$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -6.7 \text{ mA}$ (3)	$V_{TT} + 0.475$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 6.7 \text{ mA}$ (3)			$V_{TT} - 0.475$	V

**Table 4–19. SSTL-18 Class II Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{CCIO}$	Output supply voltage		1.65	1.8	1.95	V
$V_{REF}$	Reference voltage		0.8	0.9	1.0	V
$V_{TT}$	Termination voltage		$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
$V_{IH(DC)}$	High-level DC input voltage		$V_{REF} + 0.125$			V
$V_{IL(DC)}$	Low-level DC input voltage				$V_{REF} - 0.125$	V
$V_{IH(AC)}$	High-level AC input voltage		$V_{REF} + 0.275$			V
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.275$	V
$V_{OH}$	High-level output voltage	$I_{OH} = -13.4 \text{ mA}$ (3)	$V_{TT} + 0.630$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 13.4 \text{ mA}$ (3)			$V_{TT} - 0.630$	V



Tables 4–73 through 4–78 show the external timing parameters on column and row pins for EP1S30 devices.

**Table 4–73. EP1S30 External I/O Timing on Column Pins Using Fast Regional Clock Networks**

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.502		2.680		3.062		3.591		ns
$t_{\text{INH}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCO}}$	2.473	4.965	2.473	5.329	2.473	5.784	2.473	6.392	ns
$t_{\text{XZ}}$	2.413	4.839	2.413	5.197	2.413	5.660	2.413	6.277	ns
$t_{\text{ZX}}$	2.413	4.839	2.413	5.197	2.413	5.660	2.413	6.277	ns

**Table 4–74. EP1S30 External I/O Timing on Column Pins Using Regional Clock Networks**

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.286		2.426		2.769		3.249		ns
$t_{\text{INH}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCO}}$	2.641	5.225	2.641	5.629	2.641	6.130	2.641	6.796	ns
$t_{\text{XZ}}$	2.581	5.099	2.581	5.497	2.581	6.006	2.581	6.681	ns
$t_{\text{ZX}}$	2.581	5.099	2.581	5.497	2.581	6.006	2.581	6.681	ns
$t_{\text{INSUPLL}}$	1.200		1.185		1.344		1.662		ns
$t_{\text{INHPLL}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCOPLL}}$	1.108	2.367	1.108	2.534	1.108	2.569	1.108	2.517	ns
$t_{\text{XZPLL}}$	1.048	2.241	1.048	2.402	1.048	2.445	1.048	2.402	ns
$t_{\text{ZXPLL}}$	1.048	2.241	1.048	2.402	1.048	2.445	1.048	2.402	ns

**Table 4–75. EP1S30 External I/O Timing on Column Pins Using Global Clock Networks (Part 1 of 2)**

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	1.935		2.029		2.310		2.709		ns
$t_{\text{INH}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCO}}$	2.814	5.532	2.814	5.980	2.814	6.536	2.814	7.274	ns

**Table 4–77. EP1S30 External I/O Timing on Row Pins Using Regional Clock Networks**

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	2.322		2.467		2.828		3.342		ns
$t_{\text{INH}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCO}}$	2.731	5.408	2.731	5.843	2.731	6.360	2.731	7.036	ns
$t_{\text{XZ}}$	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
$t_{\text{ZX}}$	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
$t_{\text{INSUPLL}}$	1.291		1.283		1.469		1.832		ns
$t_{\text{INHPLL}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCOPLL}}$	1.192	2.539	1.192	2.737	1.192	2.786	1.192	2.742	ns
$t_{\text{XZPLL}}$	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns
$t_{\text{ZXPLL}}$	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns

**Table 4–78. EP1S30 External I/O Timing on Row Pins Using Global Clock Networks**

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$	1.995		2.089		2.398		2.830		ns
$t_{\text{INH}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCO}}$	2.917	5.735	2.917	6.221	2.917	6.790	2.917	7.548	ns
$t_{\text{XZ}}$	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
$t_{\text{ZX}}$	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
$t_{\text{INSUPLL}}$	1.337		1.312		1.508		1.902		ns
$t_{\text{INHPLL}}$	0.000		0.000		0.000		0.000		ns
$t_{\text{OUTCOPLL}}$	1.164	2.493	1.164	2.708	1.164	2.747	1.164	2.672	ns
$t_{\text{XZPLL}}$	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns
$t_{\text{ZXPLL}}$	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns

Tables 4–105 through 4–108 show the output adder delays associated with column and row I/O pins for both fast and slow slew rates. If an I/O standard is selected other than 3.3-V LVTTTL 4mA or LVCMOS 2 mA with a fast slew rate, add the selected delay to the external  $t_{OUTCO}$ ,  $t_{OUTCOPLL}$ ,  $t_{XZ}$ ,  $t_{ZX}$ ,  $t_{XZPLL}$ , and  $t_{ZXPLL}$  I/O parameters shown in Table 4–55 on page 4–36 through Table 4–96 on page 4–56.

**Table 4–105. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)**

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,895		1,990		1,990		1,990	ps
	4 mA		956		1,004		1,004		1,004	ps
	8 mA		189		198		198		198	ps
	12 mA		0		0		0		0	ps
	24 mA		–157		–165		–165		–165	ps
3.3-V LVTTTL	4 mA		1,895		1,990		1,990		1,990	ps
	8 mA		1,347		1,414		1,414		1,414	ps
	12 mA		636		668		668		668	ps
	16 mA		561		589		589		589	ps
	24 mA		0		0		0		0	ps
2.5-V LVTTTL	2 mA		2,517		2,643		2,643		2,643	ps
	8 mA		834		875		875		875	ps
	12 mA		504		529		529		529	ps
	16 mA		194		203		203		203	ps
1.8-V LVTTTL	2 mA		1,304		1,369		1,369		1,369	ps
	8 mA		960		1,008		1,008		1,008	ps
	12 mA		960		1,008		1,008		1,008	ps
1.5-V LVTTTL	2 mA		6,680		7,014		7,014		7,014	ps
	4 mA		3,275		3,439		3,439		3,439	ps
	8 mA		1,589		1,668		1,668		1,668	ps
GTL			16		17		17		17	ps
GTL+			9		9		9		9	ps
3.3-V PCI			50		52		52		52	ps
3.3-V PCI-X 1.0			50		52		52		52	ps
Compact PCI			50		52		52		52	ps
AGP 1×			50		52		52		52	ps
AGP 2×			1,895		1,990		1,990		1,990	ps

**Table 4–116. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Flip-Chip Packages**

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	422	390	390	MHz
2.5 V	422	422	390	390	MHz
1.8 V	422	422	390	390	MHz
1.5 V	422	422	390	390	MHz
LVC MOS	422	422	390	390	MHz
GTL+	300	250	200	200	MHz
SSTL-3 Class I	400	350	300	300	MHz
SSTL-3 Class II	400	350	300	300	MHz
SSTL-2 Class I	400	350	300	300	MHz
SSTL-2 Class II	400	350	300	300	MHz
SSTL-18 Class I	400	350	300	300	MHz
SSTL-18 Class II	400	350	300	300	MHz
1.5-V HSTL Class I	400	350	300	300	MHz
1.8-V HSTL Class I	400	350	300	300	MHz
CTT	300	250	200	200	MHz
Differential 1.5-V HSTL C1	400	350	300	300	MHz
LVPECL (1)	645	645	640	640	MHz
PCML (1)	300	275	275	275	MHz
LVDS (1)	645	645	640	640	MHz
HyperTransport technology (1)	500	500	450	450	MHz

**Table 4–117. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages (Part 1 of 2)**

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz
LVC MOS	422	390	390	MHz
GTL	250	200	200	MHz

**Table 4–126. High-Speed I/O Specifications for Wire-Bond Packages (Part 2 of 2)**

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SW	PCML (J = 4, 7, 8, 10) only	800			800			800			ps
	PCML (J = 2) only	1,200			1,200			1,200			ps
	PCML (J = 1) only	1,700			1,700			1,700			ps
	LVDS and LVPECL (J = 1) only	550			550			550			ps
	LVDS, LVPECL, HyperTransport technology (J = 2 through 10) only	500			500			500			ps
Input jitter tolerance (peak-to-peak)	All			250			250			250	ps
Output jitter (peak-to-peak)	All			200			200			200	ps
Output $t_{RISE}$	LVDS	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	120	170	200	120	170	200	120	170	200	ps
	LVPECL	100	135	150	100	135	150	100	135	150	ps
	PCML	80	110	135	80	110	135	80	110	135	ps
Output $t_{FALL}$	LVDS	80	110	120	80	110	120	80	110	120	ps
	HyperTransport	110	170	200	110	170	200	110	170	200	ps
	LVPECL	100	135	160	100	135	160	100	135	160	ps
	PCML	110	145	175	110	145	175	110	145	175	ps
$t_{DUTY}$	LVDS (J = 2 through 10) only	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (J = 1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	%
$t_{LOCK}$	All			100			100			100	$\mu$ s