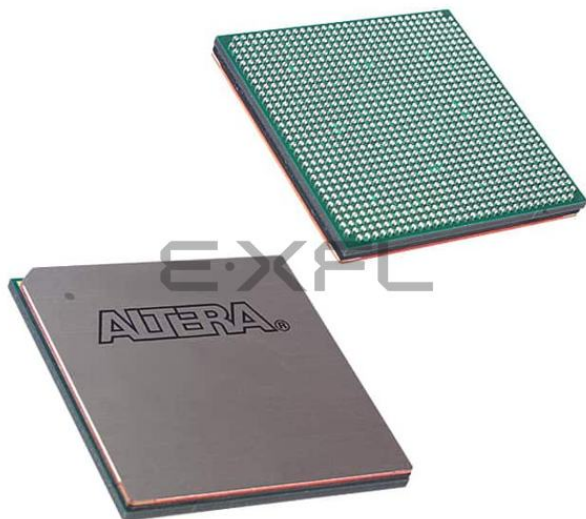




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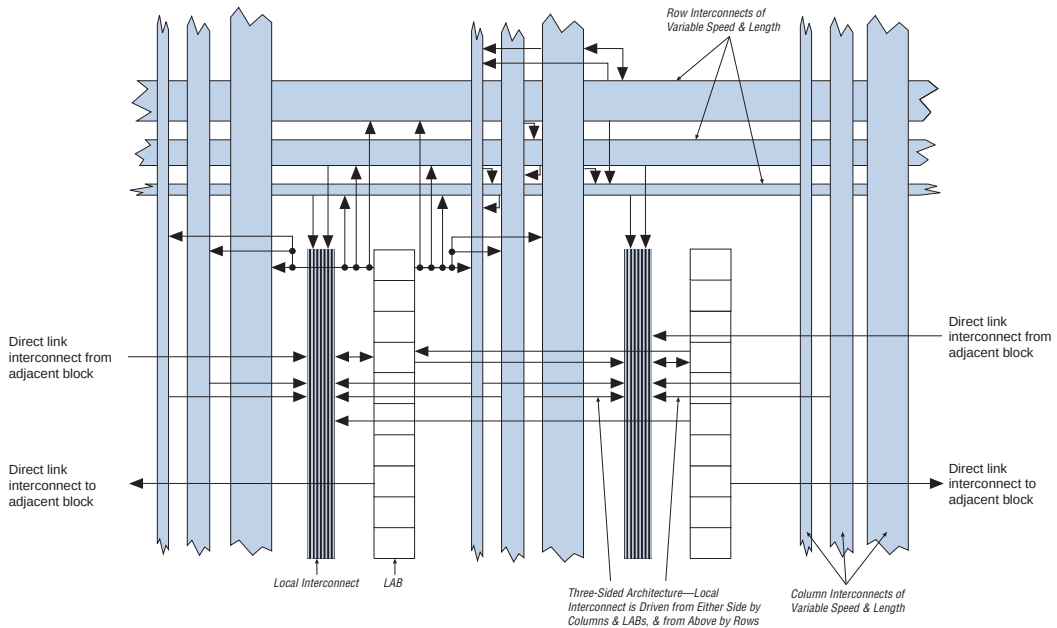
Details

Product Status	Obsolete
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	706
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s25f1020c6nga

Features

The Stratix family offers the following features:

- 10,570 to 79,040 LEs; see [Table 1–1](#)
- Up to 7,427,520 RAM bits (928,440 bytes) available without reducing logic resources
- TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (faster than 300 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 22 clocking resources per device region
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support on up to 116 channels with up to 80 channels optimized for 840 megabits per second (Mbps)
- Support for high-speed networking and communications bus standards including RapidIO, UTOPIA IV, CSIX, HyperTransport™ technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
- Differential on-chip termination support for LVDS
- Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
- Support for 66-MHz PCI (64 and 32 bit) in -6 and faster speed-grade devices, support for 33-MHz PCI (64 and 32 bit) in -8 and faster speed-grade devices
- Support for 133-MHz PCI-X 1.0 in -5 speed-grade devices
- Support for 100-MHz PCI-X 1.0 in -6 and faster speed-grade devices
- Support for 66-MHz PCI-X 1.0 in -7 speed-grade devices
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions
- Support for remote configuration updates

Figure 2–2. Stratix LAB Structure

LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects.

Figure 2–3 shows the direct link connection.

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2-7 summarizes the byte selection.

Table 2-7. Byte Enable for M4K Blocks <i>Notes (1), (2)</i>		
byteena[3..0]	datain ×18	datain ×36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Notes to Table 2-7:

- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (renwe, address, byte enable, datain, and output registers). Only the output register can be bypassed. The eight labclk signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the clock_a, clock_b, renwe_a, renwe_b, clr_a, clr_b, clocken_a, and clocken_b signals, as shown in Figure 2-17.

The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2-18 shows the M4K RAM block to logic array interface.

Table 2–11. M-RAM Combined Byte Selection for $\times 144$ Mode *Notes (1), (2)*

byteena[15..0]	datain $\times 144$
[0] = 1	[8..0]
[1] = 1	[17..9]
[2] = 1	[26..18]
[3] = 1	[35..27]
[4] = 1	[44..36]
[5] = 1	[53..45]
[6] = 1	[62..54]
[7] = 1	[71..63]
[8] = 1	[80..72]
[9] = 1	[89..81]
[10] = 1	[98..90]
[11] = 1	[107..99]
[12] = 1	[116..108]
[13] = 1	[125..117]
[14] = 1	[134..126]
[15] = 1	[143..135]

Notes to Tables 2–10 and 2–11:

- (1) Any combination of byte enables is possible.
- (2) Byte enables can be used in the same manner with 8-bit words, i.e., in $\times 16$, $\times 32$, $\times 64$, and $\times 128$ modes.

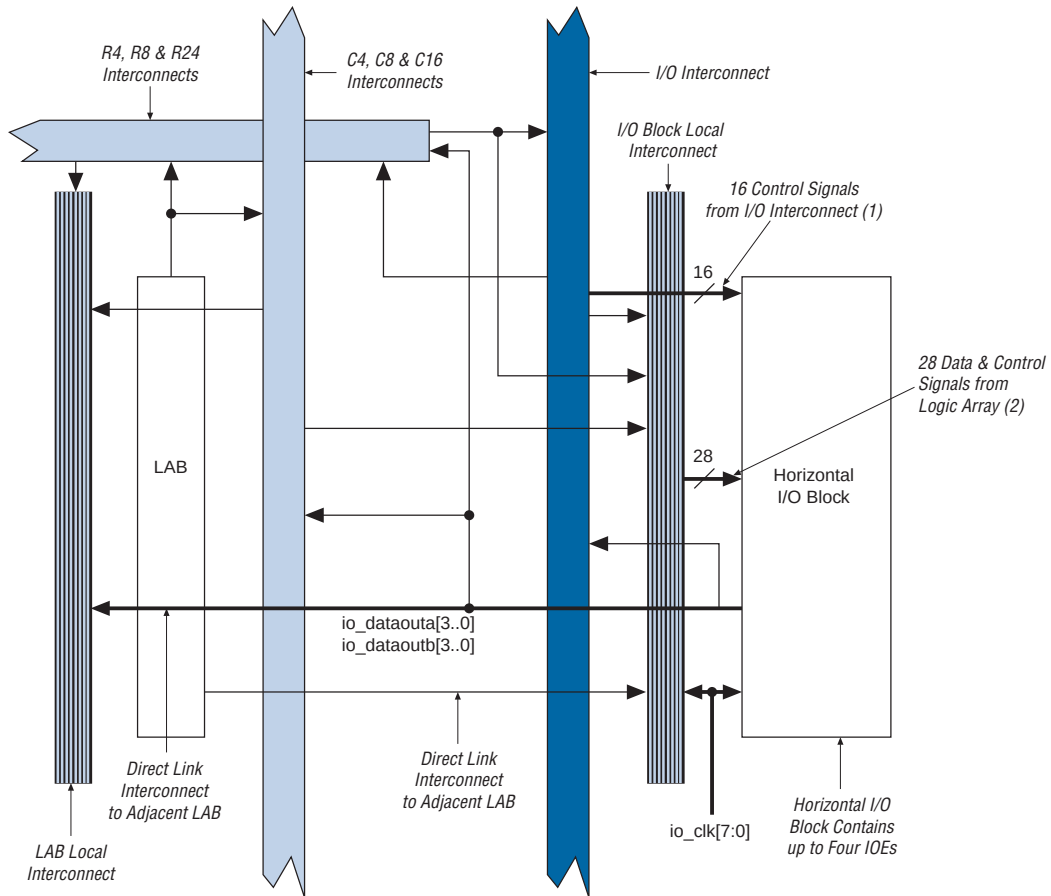
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. All input registers—renwe, datain, address, and byte enable registers—are clocked together from either of the two clocks feeding the block. The output register can be bypassed. The eight labclk signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. LEs can also control the clock_a, clock_b, renwe_a, renwe_b, clr_a, clr_b, clocken_a, and clocken_b signals as shown in Figure 2–19.

blocks facing to the left, and another 10 possible from the right adjacent LABs for M-RAM blocks facing to the right. For column interfacing, every M-RAM column unit connects to the right and left column lines, allowing each M-RAM column unit to communicate directly with three columns of LABs. [Figures 2–21](#) through [2–23](#) show the interface between the M-RAM block and the logic array.

Input Registers

A bank of optional input registers is located at the input of each multiplier and multiplicand inputs to the multiplier. When these registers are configured for parallel data inputs, they are driven by regular routing resources. You can use a clock signal, asynchronous clear signal, and a clock enable signal to independently control each set of A and B inputs for each multiplier in the DSP block. You select these control signals from a set of four different `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]` signals that drive the entire DSP block.

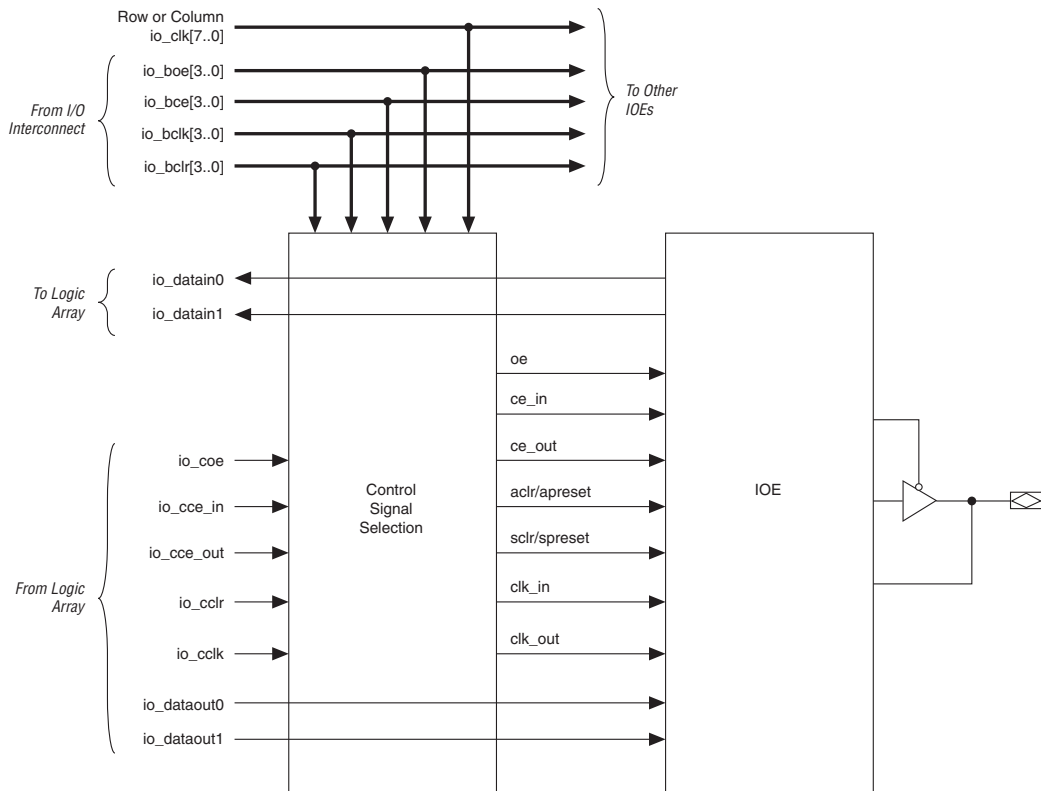
You can also configure the input registers for a shift register application. In this case, the input registers feed the multiplier and drive two dedicated shift output lines: `shiftoutA` and `shiftoutB`. The shift outputs of one multiplier block directly feed the adjacent multiplier block in the same DSP block (or the next DSP block) as shown in [Figure 2-33](#), to form a shift register chain. This chain can terminate in any block, that is, you can create any length of shift register chain up to 224 registers. You can use the input shift registers for FIR filter applications. One set of shift inputs can provide data for a filter, and the other are coefficients that are optionally loaded in serial or parallel. When implementing 9×9 - and 18×18 -bit multipliers, you do not need to implement external shift registers in LAB LEs. You implement all the filter circuitry within the DSP block and its routing resources, saving LE and general routing resources for general logic. External registers are needed for shift register inputs when using 36×36 -bit multipliers.

Figure 2–60. Row I/O Block Connection to the Interconnect**Notes to Figure 2–60:**

- (1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_clk[3..0]`, and four clear signals `io_bclr[3..0]`.
- (2) The 28 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_coe[3..0]`, four input clock enables `io_cce_in[3..0]`, four output clock enables `io_cce_out[3..0]`, four clocks `io_cclk[3..0]`, and four clear signals `io_cclr[3..0]`.

Stratix devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see “PLLs & Clock Networks” on page 2-73). Figure 2-62 illustrates the signal paths through the I/O block.

Figure 2-62. Signal Path through the I/O Block



Tables 2–25 and 2–26 show the performance specification for DDR SDRAM, RLD RAM II, QDR SRAM, QDR II SRAM, and ZBT SRAM interfaces in EP1S10 through EP1S40 devices and in EP1S60 and EP1S80 devices. The DDR SDRAM and QDR SRAM numbers in Table 2–25 have been verified with hardware characterization with third-party DDR SDRAM and QDR SRAM devices over temperature and voltage extremes.

Table 2–25. External RAM Support in EP1S10 through EP1S40 Devices

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)						
		-5 Speed Grade	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade	
		Flip-Chip	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond
DDR SDRAM (1), (2)	SSTL-2	200	167	133	133	100	100	100
DDR SDRAM - side banks (2), (3), (4)	SSTL-2	150	133	110	133	100	100	100
RLDRAM II (4)	1.8-V HSTL	200	(5)	(5)	(5)	(5)	(5)	(5)
QDR SRAM (6)	1.5-V HSTL	167	167	133	133	100	100	100
QDR II SRAM (6)	1.5-V HSTL	200	167	133	133	100	100	100
ZBT SRAM (7)	LVTTL	200	200	200	167	167	133	133

Notes to Table 2–25:

- (1) These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).
- (2) For more information on DDR SDRAM, see AN 342: *Interfacing DDR SDRAM with Stratix & Stratix GX Devices*.
- (3) DDR SDRAM is supported on the Stratix device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.
- (4) These performance specifications are preliminary.
- (5) This device does not support RLD RAM II.
- (6) For more information on QDR or QDR II SRAM, see AN 349: *QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.
- (7) For more information on ZBT SRAM, see AN 329: *ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

The only way you can use the `rx_data_align` is if one of the following is true:

- The receiver PLL is only clocking receive channels (no resources for the transmitter)
- If all channels can fit in one I/O bank

Table 2–38. EP1S30 Differential Channels *Note (1)*

Package	Transmitter/Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
780-pin FineLine BGA	Transmitter (4)	70	840	18	17	17	18	(6)	(6)	(6)	(6)
			840 (5)	35	35	35	35	(6)	(6)	(6)	(6)
	Receiver	66	840	17	16	16	17	(6)	(6)	(6)	(6)
			840 (5)	33	33	33	33	(6)	(6)	(6)	(6)
956-pin BGA	Transmitter (4)	80	840	19	20	20	19	20	20	20	20
			840 (5)	39	39	39	39	20	20	20	20
	Receiver	80	840	20	20	20	20	19	20	20	19
			840 (5)	40	40	40	40	19	20	20	19
1,020-pin FineLine BGA	Transmitter (4)	80 (2) (7)	840	19 (1)	20	20	19 (1)	20	20	20	20
			840 (5),(8)	39 (1)	39 (1)	39 (1)	39 (1)	20	20	20	20
	Receiver	80 (2) (7)	840	20	20	20	20	19 (1)	20	20	19 (1)
			840 (5),(8)	40	40	40	40	19 (1)	20	20	19 (1)

Table 2–39. EP1S40 Differential Channels (Part 1 of 2) *Note (1)*

Package	Transmitter/Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
780-pin FineLine BGA	Transmitter (4)	68	840	18	16	16	18	(6)	(6)	(6)	(6)
			840 (5)	34	34	34	34	(6)	(6)	(6)	(6)
	Receiver	66	840	17	16	16	17	(6)	(6)	(6)	(6)
			840 (5)	33	33	33	33	(6)	(6)	(6)	(6)

Table 2–40. EP1S60 Differential Channels (Part 2 of 2) Note (1)

Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
1,020-pin FineLine BGA	Transmitter (4)	80 (12) (7)	840	12 (2)	10 (4)	10 (4)	12 (2)	20	20	20	20
			840 (5), (8)	22 (6)	22 (6)	22 (6)	22 (6)	20	20	20	20
	Receiver	80 (10) (7)	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5), (8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)
1,508-pin FineLine BGA	Transmitter (4)	80 (36) (7)	840	12 (8)	10 (10)	10 (10)	12 (8)	20	20	20	20
			840 (5), (8)	22 (18)	22 (18)	22 (18)	22 (18)	20	20	20	20
	Receiver	80 (36) (7)	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5), (8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)

Table 2–41. EP1S80 Differential Channels (Part 1 of 2) Note (1)

Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
956-pin BGA	Transmitter (4)	80 (40) (7)	840	10	10	10	10	20	20	20	20
			840 (5), (8)	20	20	20	20	20	20	20	20
	Receiver	80	840	20	20	20	20	10	10	10	10
			840 (5), (8)	40	40	40	40	10	10	10	10
1,020-pin FineLine BGA	Transmitter (4)	92 (12) (7)	840	10 (2)	10 (4)	10 (4)	10 (2)	20	20	20	20
			840 (5), (8)	20 (6)	20 (6)	20 (6)	20 (6)	20	20	20	20
	Receiver	90 (10) (7)	840	20	20	20	20	10 (2)	10 (3)	10 (3)	10 (2)
			840 (5), (8)	40	40	40	40	10 (2)	10 (3)	10 (3)	10 (2)

Tables 4–61 through 4–66 show the external timing parameters on column and row pins for EP1S20 devices.

Table 4–61. EP1S20 External I/O Timing on Column Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.065		2.245		2.576		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.283	4.622	2.283	4.916	2.283	5.310	NA	NA	ns
t_{xZ}	2.223	4.496	2.223	4.784	2.223	5.186	NA	NA	ns
t_{ZX}	2.223	4.496	2.223	4.784	2.223	5.186	NA	NA	ns

Table 4–62. EP1S20 External I/O Timing on Column Pins Using Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.541		1.680		1.931		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.597	5.146	2.597	5.481	2.597	5.955	NA	NA	ns
t_{xZ}	2.537	5.020	2.537	5.349	2.537	5.831	NA	NA	ns
t_{ZX}	2.537	5.020	2.537	5.349	2.537	5.831	NA	NA	ns
t_{INSUPLL}	0.777		0.818		0.937		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
t_{OUTCOPLL}	1.296	2.690	1.296	2.801	1.296	2.876	NA	NA	ns
t_{xZPLL}	1.236	2.564	1.236	2.669	1.236	2.752	NA	NA	ns
t_{ZXPLL}	1.236	2.564	1.236	2.669	1.236	2.752	NA	NA	ns

Table 4–63. EP1S20 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.351		1.479		1.699		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.732	5.380	2.732	5.728	2.732	6.240	NA	NA	ns
t_{XZ}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
t_{ZX}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
t_{INSUPLL}	0.923		0.971		1.098		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
t_{OUTCOPLL}	1.210	2.544	1.210	2.648	1.210	2.715	NA	NA	ns
t_{XZPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns
t_{ZXPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns

Table 4–64. EP1S20 External I/O Timing on Row Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.032		2.207		2.535		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.492	5.018	2.492	5.355	2.492	5.793	NA	NA	ns
t_{XZ}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns
t_{ZX}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns

Table 4–81. EP1S40 External I/O Timing on Column Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.126		2.268		2.558		2.930		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.856	5.585	2.856	5.987	2.856	6.541	2.847	7.253	ns
t_{XZ}	2.796	5.459	2.796	5.855	2.796	6.417	2.787	7.138	ns
t_{ZX}	2.796	5.459	2.796	5.855	2.796	6.417	2.787	7.138	ns
t_{INSUPLL}	1.466		1.455		1.711		1.906		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
t_{OUTCOPLL}	1.092	2.345	1.092	2.510	1.092	2.455	1.089	2.473	ns
t_{XZPLL}	1.032	2.219	1.032	2.378	1.032	2.331	1.029	2.358	ns
t_{ZXPLL}	1.032	2.219	1.032	2.378	1.032	2.331	1.029	2.358	ns

Table 4–82. EP1S40 External I/O Timing on Row Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.472		2.685		3.083		3.056		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.631	5.258	2.631	5.625	2.631	6.105	2.745	7.324	ns
t_{XZ}	2.658	5.312	2.658	5.681	2.658	6.173	2.772	7.406	ns
t_{ZX}	2.658	5.312	2.658	5.681	2.658	6.173	2.772	7.406	ns

Table 4–101. Reporting Methodology For Maximum Timing For Single-Ended Output Pins (Part 2 of 2)
Notes (1), (2), (3)

I/O Standard	Loading and Termination							Measurement Point
	R_{UP} Ω	R_{DN} Ω	R_S Ω	R_T Ω	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS}
3.3-V SSTL-3 Class I	–	–	25	50	2.950	1.250	30	1.250
2.5-V SSTL-2 Class II	–	–	25	25	2.370	1.110	30	1.110
2.5-V SSTL-2 Class I	–	–	25	50	2.370	1.110	30	1.110
1.8-V SSTL-18 Class II	–	–	25	25	1.650	0.760	30	0.760
1.8-V SSTL-18 Class I	–	–	25	50	1.650	0.760	30	0.760
1.5-V HSTL Class II	–	–	0	25	1.400	0.700	20	0.680
1.5-V HSTL Class I	–	–	0	50	1.400	0.700	20	0.680
1.8-V HSTL Class II	–	–	0	25	1.650	0.700	20	0.880
1.8-V HSTL Class I	–	–	0	50	1.650	0.700	20	0.880
3.3-V PCI (4)	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3-V PCI-X 1.0 (4)	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3-V Compact PCI (4)	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3-V AGP 1X (4)	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3-V CTT	–	–	25	50	2.050	1.350	30	1.350

Notes to Table 4–101:

- (1) Input measurement point at internal node is $0.5 \times V_{CCINT}$.
- (2) Output measuring point for data is V_{MEAS} .
- (3) Input stimulus edge rate is 0 to V_{CCINT} in 0.5 ns (internal signal) from the driver preceding the IO buffer.
- (4) The first value is for output rising edge and the second value is for output falling edge. The hyphen (-) indicates infinite resistance or disconnection.

Table 4–102 shows the reporting methodology used by the Quartus II software for minimum timing information for output pins.

Table 4–102. Reporting Methodology For Minimum Timing For Single-Ended Output Pins (Part 1 of 2)
Notes (1), (2), (3)

I/O Standard	Loading and Termination							Measurement Point
	R_{UP} Ω	R_{DN} Ω	R_S Ω	R_T Ω	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS}
3.3-V LVTTTL	–	–	0	–	3.600	3.600	10	1.800
2.5-V LVTTTL	–	–	0	–	2.630	2.630	10	1.200
1.8-V LVTTTL	–	–	0	–	1.950	1.950	10	0.880
1.5-V LVTTTL	–	–	0	–	1.600	1.600	10	0.750
3.3-V LVCMOS	–	–	0	–	3.600	3.600	10	1.800
2.5-V LVCMOS	–	–	0	–	2.630	2.630	10	1.200
1.8-V LVCMOS	–	–	0	–	1.950	1.950	10	0.880
1.5-V LVCMOS	–	–	0	–	1.600	1.600	10	0.750
3.3-V GTL	–	–	0	25	3.600	1.260	30	0.860
2.5-V GTL	–	–	0	25	2.630	1.260	30	0.860
3.3-V GTL+	–	–	0	25	3.600	1.650	30	1.120
2.5-V GTL+	–	–	0	25	2.630	1.650	30	1.120
3.3-V SSTL-3 Class II	–	–	25	25	3.600	1.750	30	1.750
3.3-V SSTL-3 Class I	–	–	25	50	3.600	1.750	30	1.750
2.5-V SSTL-2 Class II	–	–	25	25	2.630	1.390	30	1.390
2.5-V SSTL-2 Class I	–	–	25	50	2.630	1.390	30	1.390
1.8-V SSTL-18 Class II	–	–	25	25	1.950	1.040	30	1.040
1.8-V SSTL-18 Class I	–	–	25	50	1.950	1.040	30	1.040
1.5-V HSTL Class II	–	–	0	25	1.600	0.800	20	0.900
1.5-V HSTL Class I	–	–	0	50	1.600	0.800	20	0.900
1.8-V HSTL Class II	–	–	0	25	1.950	0.900	20	1.000
1.8-V HSTL Class I	–	–	0	50	1.950	0.900	20	1.000
3.3-V PCI (4)	–/25	25/–	0	–	3.600	1.950	10	1.026/2.214
3.3-V PCI-X 1.0 (4)	–/25	25/–	0	–	3.600	1.950	10	1.026/2.214
3.3-V Compact PCI (4)	–/25	25/–	0	–	3.600	3.600	10	1.026/2.214
3.3-V AGP 1× (4)	–/25	25/–	0	–	3.600	3.600	10	1.026/2.214

Table 4–117. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
GTL+	250	200	200	MHz
SSTL-3 Class I	300	250	250	MHz
SSTL-3 Class II	300	250	250	MHz
SSTL-2 Class I	300	250	250	MHz
SSTL-2 Class II	300	250	250	MHz
SSTL-18 Class I	300	250	250	MHz
SSTL-18 Class II	300	250	250	MHz
1.5-V HSTL Class I	300	180	180	MHz
1.5-V HSTL Class II	300	180	180	MHz
1.8-V HSTL Class I	300	180	180	MHz
1.8-V HSTL Class II	300	180	180	MHz
3.3-V PCI	422	390	390	MHz
3.3-V PCI-X 1.0	422	390	390	MHz
Compact PCI	422	390	390	MHz
AGP 1×	422	390	390	MHz
AGP 2×	422	390	390	MHz
CTT	250	180	180	MHz
Differential 1.5-V HSTL C1	300	180	180	MHz
LVPECL (1)	422	400	400	MHz
PCML (1)	215	200	200	MHz
LVDS (1)	422	400	400	MHz
HyperTransport technology (1)	422	400	400	MHz

Table 4–118. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[10..7]CLK Pins in Wire-Bond Packages (Part 1 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz

Table 4–121. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTTL	400	350	300	300	MHz
2.5 V	400	350	300	300	MHz
1.8 V	400	350	300	300	MHz
1.5 V	350	300	300	300	MHz
LVC MOS	400	350	300	300	MHz
GTL	200	167	125	125	MHz
GTL+	200	167	125	125	MHz
SSTL-3 Class I	167	150	133	133	MHz
SSTL-3 Class II	167	150	133	133	MHz
SSTL-2 Class I	150	133	133	133	MHz
SSTL-2 Class II	150	133	133	133	MHz
SSTL-18 Class I	150	133	133	133	MHz
SSTL-18 Class II	150	133	133	133	MHz
1.5-V HSTL Class I	250	225	200	200	MHz
1.5-V HSTL Class II	225	225	200	200	MHz
1.8-V HSTL Class I	250	225	200	200	MHz
1.8-V HSTL Class II	225	225	200	200	MHz
3.3-V PCI	250	225	200	200	MHz
3.3-V PCI-X 1.0	225	225	200	200	MHz
Compact PCI	400	350	300	300	MHz
AGP 1×	400	350	300	300	MHz
AGP 2×	400	350	300	300	MHz
CTT	300	250	200	200	MHz
LVPECL (2)	717	717	500	500	MHz
PCML (2)	420	420	420	420	MHz
LVDS (2)	717	717	500	500	MHz
HyperTransport technology (2)	420	420	420	420	MHz

Table 4–126. High-Speed I/O Specifications for Wire-Bond Packages (Part 1 of 2)											
Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK} (Clock frequency) (LVDS, LVPECL, HyperTransport technology) f _{HCLK} = f _{HSDR} / W	W = 4 to 30 (Serdes used)	10		156	10		115.5	10		115.5	MHz
	W = 2 (Serdes bypass)	50		231	50		231	50		231	MHz
	W = 2 (Serdes used)	150		312	150		231	150		231	MHz
	W = 1 (Serdes bypass)	100		311	100		270	100		270	MHz
	W = 1 (Serdes used)	300		624	300		462	300		462	MHz
f _{HSDR} Device operation, (LVDS, LVPECL, HyperTransport technology)	J = 10	300		624	300		462	300		462	Mbps
	J = 8	300		624	300		462	300		462	Mbps
	J = 7	300		624	300		462	300		462	Mbps
	J = 4	300		624	300		462	300		462	Mbps
	J = 2	100		462	100		462	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		311	100		270	100		270	Mbps
f _{HCLK} (Clock frequency) (PCML) f _{HCLK} = f _{HSDR} / W	W = 4 to 30 (Serdes used)	10		77.75							MHz
	W = 2 (Serdes bypass)	50		150	50		77.5	50		77.5	MHz
	W = 2 (Serdes used)	150		155.5							MHz
	W = 1 (Serdes bypass)	100		200	100		155	100		155	MHz
	W = 1 (Serdes used)	300		311							MHz
Device operation, f _{HSDR} (PCML)	J = 10	300		311							Mbps
	J = 8	300		311							Mbps
	J = 7	300		311							Mbps
	J = 4	300		311							Mbps
	J = 2	100		300	100		155	100		155	Mbps
	J = 1	100		200	100		155	100		155	Mbps
TCCS	All			400			400			400	ps