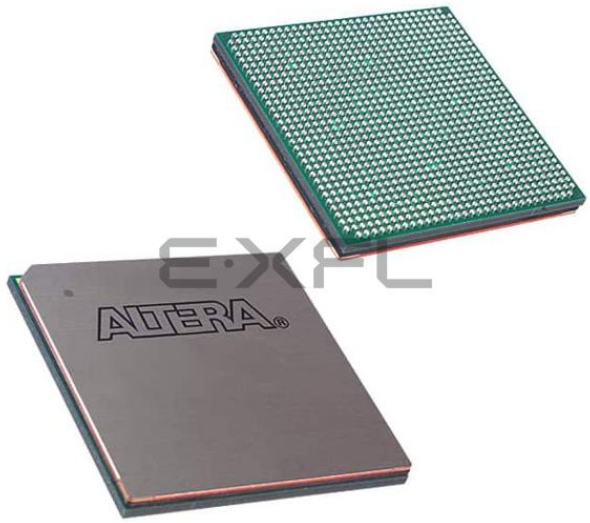


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2566 |
| Number of Logic Elements/Cells | 25660 |
| Total RAM Bits | 1944576 |
| Number of I/O | 706 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1020-BBGA |
| Supplier Device Package | 1020-FBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1s25f1020i6 |

*Table 1–5. Stratix FineLine BGA Package Sizes*

| Dimension | 484 Pin | 672 Pin | 780 Pin | 1,020 Pin | 1,508 Pin |
|---|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 529 | 729 | 841 | 1,089 | 1,600 |
| Length × width (mm × mm) | 23 × 23 | 27 × 27 | 29 × 29 | 33 × 33 | 40 × 40 |

Stratix devices are available in up to four speed grades, -5, -6, -7, and -8, with -5 being the fastest. Table 1–6 shows Stratix device speed-grade offerings.

*Table 1–6. Stratix Device Speed Grades*

| Device | 672-Pin BGA | 956-Pin BGA | 484-Pin FineLine BGA | 672-Pin FineLine BGA | 780-Pin FineLine BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|
| EP1S10 | -6, -7 | | -5, -6, -7 | -6, -7 | -5, -6, -7 | | |
| EP1S20 | -6, -7 | | -5, -6, -7 | -6, -7 | -5, -6, -7 | | |
| EP1S25 | -6, -7 | | | -6, -7, -8 | -5, -6, -7 | -5, -6, -7 | |
| EP1S30 | | -5, -6, -7 | | | -5, -6, -7, -8 | -5, -6, -7 | |
| EP1S40 | | -5, -6, -7 | | | -5, -6, -7, -8 | -5, -6, -7 | -5, -6, -7 |
| EP1S60 | | -6, -7 | | | | -5, -6, -7 | -6, -7 |
| EP1S80 | | -6, -7 | | | | -5, -6, -7 | -5, -6, -7 |

Figure 2–8 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix™ memory and DSP blocks. A carry chain can continue as far as a full column.

asynchronous load, and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Stratix devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

## MultiTrack Interconnect

In the Stratix architecture, connections between LEs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks.
- R4 interconnects traversing four blocks to the right or left.
- R8 interconnects traversing eight blocks to the right or left.
- R24 row interconnects for high-speed access across the length of the device.

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. Only one side of a M-RAM block interfaces with direct link and row interconnects. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast

TriMatrix memory architecture can implement pipelined RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (WREN) signal derived from the global or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM WREN signal while ensuring its data and address signals meet setup and hold time specifications relative to the WREN signal. The output registers can be bypassed. Flow-through reading is possible in the simple dual-port mode of M512 and M4K RAM blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple TriMatrix memory blocks. For example, two 256 × 16-bit RAM blocks can be combined to form a 256 × 32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words available in one memory block. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

## Clear Signals

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

## Parity Bit Support

The memory blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. In the M4K and M-RAM blocks, byte enables are also available for data input masking during write operations.

### *Adder/Subtractor/Accumulator*

The adder/subtractor/accumulator is the first level of the adder/output block and can be used as an accumulator or as an adder/subtractor.

**Adder/Subtractor**
Each adder/subtractor/accumulator block can perform addition or subtraction using the `addnsub` independent control signal for each first-level adder in 18 × 18-bit mode. There are two `addnsub[1..0]` signals available in a DSP block for any configuration. For 9 × 9-bit mode, one `addnsub[1..0]` signal controls the top two one-level adders and another `addnsub[1..0]` signal controls the bottom two one-level adders. A high `addnsub` signal indicates addition, and a low signal indicates subtraction. The `addnsub` control signal can be unregistered or registered once or twice when feeding the adder blocks to match data path pipelines.

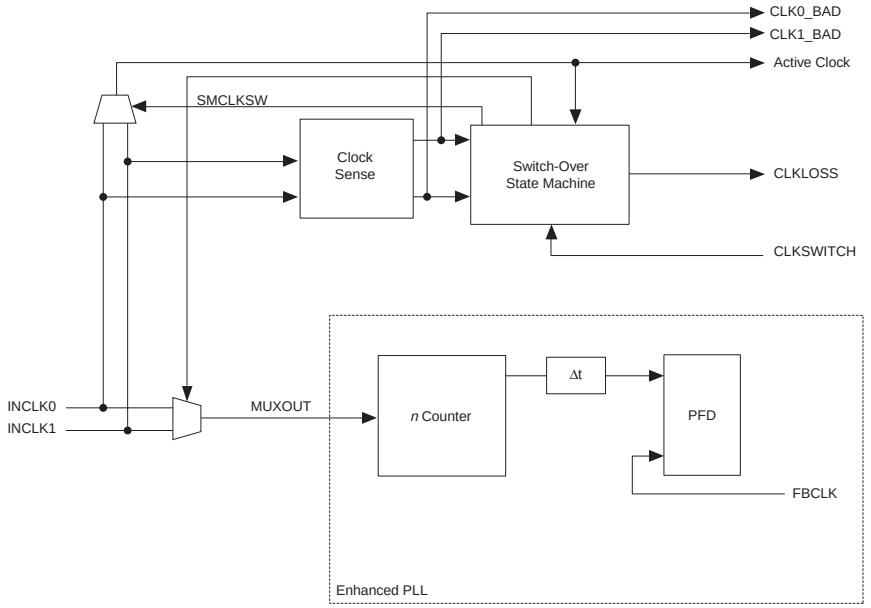
The `signa` and `signb` signals serve the same function as the multiplier block `signa` and `signb` signals. The only difference is that these signals can be registered up to two times. These signals are tied to the same `signa` and `signb` signals from the multiplier and must be connected to the same clocks and control signals.

**Accumulator**
When configured for accumulation, the adder/output block output feeds back to the accumulator as shown in Figure 2–34. The `accum_sload[1..0]` signal synchronously loads the multiplier result to the accumulator output. This signal can be unregistered or registered once or twice. Additionally, the `overflow` signal indicates the accumulator has overflowed or underflowed in accumulation mode. This signal is always registered and must be externally latched in LEs if the design requires a latched `overflow` signal.

### *Summation*

The output of the adder/subtractor/accumulator block feeds to an optional summation block. This block sums the outputs of the DSP block multipliers. In 9 × 9-bit mode, there are two summation blocks providing the sums of two sets of four 9 × 9-bit multipliers. In 18 × 18-bit mode, there is one summation providing the sum of one set of four 18 × 18-bit multipliers.

*Figure 2–53. Clock Switchover Circuitry*




There are two possible ways to use the clock switchover feature.

- Use automatic switchover circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 2–53. In this case, the secondary clock becomes the reference clock for the PLL.
- Use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. You can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

### *Control Signals*

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL.

If the input clock stops and causes the PLL to lose lock, then the PLL must be reset for correct phase shift operation.

For more information on high-speed differential I/O support, see "High-Speed Differential I/O Support" on page 2–130.

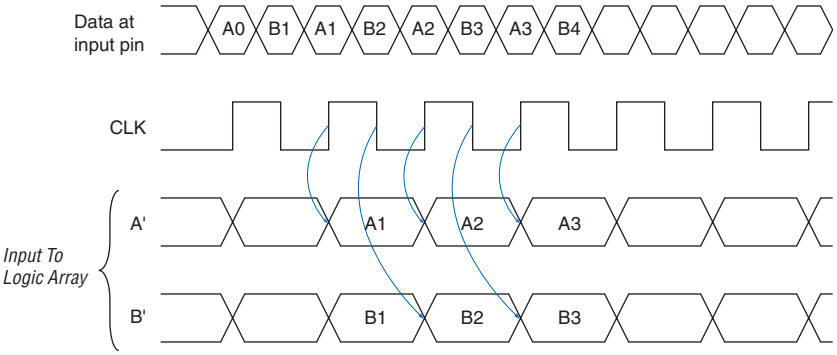
## I/O Structure

IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Differential on-chip termination for LVDS I/O standard
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double-data rate (DDR) Registers

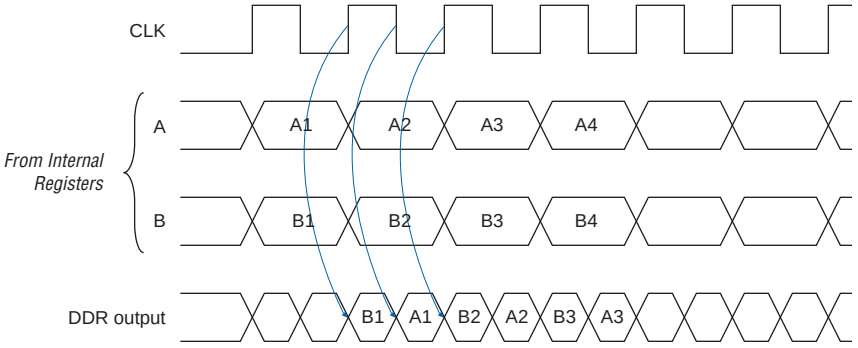
The IOE in Stratix devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–59 shows the Stratix IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

*Figure 2–66. Input Timing Diagram in DDR Mode*




When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 2–67 shows the IOE configured for DDR output. Figure 2–68 shows the DDR output timing diagram.

*Figure 2–68. Output Timing Diagram in DDR Mode*




The Stratix IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

## External RAM Interfacing

Stratix devices support DDR SDRAM at up to 200 MHz (400-Mbps data rate) through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces up to 200 MHz. Stratix devices also provide preliminary support for reduced latency DRAM II (RLDRAM II) at rates up to 200 MHz through the dedicated phase-shift circuitry.

In addition to the required signals for external memory interfacing, Stratix devices offer the optional clock enable signal. By default the Quartus II software sets the clock enable signal high, which tells the output register to update with new values. The output registers hold their own values if the design sets the clock enable signal low. See Figure 2–64.

To find out more about the DDR SDRAM specification, see the JEDEC web site (**www.jedec.org**). For information on memory controller megafunctions for Stratix devices, see the Altera web site (**www.altera.com**). See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices* for more information on DDR SDRAM interface in Stratix. Also see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices* and *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

*Table 2–41. EP1S80 Differential Channels (Part 2 of 2)* Note (1)

| Package | Transmitter/ Receiver | Total Channels | Maximum Speed (Mbps) | Center Fast PLLs | | | | Corner Fast PLLs (2), (3) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL1 | PLL2 | PLL3 | PLL4 | PLL7 | PLL8 | PLL9 | PLL10 |
| 1,508-pin FineLine BGA | Transmitter (4) | 80 (72) (7) | 840 | 10 (10) | 10 (10) | 10 (10) | 10 (10) | 20 (8) | 20 (8) | 20 (8) | 20 (8) |
| | | | 840 (5),(8) | 20 (20) | 20 (20) | 20 (20) | 20 (20) | 20 (8) | 20 (8) | 20 (8) | 20 (8) |
| | Receiver | 80 (56) (7) | 840 | 20 | 20 | 20 | 20 | 10 (14) | 10 (14) | 10 (14) | 10 (14) |
| | | | 840 (5),(8) | 40 | 40 | 40 | 40 | 10 (14) | 10 (14) | 10 (14) | 10 (14) |

***Notes to Tables 2–38 through 2–41:***

(1) The first row for each transmitter or receiver reports the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 780-pin FineLine BGA EP1S30 device, PLL 1 can drive a maximum of 18 transmitter channels at 840 Mbps or a maximum of 35 transmitter channels at 840 Mbps. The Quartus II software may also merge transmitter and receiver PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) Some of the channels accessible by the center fast PLL and the channels accessible by the corner fast PLL overlap. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10. For more information on which channels overlap, see the Stratix device pin-outs at **www.altera.com**.

(3) The corner fast PLLs in this device support a data rate of 840 Mbps for channels labeled "high" speed in the device pin-outs at **www.altera.com**.

(4) The numbers of channels listed include the transmitter clock output (`tx_outclock`) channel. An extra data channel can be used if a DDR clock is needed.

(5) These channels span across two I/O banks per side of the device. When a center PLL clocks channels in the opposite bank on the same side of the device it is called cross-bank PLL support. Both center PLLs can clock cross-bank channels simultaneously if say PLL_1 is clocking all receiver channels and PLL_2 is clocking all transmitter channels. You cannot have two adjacent PLLs simultaneously clocking cross-bank receiver channels or two adjacent PLLs simultaneously clocking transmitter channels. Cross-bank allows for all receiver channels on one side of the device to be clocked on one clock while all transmitter channels on the device are clocked on the other center PLL. Crossbank PLLs are supported at full-speed, 840 Mbps. For wire-bond devices, the full-speed is 624 Mbps.

(6) PLLs 7, 8, 9, and 10 are not available in this device.

(7) The number in parentheses is the number of slow-speed channels, guaranteed to operate at up to 462 Mbps. These channels are independent of the high-speed differential channels. For the location of these channels, see the device pin-outs at **www.altera.com**.

(8) See the Stratix device pin-outs at **www.altera.com**. Channels marked "high" speed are 840 MBps and "low" speed channels are 462 MBps.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- UTOPIA IV
- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- 10G Ethernet XSBI

*Table 4–10. 3.3-V LVDS I/O Specifications (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{ICM}$ | Input common mode voltage *(6)* | LVDS<br>0.3 V ≤$V_{ID}$ ≤1.0 V<br>*W* = 1 through 10 | 100 | | 1,100 | mV |
| | | LVDS<br>0.3 V ≤$V_{ID}$ ≤1.0 V<br>*W* = 1 through 10 | 1,600 | | 1,800 | mV |
| | | LVDS<br>0.2 V ≤$V_{ID}$ ≤1.0 V<br>*W* = 1 | 1,100 | | 1,600 | mV |
| | | LVDS<br>0.1 V ≤$V_{ID}$ ≤1.0 V<br>*W* = 2 through 10 | 1,100 | | 1,600 | mV |
| $V_{OD}$ *(1)* | Output differential voltage (single-ended) | $R_L$ = 100 Ω | 250 | 375 | 550 | mV |
| Δ $V_{OD}$ | Change in $V_{OD}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $V_{OCM}$ | Output common mode voltage | $R_L$ = 100 Ω | 1,125 | 1,200 | 1,375 | mV |
| Δ $V_{OCM}$ | Change in $V_{OCM}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $R_L$ | Receiver differential input discrete resistor (external to Stratix devices) | | 90 | 100 | 110 | Ω |

*Table 4–20. SSTL-2 Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.18 | | 3.0 | V |
| $V_{IL(DC)}$ | Low-level DC input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.35 | | | V |
| $V_{IL(AC)}$ | Low-level AC input voltage | | | | $V_{REF}$ – 0.35 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8.1 mA *(3)* | $V_{TT}$ + 0.57 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8.1 mA *(3)* | | | $V_{TT}$ – 0.57 | V |

*Table 4–21. SSTL-2 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V |
| $V_{REF}$ | Reference voltage | | 1.15 | 1.25 | 1.35 | V |
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.18 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL(DC)}$ | Low-level DC input voltage | | –0.3 | | $V_{REF}$ – 0.18 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.35 | | | V |
| $V_{IL(AC)}$ | Low-level AC input voltage | | | | $V_{REF}$ – 0.35 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16.4 mA *(3)* | $V_{TT}$ + 0.76 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16.4 mA *(3)* | | | $V_{TT}$ – 0.76 | V |

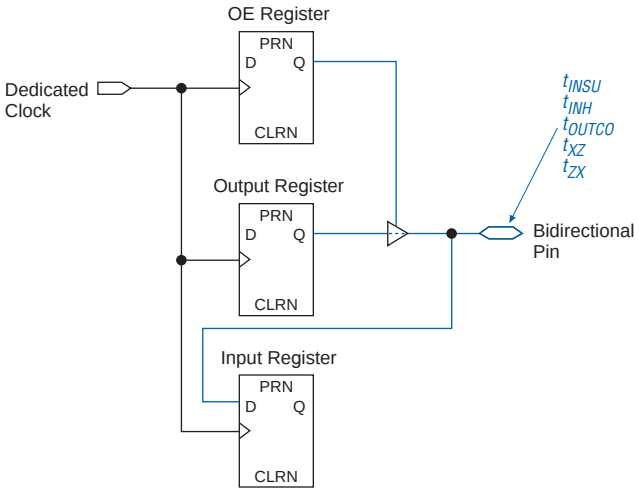
*Table 4–22. SSTL-3 Class I Specifications (Part 1 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL(DC)}$ | Low-level DC input voltage | | –0.3 | | $V_{REF}$ – 0.2 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.4 | | | V |

## External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–4 shows the pin-to-pin timing model for bidirectional IOE pin timing. All registers are within the IOE.

*Figure 4–4. External Timing in Stratix Devices*




All external timing parameters reported in this section are defined with respect to the dedicated clock pin as the starting point. All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the 24-mA current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4–103 through 4–108.

*Table 4–59. EP1S10 External I/O Timing on Row Pins Using Regional Clock Networks* *Note (1)*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.161 | | 2.336 | | 2.685 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 2.434 | 4.889 | 2.434 | 5.226 | 2.434 | 5.643 | NA | NA | ns |
| $t_{XZ}$ | 2.461 | 4.493 | 2.461 | 5.282 | 2.461 | 5.711 | NA | NA | ns |
| $t_{ZX}$ | 2.461 | 4.493 | 2.461 | 5.282 | 2.461 | 5.711 | NA | NA | ns |
| $t_{INSUPLL}$ | 1.057 | | 1.172 | | 1.315 | | NA | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCOPLL}$ | 1.327 | 2.773 | 1.327 | 2.848 | 1.327 | 2.940 | NA | NA | ns |
| $t_{XZPLL}$ | 1.354 | 2.827 | 1.354 | 2.904 | 1.354 | 3.008 | NA | NA | ns |
| $t_{ZXPLL}$ | 1.354 | 2.827 | 1.354 | 2.904 | 1.354 | 3.008 | NA | NA | ns |

*Table 4–60. EP1S10 External I/O Timing on Row Pins Using Global Clock Networks* *Note (1)*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.787 | | 1.944 | | 2.232 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 2.647 | 5.263 | 2.647 | 5.618 | 2.647 | 6.069 | NA | NA | ns |
| $t_{XZ}$ | 2.674 | 5.317 | 2.674 | 5.674 | 2.674 | 6.164 | NA | NA | ns |
| $t_{ZX}$ | 2.674 | 5.317 | 2.674 | 5.674 | 2.674 | 6.164 | NA | NA | ns |
| $t_{INSUPLL}$ | 1.371 | | 1.1472 | | 1.654 | | NA | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCOPLL}$ | 1.144 | 2.459 | 1.144 | 2.548 | 1.144 | 2.601 | NA | NA | ns |
| $t_{XZPLL}$ | 1.171 | 2.513 | 1.171 | 2.604 | 1.171 | 2.669 | NA | NA | ns |
| $t^{ZXPLL}$ | 1.171 | 2.513 | 1.171 | 2.604 | 1.171 | 2.669 | NA | NA | ns |

*Note to Tables 4–55 to 4–60:*

(1) Only EP1S25, EP1S30, and EP1S40 have speed grade of -8.

Tables 4–67 through 4–72 show the external timing parameters on column and row pins for EP1S25 devices.

*Table 4–67. EP1S25 External I/O Timing on Column Pins Using Fast Regional Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.412 | | 2.613 | | 2.968 | | 3.468 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.196 | 4.475 | 2.196 | 4.748 | 2.196 | 5.118 | 2.196 | 5.603 | ns |
| $t_{XZ}$ | 2.136 | 4.349 | 2.136 | 4.616 | 2.136 | 4.994 | 2.136 | 5.488 | ns |
| $t_{ZX}$ | 2.136 | 4.349 | 2.136 | 4.616 | 2.136 | 4.994 | 2.136 | 5.488 | ns |

*Table 4–68. EP1S25 External I/O Timing on Column Pins Using Regional Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.535 | | 1.661 | | 1.877 | | 2.125 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.739 | 5.396 | 2.739 | 5.746 | 2.739 | 6.262 | 2.739 | 6.946 | ns |
| $t_{XZ}$ | 2.679 | 5.270 | 2.679 | 5.614 | 2.679 | 6.138 | 2.679 | 6.831 | ns |
| $t_{ZX}$ | 2.679 | 5.270 | 2.679 | 5.614 | 2.679 | 6.138 | 2.679 | 6.831 | ns |
| $t_{INSUPLL}$ | 0.934 | | 0.980 | | 1.092 | | 1.231 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.316 | 2.733 | 1.316 | 2.839 | 1.316 | 2.921 | 1.316 | 3.110 | ns |
| $t^{XZPLL}$ | 1.256 | 2.607 | 1.256 | 2.707 | 1.256 | 2.797 | 1.256 | 2.995 | ns |
| $t_{ZXPLL}$ | 1.256 | 2.607 | 1.256 | 2.707 | 1.256 | 2.797 | 1.256 | 2.995 | ns |

*Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 2 of 4)* Notes (1), (2)

| Symbol | Conditions | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | -8 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (Clock frequency) (PCML) $f_{HSCLK} = f_{HSDR} / W$ | *W* = 4 to 30 (Serdes used) | 10 | | 100 | 10 | | 100 | 10 | | 77.75 | 10 | | 77.75 | MHz |
| | W = 2 (Serdes bypass) | 50 | | 200 | 50 | | 200 | 50 | | 150 | 50 | | 150 | MHz |
| | W = 2 (Serdes used) | 150 | | 200 | 150 | | 200 | 150 | | 155.5 | 150 | | 155.5 | MHz |
| | W = 1 (Serdes bypass) | 100 | | 250 | 100 | | 250 | 100 | | 200 | 100 | | 200 | MHz |
| | W = 1 (Serdes used) | 300 | | 400 | 300 | | 400 | 300 | | 311 | 300 | | 311 | MHz |
| $f_{HSDR}$ Device operation (PCML) | *J* = 10 | 300 | | 400 | 300 | | 400 | 300 | | 311 | 300 | | 311 | Mbps |
| | *J* = 8 | 300 | | 400 | 300 | | 400 | 300 | | 311 | 300 | | 311 | Mbps |
| | *J* = 7 | 300 | | 400 | 300 | | 400 | 300 | | 311 | 300 | | 311 | Mbps |
| | *J* = 4 | 300 | | 400 | 300 | | 400 | 300 | | 311 | 300 | | 311 | Mbps |
| | *J* = 2 | 100 | | 400 | 100 | | 400 | 100 | | 300 | 100 | | 300 | Mbps |
| | *J* = 1 | 100 | | 250 | 100 | | 250 | 100 | | 200 | 100 | | 200 | Mbps |
| TCCS | All | | | 200 | | | 200 | | | 300 | | | 300 | ps |

*Table 4–126. High-Speed I/O Specifications for Wire-Bond Packages (Part 2 of 2)*

| Symbol | Conditions | -6 Speed Grade | | | -7 Speed Grade | | | -8 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SW | PCML (J = 4, 7, 8, 10) only | 800 | | | 800 | | | 800 | | | ps |
| | PCML (J = 2) only | 1,200 | | | 1,200 | | | 1,200 | | | ps |
| | PCML (J = 1) only | 1,700 | | | 1,700 | | | 1,700 | | | ps |
| | LVDS and LVPECL (J = 1) only | 550 | | | 550 | | | 550 | | | ps |
| | LVDS, LVPECL, HyperTransport technology (J = 2 through 10) only | 500 | | | 500 | | | 500 | | | ps |
| Input jitter tolerance (peak-to-peak) | All | | | 250 | | | 250 | | | 250 | ps |
| Output jitter (peak-to-peak) | All | | | 200 | | | 200 | | | 200 | ps |
| Output $t_{RISE}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport technology | 120 | 170 | 200 | 120 | 170 | 200 | 120 | 170 | 200 | ps |
| | LVPECL | 100 | 135 | 150 | 100 | 135 | 150 | 100 | 135 | 150 | ps |
| | PCML | 80 | 110 | 135 | 80 | 110 | 135 | 80 | 110 | 135 | ps |
| Output $t_{FALL}$ | LVDS | 80 | 110 | 120 | 80 | 110 | 120 | 80 | 110 | 120 | ps |
| | HyperTransport | 110 | 170 | 200 | 110 | 170 | 200 | 110 | 170 | 200 | ps |
| | LVPECL | 100 | 135 | 160 | 100 | 135 | 160 | 100 | 135 | 160 | ps |
| | PCML | 110 | 145 | 175 | 110 | 145 | 175 | 110 | 145 | 175 | ps |
| $t_{DUTY}$ | LVDS (J = 2 through10) only | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | % |
| | LVDS (J =1) and LVPECL, PCML, HyperTransport technology | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{LOCK}$ | All | | | 100 | | | 100 | | | 100 | µs |

*Table 4–129. Enhanced PLL Specifications for -7 Speed Grade (Part 2 of 2)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |
| $t_{JITTER}$ | Period jitter for external clock output *(6)* | | | ±100 ps for >200-MHz `outclk`<br>±20 mUI for <200-MHz `outclk` | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(5)* | | | 22 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(7)* *(11)* | *(9)* | | 100 | µs |
| $t_{LOCK}$ | Time required to lock from end of device configuration *(11)* | 10 | | 400 | µs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 600 *(8)* | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(10)* | 0.5 | | 0.6 | % |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal | 10 | | | ns |

*Table 4–130. Enhanced PLL Specifications for -8 Speed Grade (Part 1 of 3)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)*, *(2)* | | 480 | MHz |
| $f_{INPFD}$ | Input frequency to PFD | 3 | | 420 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock period jitter | | | ±200 *(3)* | ps |

*Table 4–132. Fast PLL Specifications for -7 Speed Grades (Part 2 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JITTER}$ | Period jitter for DIFFIO clock out *(6)* | | *(5)* | ps |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | µs |
| m | Multiplication factors for *m* counter *(7)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(7)*, *(8)* | 1 | 32 | Integer |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal | 10 | | ns |

*Table 4–133. Fast PLL Specifications for -8 Speed Grades (Part 1 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{IN}$ | `CLKIN` frequency *(1)*, *(3)* | 10 | 460 | MHz |
| $f_{INPFD}$ | Input frequency to PFD | 10 | 500 | MHz |
| $f_{OUT}$ | Output frequency for internal global or regional clock *(4)* | 9.375 | 420 | MHz |
| $f_{OUT\_DIFFIO}$ | Output frequency for external clock driven out on a differential I/O data channel | *(5)* | *(5)* | MHz |
| $f_{VCO}$ | VCO operating frequency | 300 | 700 | MHz |
| $t_{INDUTY}$ | `CLKIN` duty cycle | 40 | 60 | % |
| $t_{INJITTER}$ | Period jitter for `CLKIN` pin | | ±200 | ps |
| $t_{DUTY}$ | Duty cycle for `DFFIO` 1× `CLKOUT` pin *(6)* | 45 | 55 | % |
| $t_{JITTER}$ | Period jitter for DIFFIO clock out *(6)* | | *(5)* | ps |
| $t_{LOCK}$ | Time required for PLL to acquire lock | 10 | 100 | µs |
| m | Multiplication factors for *m* counter *(7)* | 1 | 32 | Integer |
| *l*0, *l*1, *g*0 | Multiplication factors for *l*0, *l*1, and *g*0 counter *(7)*, *(8)* | 1 | 32 | Integer |

*Figure 5–1. Stratix Device Packaging Ordering Information*