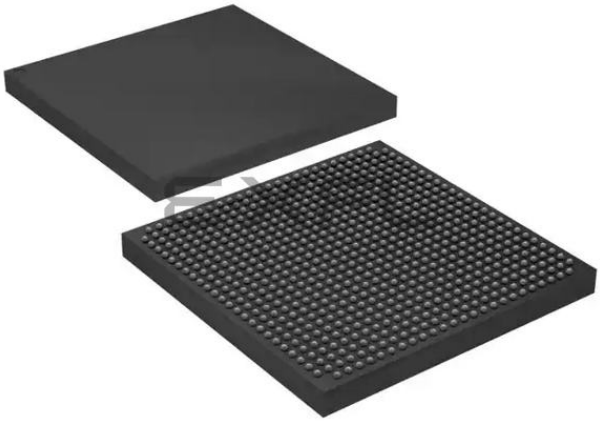

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2566 |
| Number of Logic Elements/Cells | 25660 |
| Total RAM Bits | 1944576 |
| Number of I/O | 473 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1s25f672i7 |

| Chapter | Date/Version | Changes Made |
|---|---|---|
| 4 | October 2003, v2.1 | • Added -8 speed grade information.<br>• Updated performance information in Table 4–36.<br>• Updated timing information in Tables 4–55 through 4–96.<br>• Updated delay information in Tables 4–103 through 4–108.<br>• Updated programmable delay information in Tables 4–100 and 4–103. |
| | July 2003, v2.0 | • Updated clock rates in Tables 4–114 through 4–123.<br>• Updated speed grade information in the introduction on page 4-1.<br>• Corrected figures 4-1 & 4-2 and Table 4-9 to reflect how VID and VOD are specified.<br>• Added note 6 to Table 4-32.<br>• Updated Stratix Performance Table 4-35.<br>• Updated EP1S60 and EP1S80 timing parameters in Tables 4-82 to 4-93. The Stratix timing models are final for all devices.<br>• Updated Stratix IOE programmable delay chains in Tables 4-100 to 4-101.<br>• Added single-ended I/O standard output pin delay adders for loading in Table 4-102.<br>• Added spec for FPLL[10..7]CLK pins in Tables 4-104 and 4-107.<br>• Updated high-speed I/O specification for J=2 in Tables 4-114 and 4-115.<br>• Updated EPLL specification and fast PLL specification in Tables 4-116 to 4-120. |
| 5 | September 2004, v2.1 | • Updated reference to device pin-outs on page 5–1 to indicate that device pin-outs are no longer included in this manual and are now available on the Altera web site. |
| | April 2003, v1.0 | • No new changes in Stratix Device Handbook v2.0. |

## Shift Register Support

You can configure embedded memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a $w \times m \times n$ shift register is determined by the input data width ($w$), the length of the taps ($m$), and the number of taps ($n$). The size of a $w \times m \times n$ shift register must be less than or equal to the maximum number of memory bits in the respective block: 576 bits for the M512 RAM block and 4,608 bits for the M4K RAM block. The total number of shift register outputs (number of taps $n \times$ width $w$) must be less than the maximum data width of the RAM block (18 for M512 blocks, 36 for M4K blocks). To create larger shift registers, the memory blocks are cascaded together.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 2–14 shows the TriMatrix memory block in the shift register mode.

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2–7 summarizes the byte selection.

*Table 2–7. Byte Enable for M4K Blocks Notes (1), (2)*

| byteena[3..0] | datain ×18 | datain ×36 |
|---|---|---|
| [0] = 1 | [8..0] | [8..0] |
| [1] = 1 | [17..9] | [17..9] |
| [2] = 1 | – | [26..18] |
| [3] = 1 | – | [35..27] |

*Notes to Table 2–7:*
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The eight `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–17.

The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2–18 shows the M4K RAM block to logic array interface.

### Clock Multiplication & Division

Each Stratix device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times$ post-scale counter) scaling factors. The input clock is divided by a pre-scale divider, $n$, and is then multiplied by the $m$ feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale counter, $n$, and one multiply counter, $m$, per PLL, with a range of 1 to 512 on each. There are two post-scale counters ($l$) for regional clock output ports, four counters ($g$) for global clock output ports, and up to four counters ($e$) for external clock outputs, all ranging from 1 to 1024 with a 50% duty cycle setting. The post-scale counters range from 1 to 512 with any non-50% duty cycle setting. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

### Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix device enhanced PLLs support a flexible clock switchover capability. Figure 2–53 shows a block diagram of the switchover circuit.The switchover circuit is configurable, so you can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

The pllenable pin is a dedicated pin that enables/disables PLLs. When the pllenable pin is low, the clock output ports are driven by GND and all the PLLs go out of lock. When the pllenable pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the pllenable signal by connecting the pllenable input port of the altpll megafunction to the common pllenable input pin.

The areset signals are reset/resynchronization inputs for each PLL. The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the areset signal in designs if any of the following conditions are true:

- PLL Reconfiguration or Clock switchover enables in the design.
- Phase relationships between output clocks need to be maintained after a loss of lock condition

The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value than desired as the PLL locks. If the system cannot tolerate this, the clkena signal can disable the output clocks until the PLL locks.

The pfdena signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or a clkloss status signal to trigger pfdena.

The clkena signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own clkena signal. The clkena signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the *g* and *l* counters. The clkena signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. Figure 2–57 shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the clkena signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a

## Programmable Pull-Up Resistor

Each Stratix device I/O pin provides an optional programmable pull-up resistor during user mode. If this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the $V_{CCIO}$ level of the output pin's bank. Table 2–30 shows which pin types support the weak pull-up resistor feature.

*Table 2–30. Programmable Weak Pull-Up Resistor Support*

| Pin Type | Programmable Weak Pull-Up Resistor |
|---|---|
| I/O pins | ✓ |
| CLK[15..0] | |
| FCLK | ✓ |
| FPLL[7..10]CLK | |
| Configuration pins | |
| JTAG pins | ✓ *(1)* |

***Note to Table 2–30:***
(1) TDO pins do not support programmable weak pull-up resistors.

## Advanced I/O Standard Support

Stratix device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP (1× and 2×)
- LVDS
- LVPECL
- 3.3-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output column clock pins only)
- GTL/GTL+
- 1.5-V HSTL Class I and II

For more information on I/O standards supported by Stratix devices, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook, Volume 2*.

Stratix devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in Figure 2–70. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in Table 2–31 except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. Table 2–32 shows I/O standard support for each I/O bank.

The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 2–36 summarizes Stratix MultiVolt I/O support.

*Table 2–36. Stratix MultiVolt I/O Support Note (1)*

| $V_{CCIO}$ (V) | Input Signal (5) | | | | | Output Signal (6) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5.0 V |
| 1.5 | ✓ | ✓ | ✓ (2) | ✓ (2) | | ✓ | | | | |
| 1.8 | ✓ (2) | ✓ | ✓ (2) | ✓ (2) | | ✓ (3) | ✓ | | | |
| 2.5 | | | ✓ | ✓ | | ✓ (3) | ✓ (3) | ✓ | | |
| 3.3 | | | ✓ (2) | ✓ | ✓ (4) | ✓ (3) | ✓ (3) | ✓ (3) | ✓ | ✓ |

*Notes to Table 2–36:*

(1) To drive inputs higher than $V_{CCIO}$ but less than 4.1 V, disable the PCI clamping diode. However, to drive 5.0-V inputs to the device, enable the PCI clamping diode to prevent $V_I$ from rising above 4.0 V.
(2) The input pin current may be slightly higher than the typical value.
(3) Although $V_{CCIO}$ specifies the voltage necessary for the Stratix device to drive out, a receiving device powered at a different level can still interface with the Stratix device if it has inputs that tolerate the $V_{CCIO}$ value.
(4) Stratix devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.
(5) This is the external signal that is driving the Stratix device.
(6) This represents the system voltage that Stratix supports when a VCCIO pin is connected to a specific voltage level. For example, when VCCIO is 3.3 V and if the I/O standard is LVTTL/LVCMOS, the output high of the signal coming out from Stratix is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

## High-Speed Differential I/O Support

Stratix devices contain dedicated circuitry for supporting differential standards at speeds up to 840 Mbps. The following differential I/O standards are supported in the Stratix device: LVDS, LVPECL, HyperTransport, and 3.3-V PCML.

There are four dedicated high-speed PLLs in the EP1S10 to EP1S25 devices and eight dedicated high-speed PLLs in the EP1S30 to EP1S80 devices to multiply reference clocks and drive high-speed differential SERDES channels.

See the Stratix device pin-outs at **www.altera.com** for additional high speed DIFFIO pin information for Stratix devices.

While in the factory configuration, the factory-configuration logic performs the following operations:

- Loads a remote update-control register to determine the page address of the new application configuration
- Determines whether to enable a user watchdog timer for the application configuration
- Determines what the watchdog timer setting should be if it is enabled

The user watchdog timer is a counter that must be continually reset within a specific amount of time in the user mode of an application configuration to ensure that valid configuration occurred during a remote update. Only valid application configurations designed for remote update can reset the user watchdog timer in user mode. If a valid application configuration does not reset the user watchdog timer in a specific amount of time, the timer updates a status register and loads the factory configuration. The user watchdog timer is automatically disabled for factory configurations.

If an error occurs in loading the application configuration, the configuration logic writes a status register to specify the cause of the error. Once this occurs, the Stratix device automatically loads the factory configuration, which reads the status register and determines the reason for reconfiguration. Based on the reason, the factory configuration will take appropriate steps and will write the remote update control register to specify the next application configuration page to be loaded.

When the Stratix device successfully loads the application configuration, it enters into user mode. The Stratix device then executes the main application of the user. Intellectual property (IP), such as a Nios® (16-bit ISA) and Nios® II (32-bit ISA) embedded processors, can help the Stratix device determine when remote update is coming. The Nios embedded processor or user logic receives incoming data, writes it to the configuration device, and loads the factory configuration. The factory configuration will read the remote update status register and determine the valid application configuration to load. Figure 3–2 shows the Stratix remote update. Figure 3–3 shows the transition diagram for remote update mode.

*Table 4–7. 1.8-V I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.95 | V |
| $V_{IH}$ | High-level input voltage | | 0.65 × $V_{CCIO}$ | 2.25 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.35 × $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –2 to –8 mA *(10)* | $V_{CCIO}$ – 0.45 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 to 8 mA *(10)* | | 0.45 | V |

*Table 4–8. 1.5-V I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.4 | 1.6 | V |
| $V_{IH}$ | High-level input voltage | | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | 0.35 × $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –2 mA *(10)* | 0.75 × $V_{CCIO}$ | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA *(10)* | | 0.25 × $V_{CCIO}$ | V |

***Notes to Tables 4–1 through 4–8:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns, or overshoot to the voltage shown in Table 4–9, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.

(5) $V_{CCIO}$ maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.

(7) Typical values are for $T_A$ = 25°C, $V_{CCINT}$ = 1.5 V, and $V_{CCIO}$ = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all $V_{CCIO}$ settings (3.3, 2.5, 1.8, and 1.5 V).

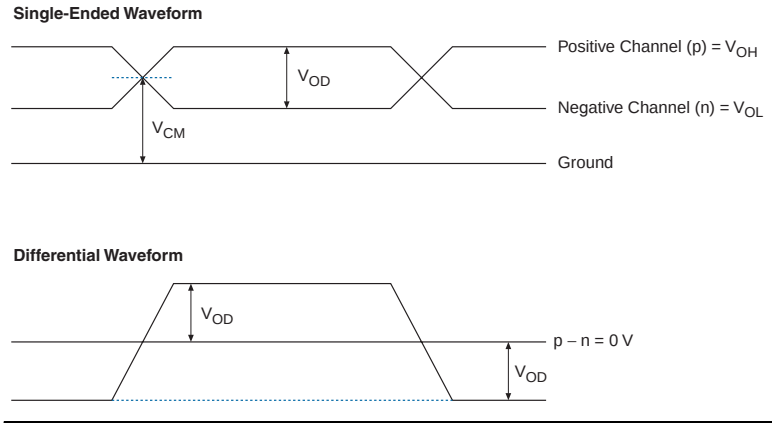
(9) Pin pull-up resistance values will lower if an external source drives the pin higher than $V_{CCIO}$.

(10) Drive strength is programmable according to the values shown in the *Stratix Architecture* chapter of the *Stratix Device Handbook, Volume 1*.

*Table 4–9. Overshoot Input Voltage with Respect to Duty Cycle (Part 1 of 2)*

| Vin (V) | Maximum Duty Cycle (%) |
|---|---|
| 4.0 | 100 |
| 4.1 | 90 |
| 4.2 | 50 |

*Figure 4–2. Transmitter Output Waveforms for Differential I/O Standards*




Tables 4–10 through 4–33 recommend operating conditions, DC operating conditions, and capacitance for 1.5-V Stratix devices.

*Table 4–10. 3.3-V LVDS I/O Specifications (Part 1 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{ID}$ *(6)* | Input differential voltage swing (single-ended) | 0.1 V ≤$V_{CM}$ < 1.1 V<br>*W* = 1 through 10 | 300 | | 1,000 | mV |
| | | 1.1 V ≤$V_{CM}$ ≤1.6 V<br>*W* = 1 | 200 | | 1,000 | mV |
| | | 1.1 V ≤$V_{CM}$ ≤1.6 V<br>*W* = 2 through10 | 100 | | 1,000 | mV |
| | | 1.6 V < $V_{CM}$ ≤1.8 V<br>*W* = 1 through 10 | 300 | | 1,000 | mV |

### *Definition of I/O Skew*

I/O skew is defined as the absolute value of the worst-case difference in clock-to-out times ($t_{CO}$) between any two output registers fed by a common clock source.

I/O bank skew is made up of the following components:

- Clock network skews: This is the difference between the arrival times of the clock at the clock input port of the two IOE registers.
- Package skews: This is the package trace length differences between (I/O pad A to I/O pin A) and (I/O pad B to I/O pin B).

Figure 4–5 shows an example of two IOE registers located in the same bank, being fed by a common clock source. The clock can come from an input pin or from a PLL output.

***Figure 4–5. I/O Skew within an I/O Bank***

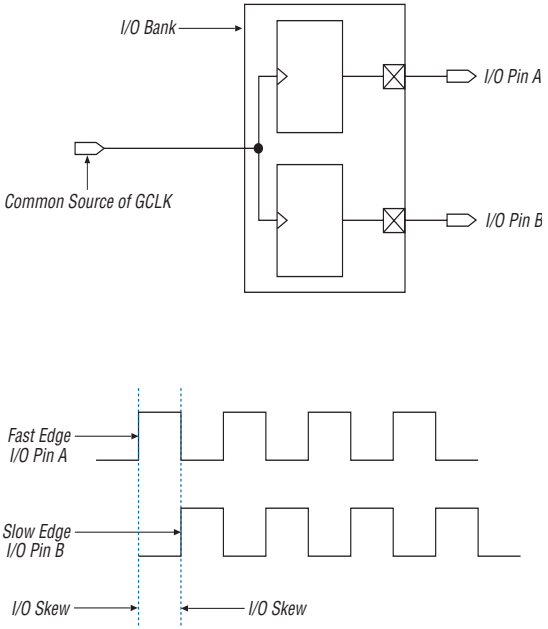


Table 4–102 shows the reporting methodology used by the Quartus II software for minimum timing information for output pins.

*Table 4–102. Reporting Methodology For Minimum Timing For Single-Ended Output Pins (Part 1 of 2)*
*Notes (1), (2), (3)*

| I/O Standard | Loading and Termination | | | | | | | Measurement Point |
|---|---|---|---|---|---|---|---|---|
| | $R_{UP}$ Ω | $R_{DN}$ Ω | $R_S$ Ω | $R_T$ Ω | $V_{CCIO}$ (V) | VTT (V) | $C_L$ (pF) | $V_{MEAS}$ |
| 3.3-V LVTTL | – | – | 0 | – | 3.600 | 3.600 | 10 | 1.800 |
| 2.5-V LVTTL | – | – | 0 | – | 2.630 | 2.630 | 10 | 1.200 |
| 1.8-V LVTTL | – | – | 0 | – | 1.950 | 1.950 | 10 | 0.880 |
| 1.5-V LVTTL | – | – | 0 | – | 1.600 | 1.600 | 10 | 0.750 |
| 3.3-V LVCMOS | – | – | 0 | – | 3.600 | 3.600 | 10 | 1.800 |
| 2.5-V LVCMOS | – | – | 0 | – | 2.630 | 2.630 | 10 | 1.200 |
| 1.8-V LVCMOS | – | – | 0 | – | 1.950 | 1.950 | 10 | 0.880 |
| 1.5-V LVCMOS | – | – | 0 | – | 1.600 | 1.600 | 10 | 0.750 |
| 3.3-V GTL | – | – | 0 | 25 | 3.600 | 1.260 | 30 | 0.860 |
| 2.5-V GTL | – | – | 0 | 25 | 2.630 | 1.260 | 30 | 0.860 |
| 3.3-V GTL+ | – | – | 0 | 25 | 3.600 | 1.650 | 30 | 1.120 |
| 2.5-V GTL+ | – | – | 0 | 25 | 2.630 | 1.650 | 30 | 1.120 |
| 3.3-V SSTL-3 Class II | – | – | 25 | 25 | 3.600 | 1.750 | 30 | 1.750 |
| 3.3-V SSTL-3 Class I | – | – | 25 | 50 | 3.600 | 1.750 | 30 | 1.750 |
| 2.5-V SSTL-2 Class II | – | – | 25 | 25 | 2.630 | 1.390 | 30 | 1.390 |
| 2.5-V SSTL-2 Class I | – | – | 25 | 50 | 2.630 | 1.390 | 30 | 1.390 |
| 1.8-V SSTL-18 Class II | – | – | 25 | 25 | 1.950 | 1.040 | 30 | 1.040 |
| 1.8-V SSTL-18 Class I | – | – | 25 | 50 | 1.950 | 1.040 | 30 | 1.040 |
| 1.5-V HSTL Class II | – | – | 0 | 25 | 1.600 | 0.800 | 20 | 0.900 |
| 1.5-V HSTL Class I | – | – | 0 | 50 | 1.600 | 0.800 | 20 | 0.900 |
| 1.8-V HSTL Class II | – | – | 0 | 25 | 1.950 | 0.900 | 20 | 1.000 |
| 1.8-V HSTL Class I | – | – | 0 | 50 | 1.950 | 0.900 | 20 | 1.000 |
| 3.3-V PCI *(4)* | –/25 | 25/– | 0 | – | 3.600 | 1.950 | 10 | 1.026/2.214 |
| 3.3-V PCI-X 1.0 *(4)* | –/25 | 25/– | 0 | – | 3.600 | 1.950 | 10 | 1.026/2.214 |
| 3.3-V Compact PCI *(4)* | –/25 | 25/– | 0 | – | 3.600 | 3.600 | 10 | 1.026/2.214 |
| 3.3-V AGP 1× *(4)* | –/25 | 25/– | 0 | – | 3.600 | 3.600 | 10 | 1.026/2.214 |

## External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density. All of the timing parameters in this section apply to both flip-chip and wire-bond packages.

Tables 4–103 and 4–104 show the input adder delays associated with column and row I/O pins. If an I/O standard is selected other than 3.3-V LVTTL or LVCMOS, add the selected delay to the external $t_{INSU}$ and $t_{INSUPLL}$ I/O parameters shown in Tables 4–54 through 4–96.

*Table 4–103. Stratix I/O Standard Column Pin Input Delay Adders*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVCMOS | | 0 | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | | 0 | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | | 19 | | 19 | | 22 | | 26 | ps |
| 1.8-V LVTTL | | 221 | | 232 | | 266 | | 313 | ps |
| 1.5-V LVTTL | | 352 | | 369 | | 425 | | 500 | ps |
| GTL | | –45 | | –48 | | –55 | | –64 | ps |
| GTL+ | | –75 | | –79 | | –91 | | –107 | ps |
| 3.3-V PCI | | 0 | | 0 | | 0 | | 0 | ps |
| 3.3-V PCI-X 1.0 | | 0 | | 0 | | 0 | | 0 | ps |
| Compact PCI | | 0 | | 0 | | 0 | | 0 | ps |
| AGP 1× | | 0 | | 0 | | 0 | | 0 | ps |
| AGP 2× | | 0 | | 0 | | 0 | | 0 | ps |
| CTT | | 120 | | 126 | | 144 | | 170 | ps |
| SSTL-3 Class I | | –162 | | –171 | | –196 | | –231 | ps |
| SSTL-3 Class II | | –162 | | –171 | | –196 | | –231 | ps |
| SSTL-2 Class I | | –202 | | –213 | | –244 | | –287 | ps |
| SSTL-2 Class II | | –202 | | –213 | | –244 | | –287 | ps |
| SSTL-18 Class I | | 78 | | 81 | | 94 | | 110 | ps |
| SSTL-18 Class II | | 78 | | 81 | | 94 | | 110 | ps |
| 1.5-V HSTL Class I | | –76 | | –80 | | –92 | | –108 | ps |
| 1.5-V HSTL Class II | | –76 | | –80 | | –92 | | –108 | ps |
| 1.8-V HSTL Class I | | –52 | | –55 | | –63 | | –74 | ps |
| 1.8-V HSTL Class II | | –52 | | –55 | | –63 | | –74 | ps |

*Table 4–105. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2)*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| CTT | | 973 | | 1,021 | | 1,021 | | 1,021 | ps |
| SSTL-3 Class I | | 719 | | 755 | | 755 | | 755 | ps |
| SSTL-3 Class II | | 146 | | 153 | | 153 | | 153 | ps |
| SSTL-2 Class I | | 678 | | 712 | | 712 | | 712 | ps |
| SSTL-2 Class II | | 223 | | 234 | | 234 | | 234 | ps |
| SSTL-18 Class I | | 1,032 | | 1,083 | | 1,083 | | 1,083 | ps |
| SSTL-18 Class II | | 447 | | 469 | | 469 | | 469 | ps |
| 1.5-V HSTL Class I | | 660 | | 693 | | 693 | | 693 | ps |
| 1.5-V HSTL Class II | | 537 | | 564 | | 564 | | 564 | ps |
| 1.8-V HSTL Class I | | 304 | | 319 | | 319 | | 319 | ps |
| 1.8-V HSTL Class II | | 231 | | 242 | | 242 | | 242 | ps |

*Table 4–106. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2)*

| Parameter | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVCMOS | 2 mA | | 1,518 | | 1,594 | | 1,594 | | 1,594 | ps |
| | 4 mA | | 746 | | 783 | | 783 | | 783 | ps |
| | 8 mA | | 96 | | 100 | | 100 | | 100 | ps |
| | 12 mA | | 0 | | 0 | | 0 | | 0 | ps |
| 3.3-V LVTTL | 4 mA | | 1,518 | | 1,594 | | 1,594 | | 1,594 | ps |
| | 8 mA | | 1,038 | | 1,090 | | 1,090 | | 1,090 | ps |
| | 12 mA | | 521 | | 547 | | 547 | | 547 | ps |
| | 16 mA | | 414 | | 434 | | 434 | | 434 | ps |
| | 24 mA | | 0 | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | 2 mA | | 2,032 | | 2,133 | | 2,133 | | 2,133 | ps |
| | 8 mA | | 699 | | 734 | | 734 | | 734 | ps |
| | 12 mA | | 374 | | 392 | | 392 | | 392 | ps |
| | 16 mA | | 165 | | 173 | | 173 | | 173 | ps |
| 1.8-V LVTTL | 2 mA | | 3,714 | | 3,899 | | 3,899 | | 3,899 | ps |
| | 8 mA | | 1,055 | | 1,107 | | 1,107 | | 1,107 | ps |
| | 12 mA | | 830 | | 871 | | 871 | | 871 | ps |

*Table 4–107. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)*

| Parameter | | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTL | 4 mA | | 1,822 | | 1,913 | | 1,913 | | 1,913 | ps |
| | 8 mA | | 1,586 | | 1,665 | | 1,665 | | 1,665 | ps |
| | 12 mA | | 686 | | 720 | | 720 | | 720 | ps |
| | 16 mA | | 630 | | 662 | | 662 | | 662 | ps |
| | 24 mA | | 0 | | 0 | | 0 | | 0 | ps |
| 2.5-V LVTTL | 2 mA | | 2,925 | | 3,071 | | 3,071 | | 3,071 | ps |
| | 8 mA | | 1,496 | | 1,571 | | 1,571 | | 1,571 | ps |
| | 12 mA | | 937 | | 984 | | 984 | | 984 | ps |
| | 16 mA | | 1,003 | | 1,053 | | 1,053 | | 1,053 | ps |
| 1.8-V LVTTL | 2 mA | | 7,101 | | 7,456 | | 7,456 | | 7,456 | ps |
| | 8 mA | | 3,620 | | 3,801 | | 3,801 | | 3,801 | ps |
| | 12 mA | | 3,109 | | 3,265 | | 3,265 | | 3,265 | ps |
| 1.5-V LVTTL | 2 mA | | 10,941 | | 11,488 | | 11,488 | | 11,488 | ps |
| | 4 mA | | 7,431 | | 7,803 | | 7,803 | | 7,803 | ps |
| | 8 mA | | 5,990 | | 6,290 | | 6,290 | | 6,290 | ps |
| GTL | | | –959 | | –1,007 | | –1,007 | | –1,007 | ps |
| GTL+ | | | –438 | | –460 | | –460 | | –460 | ps |
| 3.3-V PCI | | | 660 | | 693 | | 693 | | 693 | ps |
| 3.3-V PCI-X 1.0 | | | 660 | | 693 | | 693 | | 693 | ps |
| Compact PCI | | | 660 | | 693 | | 693 | | 693 | ps |
| AGP 1× | | | 660 | | 693 | | 693 | | 693 | ps |
| AGP 2× | | | 288 | | 303 | | 303 | | 303 | ps |
| CTT | | | 631 | | 663 | | 663 | | 663 | ps |
| SSTL-3 Class I | | | 301 | | 316 | | 316 | | 316 | ps |
| SSTL-3 Class II | | | –359 | | –377 | | –377 | | –377 | ps |
| SSTL-2 Class I | | | 523 | | 549 | | 549 | | 549 | ps |
| SSTL-2 Class II | | | –49 | | –51 | | –51 | | –51 | ps |
| SSTL-18 Class I | | | 2,315 | | 2,431 | | 2,431 | | 2,431 | ps |
| SSTL-18 Class II | | | 723 | | 759 | | 759 | | 759 | ps |
| 1.5-V HSTL Class I | | | 1,687 | | 1,771 | | 1,771 | | 1,771 | ps |
| 1.5-V HSTL Class II | | | 1,095 | | 1,150 | | 1,150 | | 1,150 | ps |
| 1.8-V HSTL Class I | | | 599 | | 629 | | 678 | | 744 | ps |
| 1.8-V HSTL Class II | | | 87 | | 102 | | 102 | | 102 | ps |

*Table 4–118. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[10..7]CLK Pins in Wire-Bond Packages (Part 2 of 2)*

| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
|---|---|---|---|---|
| LVCMOS | 422 | 390 | 390 | MHz |
| GTL+ | 250 | 200 | 200 | MHz |
| SSTL-3 Class I | 350 | 300 | 300 | MHz |
| SSTL-3 Class II | 350 | 300 | 300 | MHz |
| SSTL-2 Class I | 350 | 300 | 300 | MHz |
| SSTL-2 Class II | 350 | 300 | 300 | MHz |
| SSTL-18 Class I | 350 | 300 | 300 | MHz |
| SSTL-18 Class II | 350 | 300 | 300 | MHz |
| 1.5-V HSTL Class I | 350 | 300 | 300 | MHz |
| 1.8-V HSTL Class I | 350 | 300 | 300 | MHz |
| CTT | 250 | 200 | 200 | MHz |
| Differential 1.5-V HSTL C1 | 350 | 300 | 300 | MHz |
| LVPECL *(1)* | 717 | 640 | 640 | MHz |
| PCML *(1)* | 375 | 350 | 350 | MHz |
| LVDS *(1)* | 717 | 640 | 640 | MHz |
| HyperTransport technology *(1)* | 717 | 640 | 640 | MHz |

*Table 4–119. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Wire-Bond Packages (Part 1 of 2)*

| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 422 | 390 | 390 | MHz |
| 2.5 V | 422 | 390 | 390 | MHz |
| 1.8 V | 422 | 390 | 390 | MHz |
| 1.5 V | 422 | 390 | 390 | MHz |
| LVCMOS | 422 | 390 | 390 | MHz |
| GTL+ | 250 | 200 | 200 | MHz |
| SSTL-3 Class I | 350 | 300 | 300 | MHz |
| SSTL-3 Class II | 350 | 300 | 300 | MHz |
| SSTL-2 Class I | 350 | 300 | 300 | MHz |
| SSTL-2 Class II | 350 | 300 | 300 | MHz |

*Table 4–121. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages*

| I/O Standard | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
|---|---|---|---|---|---|
| LVTTL | 400 | 350 | 300 | 300 | MHz |
| 2.5 V | 400 | 350 | 300 | 300 | MHz |
| 1.8 V | 400 | 350 | 300 | 300 | MHz |
| 1.5 V | 350 | 300 | 300 | 300 | MHz |
| LVCMOS | 400 | 350 | 300 | 300 | MHz |
| GTL | 200 | 167 | 125 | 125 | MHz |
| GTL+ | 200 | 167 | 125 | 125 | MHz |
| SSTL-3 Class I | 167 | 150 | 133 | 133 | MHz |
| SSTL-3 Class II | 167 | 150 | 133 | 133 | MHz |
| SSTL-2 Class I | 150 | 133 | 133 | 133 | MHz |
| SSTL-2 Class II | 150 | 133 | 133 | 133 | MHz |
| SSTL-18 Class I | 150 | 133 | 133 | 133 | MHz |
| SSTL-18 Class II | 150 | 133 | 133 | 133 | MHz |
| 1.5-V HSTL Class I | 250 | 225 | 200 | 200 | MHz |
| 1.5-V HSTL Class II | 225 | 225 | 200 | 200 | MHz |
| 1.8-V HSTL Class I | 250 | 225 | 200 | 200 | MHz |
| 1.8-V HSTL Class II | 225 | 225 | 200 | 200 | MHz |
| 3.3-V PCI | 250 | 225 | 200 | 200 | MHz |
| 3.3-V PCI-X 1.0 | 225 | 225 | 200 | 200 | MHz |
| Compact PCI | 400 | 350 | 300 | 300 | MHz |
| AGP 1× | 400 | 350 | 300 | 300 | MHz |
| AGP 2× | 400 | 350 | 300 | 300 | MHz |
| CTT | 300 | 250 | 200 | 200 | MHz |
| LVPECL *(2)* | 717 | 717 | 500 | 500 | MHz |
| PCML *(2)* | 420 | 420 | 420 | 420 | MHz |
| LVDS *(2)* | 717 | 717 | 500 | 500 | MHz |
| HyperTransport technology *(2)* | 420 | 420 | 420 | 420 | MHz |

*Table 4–122. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Wire-Bond Packages (Part 1 of 2)*

| I/O Standard | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Unit |
|---|---|---|---|---|
| LVTTL | 175 | 150 | 150 | MHz |
| 2.5 V | 175 | 150 | 150 | MHz |
| 1.8 V | 175 | 150 | 150 | MHz |
| 1.5 V | 175 | 150 | 150 | MHz |
| LVCMOS | 175 | 150 | 150 | MHz |
| GTL | 125 | 100 | 100 | MHz |
| GTL+ | 125 | 100 | 100 | MHz |
| SSTL-3 Class I | 110 | 90 | 90 | MHz |
| SSTL-3 Class II | 133 | 125 | 125 | MHz |
| SSTL-2 Class I | 166 | 133 | 133 | MHz |
| SSTL-2 Class II | 133 | 100 | 100 | MHz |
| SSTL-18 Class I | 110 | 100 | 100 | MHz |
| SSTL-18 Class II | 110 | 100 | 100 | MHz |
| 1.5-V HSTL Class I | 167 | 167 | 167 | MHz |
| 1.5-V HSTL Class II | 167 | 133 | 133 | MHz |
| 1.8-V HSTL Class I | 167 | 167 | 167 | MHz |
| 1.8-V HSTL Class II | 167 | 133 | 133 | MHz |
| 3.3-V PCI | 167 | 167 | 167 | MHz |
| 3.3-V PCI-X 1.0 | 167 | 133 | 133 | MHz |
| Compact PCI | 175 | 150 | 150 | MHz |
| AGP 1× | 175 | 150 | 150 | MHz |
| AGP 2× | 175 | 150 | 150 | MHz |
| CTT | 125 | 100 | 100 | MHz |
| Differential 1.5-V HSTL C1 | 167 | 133 | 133 | MHz |
| Differential 1.8-V HSTL Class I | 167 | 167 | 167 | MHz |
| Differential 1.8-V HSTL Class II | 167 | 133 | 133 | MHz |
| Differential SSTL-2 *(1)* | 110 | 100 | 100 | MHz |
| LVPECL *(2)* | 311 | 275 | 275 | MHz |
| PCML *(2)* | 250 | 200 | 200 | MHz |

*Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 4 of 4)* Notes (1), (2)

| Symbol | Conditions | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | -8 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{DUTY}$ | LVDS ($J$ = 2 through 10) | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | 47.5 | 50 | 52.5 | % |
| | LVDS ($J$ =1) and LVPECL, PCML, HyperTransport technology | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{LOCK}$ | All | | | 100 | | | 100 | | | 100 | | | 100 | µs |

***Notes to Table 4–125:***

(1) When J = 4, 7, 8, and 10, the SERDES block is used.

(2) When J = 2 or J = 1, the SERDES is bypassed.