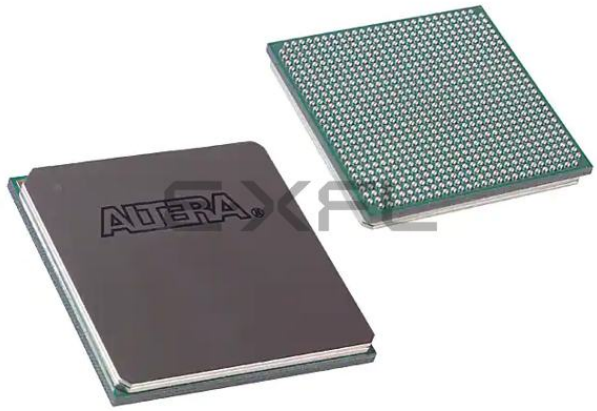


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2566 |
| Number of Logic Elements/Cells | 25660 |
| Total RAM Bits | 1944576 |
| Number of I/O | 597 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 780-BBGA |
| Supplier Device Package | 780-FBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1s25f780c6n |

| Chapter | Date/Version | Changes Made |
|---|---|---|
| 2 | July 2005 v3.2 | • Added "Clear Signals" section.<br>• Updated "Power Sequencing & Hot Socketing" section.<br>• Format changes. |
| | September 2004, v3.1 | • Updated fast regional clock networks description on page 2–73.<br>• Deleted the word preliminary from the "specification for the maximum time to relock is 100 µs" on page 2–90.<br>• Added information about differential SSTL and HSTL outputs in "External Clock Outputs" on page 2–92.<br>• Updated notes in Figure 2–55 on page 2–93.<br>• Added information about *m* counter to "Clock Multiplication & Division" on page 2–101.<br>• Updated Note 1 in Table 2–58 on page 2–101.<br>• Updated description of "Clock Multiplication & Division" on page 2–88.<br>• Updated Table 2–22 on page 2–102.<br>• Added references to AN 349 and AN 329 to "External RAM Interfacing" on page 2–115.<br>• Table 2–25 on page 2–116: updated the table, updated Notes 3 and 4. Notes 4, 5, and 6, are now Notes 5, 6, and 7, respectively.<br>• Updated Table 2–26 on page 2–117.<br>• Added information about PCI Compliance to page 2–120.<br>• Table 2–32 on page 2–126: updated the table and deleted Note 1.<br>• Updated reference to device pin-outs now being available on the web on page 2–130.<br>• Added Notes 4 and 5 to Table 2–36 on page 2–130.<br>• Updated Note 3 in Table 2–37 on page 2–131.<br>• Updated Note 5 in Table 2–41 on page 2–135. |
| | April 2004, v3.0 | • Added note 3 to rows 11 and 12 in Table 2–18.<br>• Deleted "Stratix and Stratix GX Device PLL Availability" table.<br>• Added I/O standards row in Table 2–28 that support max and min strength.<br>• Row `clk [1,3,8,10]` was removed from Table 2–30.<br>• Added checkmarks in Enhanced column for LVPECL, 3.3-V PCML, LVDS, and HyperTransport technology rows in Table 2–32.<br>• Removed the Left and Right I/O Banks row in Table 2–34.<br>• Changed `RCLK` values in Figures 2–50 and 2–51.<br>• External RAM Interfacing section replaced. |
| | November 2003, v2.2 | • Added 672-pin BGA package information in Table 2–37.<br>• Removed support for series and parallel on-chip termination.<br>• Termination Technology renamed differential on-chip termination.<br>• Updated the number of channels per PLL in Tables 2-38 through 2-42.<br>• Updated Figures 2–65 and 2–67. |
| | October 2003, v2.1 | • Updated DDR I information.<br>• Updated Table 2–22.<br>• Added Tables 2–25, 2–29, 2–30, and 2–72.<br>• Updated Figures 2–59, 2–65, and 2–67.<br>• Updated the Lock Detect section. |

Stratix devices are available in space-saving FineLine BGA® and ball-grid array (BGA) packages (see Tables 1–3 through 1–5). All Stratix devices support vertical migration within the same package (for example, you can migrate between the EP1S10, EP1S20, and EP1S25 devices in the 672-pin BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migrational. The Quartus® II software can automatically cross reference and place all pins except differential pins for migration when given a device migration list. You must use the pin-outs for each device to verify the differential placement migration. A future version of the Quartus II software will support differential pin migration.

*Table 1–3. Stratix Package Options & I/O Pin Counts*

| Device | 672-Pin BGA | 956-Pin BGA | 484-Pin FineLine BGA | 672-Pin FineLine BGA | 780-Pin FineLine BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|
| EP1S10 | 345 | | 335 | 345 | 426 | | |
| EP1S20 | 426 | | 361 | 426 | 586 | | |
| EP1S25 | 473 | | | 473 | 597 | 706 | |
| EP1S30 | | 683 | | | 597 | 726 | |
| EP1S40 | | 683 | | | 615 | 773 | 822 |
| EP1S60 | | 683 | | | | 773 | 1,022 |
| EP1S80 | | 683 | | | | 773 | 1,203 |

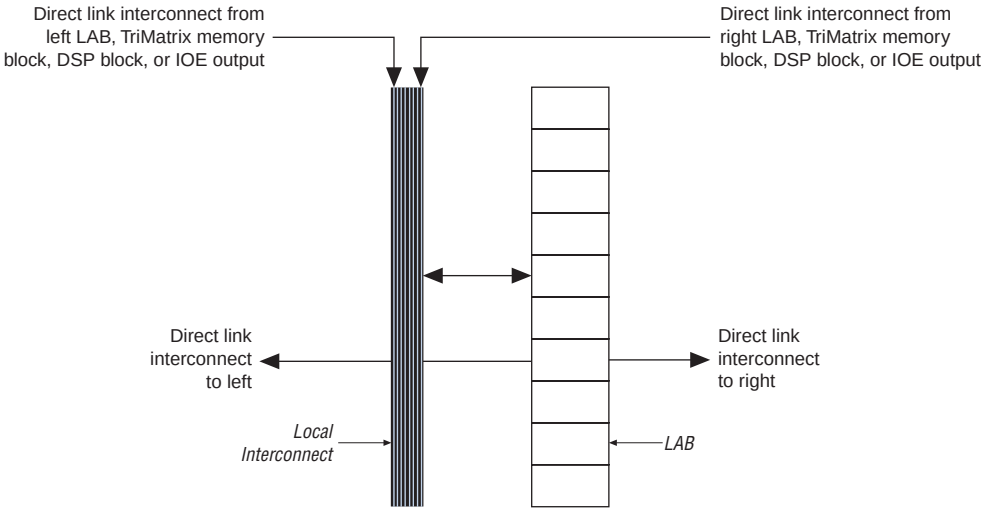
*Note to Table 1–3:*

(1) All I/O pin counts include 20 dedicated clock input pins (`clk[15..0]p`, `clk0n`, `clk2n`, `clk9n`, and `clk11n`) that can be used for data inputs.

*Table 1–4. Stratix BGA Package Sizes*

| Dimension | 672 Pin | 956 Pin |
|---|---|---|
| Pitch (mm) | 1.27 | 1.27 |
| Area (mm²) | 1,225 | 1,600 |
| Length × width (mm × mm) | 35 × 35 | 40 × 40 |

*Figure 2–3. Direct Link Connection*



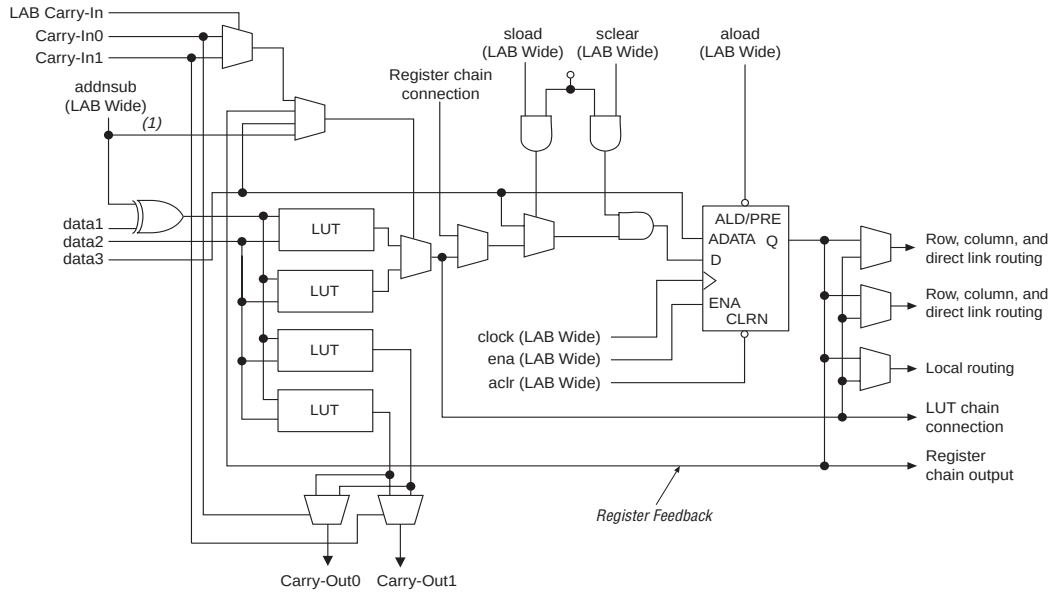

## LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

*Figure 2–7. LE in Dynamic Arithmetic Mode*



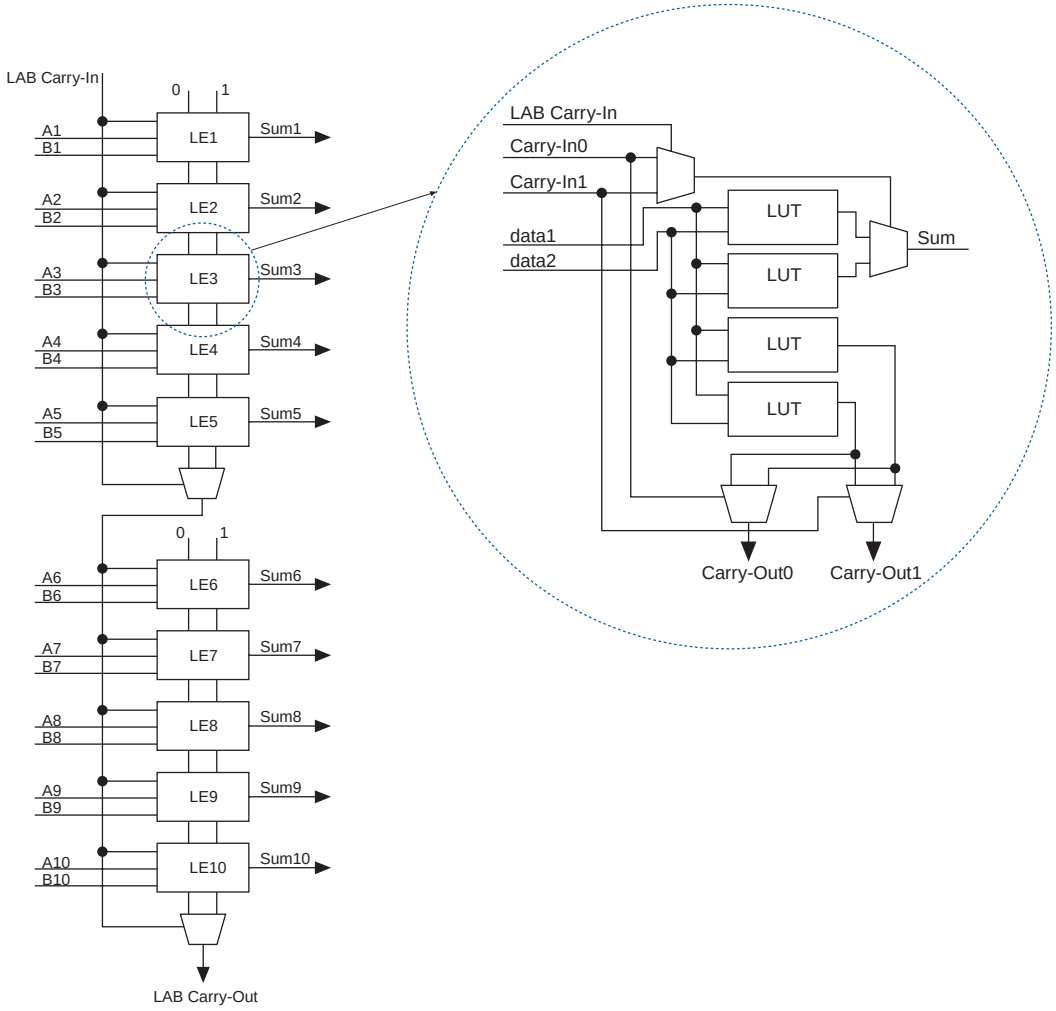

*Note to Figure 2–7:*
(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

### *Carry-Select Chain*

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

*Figure 2–8. Carry Select Chain*

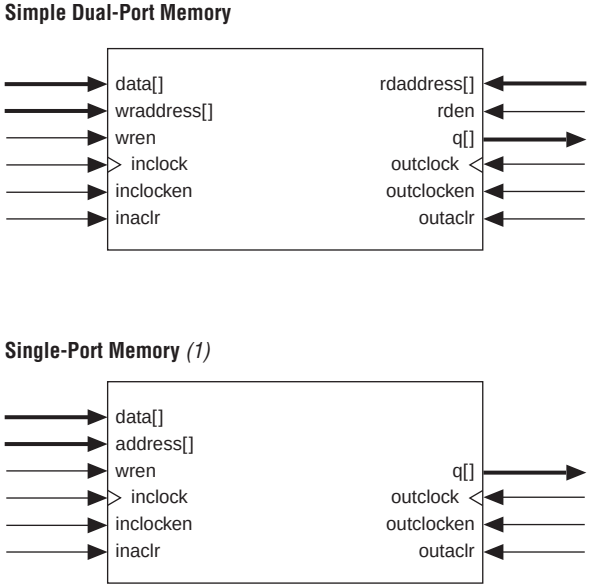



## Clear & Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix devices support simultaneous preset/

In addition to true dual-port memory, the memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write and can either read old data before the write occurs or just read the don't care bits. Single-port memory supports non-simultaneous reads and writes, but the q[] port will output the data once it has been written to the memory (if the outputs are not registered) or after the next rising edge of the clock (if the outputs are registered). For more information, see Chapter 2, TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2*. Figure 2–13 shows these different RAM memory port configurations for TriMatrix memory.

***Figure 2–13. Simple Dual-Port & Single-Port Memory Configurations***




***Note to Figure 2–13:***

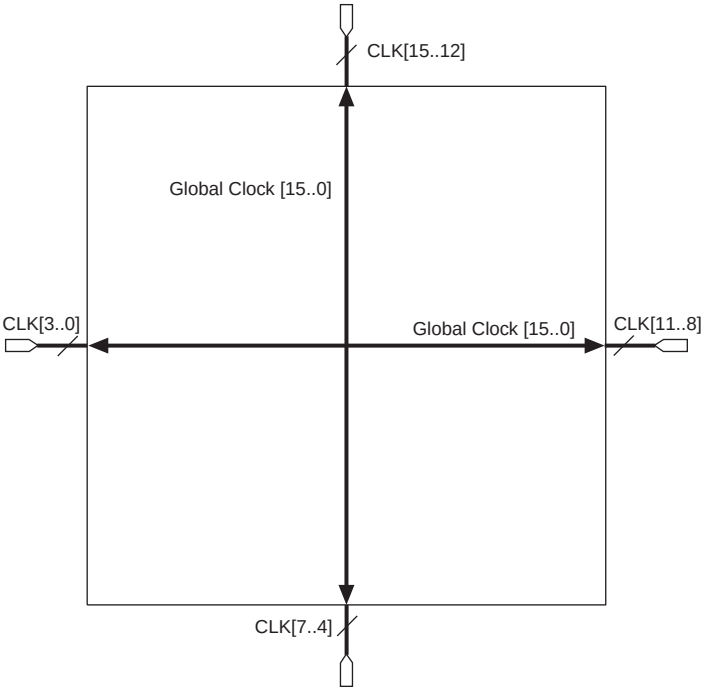
(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

### Read/Write Clock Mode

The memory blocks implement read/write clock mode for simple dual-port memory. You can use up to two clocks in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 2–27 shows a memory block in read/write clock mode.

*Figure 2–42. Global Clocking Note (1)*




*Note to Figure 2–42:*

(1) The corner fast PLLs can also be driven through the global or regional clock networks. The global or regional clock input to the fast PLL can be driven by an output from another PLL, a pin-driven global or regional clock, or internally-generated global signals.

## Regional Clock Network

There are four regional clock networks within each quadrant of the Stratix device that are driven by the same dedicated CLK[15..0] input pins or from PLL outputs. From a top view of the silicon, RCLK[0..3] are in the top left quadrant, RCLK[8..11] are in the top-right quadrant, RCLK[4..7] are in the bottom-left quadrant, and RCLK[12..15] are in the bottom-right quadrant. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. RCLK cannot be driven by internal logic. The CLK clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 2–43. See Figures 2–50 and 2–51 for RCLK connections from PLLs and CLK pins.

Figure 2–49 shows a top-level diagram of the Stratix device and PLL floorplan.

*Figure 2–49. PLL Locations*

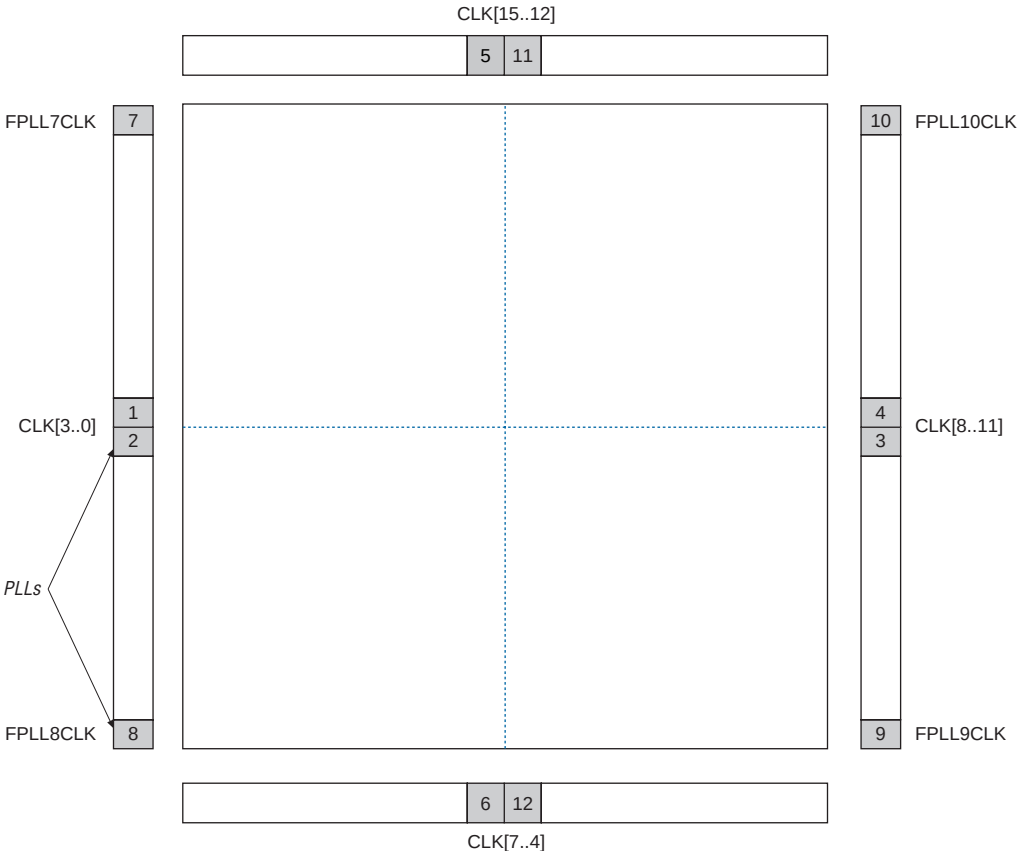


*Table 2–27. DQS & DQ Bus Mode Support (Part 2 of 2)* Note (1)

| Device | Package | Number of ×8 Groups | Number of ×16 Groups | Number of ×32 Groups |
|---|---|---|---|---|
| EP1S25 | 672-pin BGA<br>672-pin FineLine BGA | 16 (3) | 8 | 4 |
| | 780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S30 | 956-pin BGA<br>780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S40 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S60 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S80 | 956-pin BGA<br>1,508-pin FineLine BGA<br>1,923-pin FineLine BGA | 20 | 8 | 4 |

*Notes to Table 2–27:*

(1) See the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2* for $V_{REF}$ guidelines.
(2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.
(3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.
(4) This package has nine groups in I/O banks 3 and 4 and nine groups in I/O banks 7 and 8.
(5) These packages have three groups in I/O banks 3 and 4 and four groups in I/O banks 7 and 8.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Two separate single phase-shifting reference circuits are located on the top and bottom of the Stratix device. Each circuit is driven by a system reference clock through the `CLK` pins that is the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase-shift circuitry on the bottom of the device. The phase-shifting reference circuit on the top of the device controls the compensated delay elements for all 10 DQS pins located at the top of the device. The phase-shifting reference circuit on the bottom of the device controls the compensated delay elements for all 10 DQS pins located on the bottom of the device. All 10 delay elements (DQS signals) on either the top or bottom of the device

- 1.8-V HSTL Class I and II
- SSTL-3 Class I and II
- SSTL-2 Class I and II
- SSTL-18 Class I and II
- CTT

Table 2–31 describes the I/O standards supported by Stratix devices.

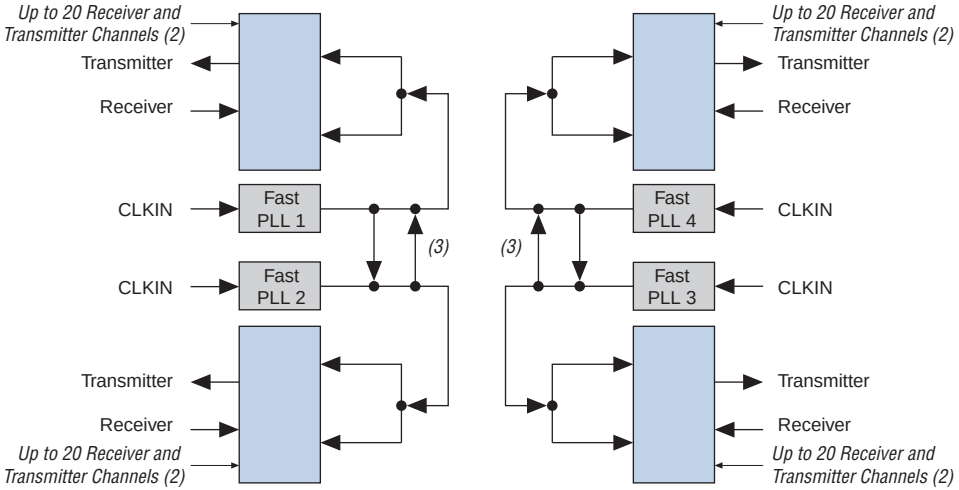
*Table 2–31. Stratix Supported I/O Standards*

| I/O Standard | Type | Input Reference Voltage ($V_{REF}$) (V) | Output Supply Voltage ($V_{CCIO}$) (V) | Board Termination Voltage ($V_{TT}$) (V) |
|---|---|---|---|---|
| LVTTL | Single-ended | N/A | 3.3 | N/A |
| LVCMOS | Single-ended | N/A | 3.3 | N/A |
| 2.5 V | Single-ended | N/A | 2.5 | N/A |
| 1.8 V | Single-ended | N/A | 1.8 | N/A |
| 1.5 V | Single-ended | N/A | 1.5 | N/A |
| 3.3-V PCI | Single-ended | N/A | 3.3 | N/A |
| 3.3-V PCI-X 1.0 | Single-ended | N/A | 3.3 | N/A |
| LVDS | Differential | N/A | 3.3 | N/A |
| LVPECL | Differential | N/A | 3.3 | N/A |
| 3.3-V PCML | Differential | N/A | 3.3 | N/A |
| HyperTransport | Differential | N/A | 2.5 | N/A |
| Differential HSTL *(1)* | Differential | 0.75 | 1.5 | 0.75 |
| Differential SSTL *(2)* | Differential | 1.25 | 2.5 | 1.25 |
| GTL | Voltage-referenced | 0.8 | N/A | 1.20 |
| GTL+ | Voltage-referenced | 1.0 | N/A | 1.5 |
| 1.5-V HSTL Class I and II | Voltage-referenced | 0.75 | 1.5 | 0.75 |
| 1.8-V HSTL Class I and II | Voltage-referenced | 0.9 | 1.8 | 0.9 |
| SSTL-18 Class I and II | Voltage-referenced | 0.90 | 1.8 | 0.90 |
| SSTL-2 Class I and II | Voltage-referenced | 1.25 | 2.5 | 1.25 |
| SSTL-3 Class I and II | Voltage-referenced | 1.5 | 3.3 | 1.5 |
| AGP (1× and 2°) | Voltage-referenced | 1.32 | 3.3 | N/A |
| CTT | Voltage-referenced | 1.5 | 3.3 | 1.5 |

*Notes to Table 2–31:*
(1) This I/O standard is only available on input and output clock pins.
(2) This I/O standard is only available on output column clock pins.

The Quartus II MegaWizard® Plug-In Manager only allows the implementation of up to 20 receiver or 20 transmitter channels for each fast PLL. These channels operate at up to 840 Mbps. The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–74 shows the fast PLL and channel layout in EP1S10, EP1S20, and EP1S25 devices. Figure 2–75 shows the fast PLL and channel layout in the EP1S30 to EP1S80 devices.

***Figure 2–74. Fast PLL & Channel Layout in the EP1S10, EP1S20 or EP1S25 Devices*** *Note (1)*




*Notes to Figure 2–74:*

(1) Wire-bond packages support up to 624 Mbps.

(2) See Table 2–41 for the number of channels each device supports.

(3) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant, those clocked channels support up to 840 Mbps for "high" speed channels and 462 Mbps for "low" speed channels, as labeled in the device pin-outs at **www.altera.com**.

*Table 3–1. Stratix JTAG Instructions*

| JTAG Instruction | Instruction Code | Description |
|---|---|---|
| SAMPLE/PRELOAD | 00 0000 0101 | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer. |
| EXTEST *(1)* | 00 0000 0000 | Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | 11 1111 1111 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| USERCODE | 00 0000 0111 | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | 00 0000 0110 | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| HIGHZ *(1)* | 00 0000 1011 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins. |
| CLAMP *(1)* | 00 0000 1010 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |
| ICR instructions | | Used when configuring an Stratix device via the JTAG port with a MasterBlaster™, ByteBlasterMV™, or ByteBlaster™ II download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor or JRunner. |
| PULSE_NCONFIG | 00 0000 0001 | Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected. |
| CONFIG_IO | 00 0000 1101 | Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction will hold nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured. |
| SignalTap II instructions | | Monitors internal device operation with the SignalTap II embedded logic analyzer. |

***Note to Table 3–1:***

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

*Table 4–2. Stratix Device Recommended Operating Conditions (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4)*, *(5)* | 3.00 (3.135) | 3.60 (3.465) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4)* | 2.375 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | *(4)* | 1.71 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | *(4)* | 1.4 | 1.6 | V |
| $V_I$ | Input voltage | *(3)*, *(6)* | –0.5 | 4.0 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | 85 | °C |
| | | For industrial use | –40 | 100 | °C |

*Table 4–3. Stratix Device DC Operating Conditions Note (7) (Part 1 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I = V_{CCIOmax}$ to 0 V *(8)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O = V_{CCIOmax}$ to 0 V *(8)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All memory blocks in power-down mode) | $V_I$ = ground, no load, no toggling inputs | | | | mA |
| | | EP1S10. $V_I$ = ground, no load, no toggling inputs | | 37 | | mA |
| | | EP1S20. $V_I$ = ground, no load, no toggling inputs | | 65 | | mA |
| | | EP1S25. $V_I$ = ground, no load, no toggling inputs | | 90 | | mA |
| | | EP1S30. $V_I$ = ground, no load, no toggling inputs | | 114 | | mA |
| | | EP1S40. $V_I$ = ground, no load, no toggling inputs | | 145 | | mA |
| | | EP1S60. $V_I$ = ground, no load, no toggling inputs | | 200 | | mA |
| | | EP1S80. $V_I$ = ground, no load, no toggling inputs | | 277 | | mA |

*Table 4–36. Stratix Performance (Part 2 of 2)* Notes (1), (2)

| Applications | | Resources Used | | | Performance | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | LEs | TriMatrix Memory Blocks | DSP Blocks | -5 Speed Grade | -6 Speed Grade | -7 Speed Grade | -8 Speed Grade | Units |
| TriMatrix memory M-RAM block | True dual-port RAM 16K × 36 bit | 0 | 1 | 0 | 269.83 | 237.69 | 206.82 | 175.74 | MHz |
| | Single port RAM 32K × 18 bit | 0 | 1 | 0 | 275.86 | 244.55 | 212.76 | 180.83 | MHz |
| | Simple dual-port RAM 32K × 18 bit | 0 | 1 | 0 | 275.86 | 244.55 | 212.76 | 180.83 | MHz |
| | True dual-port RAM 32K × 18 bit | 0 | 1 | 0 | 275.86 | 244.55 | 212.76 | 180.83 | MHz |
| | Single port RAM 64K × 9 bit | 0 | 1 | 0 | 287.85 | 253.29 | 220.36 | 187.26 | MHz |
| | Simple dual-port RAM 64K × 9 bit | 0 | 1 | 0 | 287.85 | 253.29 | 220.36 | 187.26 | MHz |
| | True dual-port RAM 64K × 9 bit | 0 | 1 | 0 | 287.85 | 253.29 | 220.36 | 187.26 | MHz |
| DSP block | 9 × 9-bit multiplier *(3)* | 0 | 0 | 1 | 335.0 | 293.94 | 255.68 | 217.24 | MHz |
| | 18 × 18-bit multiplier *(4)* | 0 | 0 | 1 | 278.78 | 237.41 | 206.52 | 175.50 | MHz |
| | 36 × 36-bit multiplier *(4)* | 0 | 0 | 1 | 148.25 | 134.71 | 117.16 | 99.59 | MHz |
| | 36 × 36-bit multiplier *(5)* | 0 | 0 | 1 | 278.78 | 237.41 | 206.52 | 175.5 | MHz |
| | 18-bit, 4-tap FIR filter | 0 | 0 | 1 | 278.78 | 237.41 | 206.52 | 175.50 | MHz |
| Larger Designs | 8-bit, 16-tap parallel FIR filter | 58 | 0 | 4 | 141.26 | 133.49 | 114.88 | 100.28 | MHz |
| | 8-bit, 1,024-point FFT function | 870 | 5 | 1 | 261.09 | 235.51 | 205.21 | 175.22 | MHz |

*Notes to Table 4–36:*

(1) These design performance numbers were obtained using the Quartus II software.
(2) Numbers not listed will be included in a future version of the data sheet.
(3) This application uses registered inputs and outputs.
(4) This application uses registered multiplier input and output stages within the DSP block.
(5) This application uses registered multiplier input, pipeline, and output stages within the DSP block.

*Table 4–41. M4K Block Internal Timing Microparameter Descriptions (Part 2 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{M4KDATAAH}$ | A port data hold time after clock |
| $t_{M4KADDRASU}$ | A port address setup time before clock |
| $t_{M4KADDRAH}$ | A port address hold time after clock |
| $t_{M4KDATABSU}$ | B port data setup time before clock |
| $t_{M4KDATABH}$ | B port data hold time after clock |
| $t_{M4KADDRBSU}$ | B port address setup time before clock |
| $t_{M4KADDRBH}$ | B port address hold time after clock |
| $t_{M4KDATACO1}$ | Clock-to-output delay when using output registers |
| $t_{M4KDATACO2}$ | Clock-to-output delay without output registers |
| $t_{M4KCLKHL}$ | Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown inTable 4–36 on page 4–20 and as reported by the timing analyzer in the Quartus II software. |
| $t_{M4KCLR}$ | Minimum clear pulse width |

*Table 4–42. M-RAM Block Internal Timing Microparameter Descriptions (Part 1 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{MRAMRC}$ | Synchronous read cycle time |
| $t_{MRAMWC}$ | Synchronous write cycle time |
| $t_{MRAMWERESU}$ | Write or read enable setup time before clock |
| $t_{MRAMWEREH}$ | Write or read enable hold time after clock |
| $t_{MRAMCLKENSU}$ | Clock enable setup time before clock |
| $t_{MRAMCLKENH}$ | Clock enable hold time after clock |
| $t_{MRAMBESU}$ | Byte enable setup time before clock |
| $t_{MRAMBEH}$ | Byte enable hold time after clock |
| $t_{MRAMDATAASU}$ | A port data setup time before clock |
| $t_{MRAMDATAAH}$ | A port data hold time after clock |
| $t_{MRAMADDRASU}$ | A port address setup time before clock |
| $t_{MRAMADDRAH}$ | A port address hold time after clock |
| $t_{MRAMDATABSU}$ | B port setup time before clock |

*Table 4–71. EP1S25 External I/O Timing on Row Pins Using Regional Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.793 | | 1.927 | | 2.182 | | 2.542 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.759 | 5.457 | 2.759 | 5.835 | 2.759 | 6.346 | 2.759 | 7.024 | ns |
| $t_{XZ}$ | 2.786 | 5.511 | 2.786 | 5.891 | 2.786 | 6.414 | 2.786 | 7.106 | ns |
| $t_{ZX}$ | 2.786 | 5.511 | 2.786 | 5.891 | 2.786 | 6.414 | 2.786 | 7.106 | ns |
| $t_{INSUPLL}$ | 1.169 | | 1.221 | | 1.373 | | 1.600 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.375 | 2.861 | 1.375 | 2.999 | 1.375 | 3.082 | 1.375 | 3.174 | ns |
| $t_{XZPLL}$ | 1.402 | 2.915 | 1.402 | 3.055 | 1.402 | 3.150 | 1.402 | 3.256 | ns |
| $t_{ZXPLL}$ | 1.402 | 2.915 | 1.402 | 3.055 | 1.402 | 3.150 | 1.402 | 3.256 | ns |

*Table 4–72. EP1S25 External I/O Timing on Row Pins Using Global Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.665 | | 1.779 | | 2.012 | | 2.372 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.834 | 5.585 | 2.834 | 5.983 | 2.834 | 6.516 | 2.834 | 7.194 | ns |
| $t_{XZ}$ | 2.861 | 5.639 | 2.861 | 6.039 | 2.861 | 6.584 | 2.861 | 7.276 | ns |
| $t_{ZX}$ | 2.861 | 5.639 | 2.861 | 6.039 | 2.861 | 6.584 | 2.861 | 7.276 | ns |
| $t_{INSUPLL}$ | 1.538 | | 1.606 | | 1.816 | | 2.121 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.164 | 2.492 | 1.164 | 2.614 | 1.164 | 2.639 | 1.164 | 2.653 | ns |
| $t_{XZPLL}$ | 1.191 | 2.546 | 1.191 | 2.670 | 1.191 | 2.707 | 1.191 | 2.735 | ns |
| $t_{ZXPLL}$ | 1.191 | 2.546 | 1.191 | 2.670 | 1.191 | 2.707 | 1.191 | 2.735 | ns |

*Table 4–93. EP1S80 External I/O Timing on Column Pins Using Global Clock Networks* Note (1)

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 0.884 | | 0.976 | | 1.118 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 3.267 | 6.274 | 3.267 | 6.721 | 3.267 | 7.415 | NA | NA | ns |
| $t_{XZ}$ | 3.207 | 6.148 | 3.207 | 6.589 | 3.207 | 7.291 | NA | NA | ns |
| $t_{ZX}$ | 3.207 | 6.148 | 3.207 | 6.589 | 3.207 | 7.291 | NA | NA | ns |
| $t_{INSUPLL}$ | 0.506 | | 0.656 | | 0.838 | | NA | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCOPLL}$ | 1.635 | 2.805 | 1.635 | 2.809 | 1.635 | 2.828 | NA | NA | ns |
| $t_{XZPLL}$ | 1.575 | 2.679 | 1.575 | 2.677 | 1.575 | 2.704 | NA | NA | ns |
| $t_{ZXPLL}$ | 1.575 | 2.679 | 1.575 | 2.677 | 1.575 | 2.704 | NA | NA | ns |

*Table 4–94. EP1S80 External I/O Timing on Row Pins Using Fast Regional Clock Networks* Note (1)

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.792 | | 2.993 | | 3.386 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 2.619 | 5.235 | 2.619 | 5.609 | 2.619 | 6.086 | NA | NA | ns |
| $t_{XZ}$ | 2.646 | 5.289 | 2.646 | 5.665 | 2.646 | 6.154 | NA | NA | ns |
| $t_{ZX}$ | 2.646 | 5.289 | 2.646 | 5.665 | 2.646 | 6.154 | NA | NA | ns |

Tables 4–125 and 4–126 show the high-speed I/O timing for Stratix devices.

*Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 1 of 4) Notes (1), (2)*

| Symbol | Conditions | -5 Speed Grade | | | -6 Speed Grade | | | -7 Speed Grade | | | -8 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ (Clock frequency) (LVDS, LVPECL, HyperTransport technology) $f_{HSCLK} = f_{HSDR} / W$ | *W* = 4 to 30 (Serdes used) | 10 | | 210 | 10 | | 210 | 10 | | 156 | 10 | | 115.5 | MHz |
| | W = 2 (Serdes bypass) | 50 | | 231 | 50 | | 231 | 50 | | 231 | 50 | | 231 | MHz |
| | W = 2 (Serdes used) | 150 | | 420 | 150 | | 420 | 150 | | 312 | 150 | | 231 | MHz |
| | W = 1 (Serdes bypass) | 100 | | 462 | 100 | | 462 | 100 | | 462 | 100 | | 462 | MHz |
| | W = 1 (Serdes used) | 300 | | 717 | 300 | | 717 | 300 | | 624 | 300 | | 462 | MHz |
| $f_{HSDR}$ Device operation (LVDS, LVPECL, HyperTransport technology) | *J* = 10 | 300 | | 840 | 300 | | 840 | 300 | | 640 | 300 | | 462 | Mbps |
| | *J* = 8 | 300 | | 840 | 300 | | 840 | 300 | | 640 | 300 | | 462 | Mbps |
| | *J* = 7 | 300 | | 840 | 300 | | 840 | 300 | | 640 | 300 | | 462 | Mbps |
| | *J* = 4 | 300 | | 840 | 300 | | 840 | 300 | | 640 | 300 | | 462 | Mbps |
| | *J* = 2 | 100 | | 462 | 100 | | 462 | 100 | | 640 | 100 | | 462 | Mbps |
| | *J* = 1 (LVDS and LVPECL only) | 100 | | 462 | 100 | | 462 | 100 | | 640 | 100 | | 462 | Mbps |

*Table 4–129. Enhanced PLL Specifications for -7 Speed Grade (Part 2 of 2)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |
| $t_{JITTER}$ | Period jitter for external clock output *(6)* | | | ±100 ps for >200-MHz `outclk`<br>±20 mUI for <200-MHz `outclk` | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(5)* | | | 22 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(7)* *(11)* | *(9)* | | 100 | µs |
| $t_{LOCK}$ | Time required to lock from end of device configuration *(11)* | 10 | | 400 | µs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 600 *(8)* | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(10)* | 0.5 | | 0.6 | % |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal | 10 | | | ns |

*Table 4–130. Enhanced PLL Specifications for -8 Speed Grade (Part 1 of 3)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)*, *(2)* | | 480 | MHz |
| $f_{INPFD}$ | Input frequency to PFD | 3 | | 420 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock period jitter | | | ±200 *(3)* | ps |