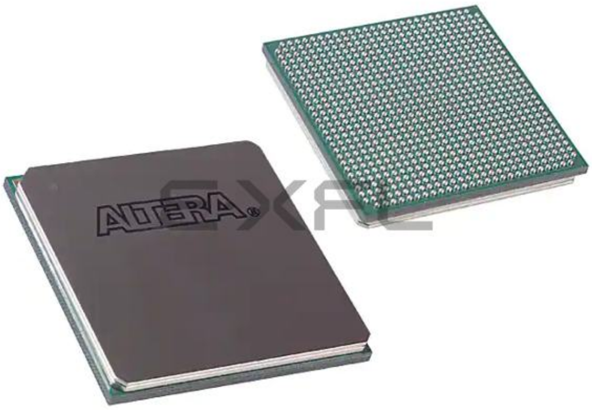

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2566
Number of Logic Elements/Cells	25660
Total RAM Bits	1944576
Number of I/O	597
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s25f780c7n

Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *July 2005*
Part number: *S51001-3.2*

Chapter 2. Stratix Architecture
Revised: *July 2005*
Part number: *S51002-3.2*

Chapter 3. Configuration & Testing
Revised: *July 2005*
Part number: *S51003-1.3*

Chapter 4. DC & Switching Characteristics
Revised: *January 2006*
Part number: *S51004-3.4*

Chapter 5. Reference & Ordering Information
Revised: *September 2004*
Part number: *S51005-2.1*

Chapter	Date/Version	Changes Made
4		• Updated Table 4–123 on page 4–85 through Table 4–126 on page 4–92. • Updated Note 3 in Table 4–123 on page 4–85. • Table 4–125 on page 4–88: moved to correct order in chapter, and updated table. • Updated Table 4–126 on page 4–92. • Updated Table 4–127 on page 4–94. • Updated Table 4–128 on page 4–95.
	April 2004, v3.0	• Table 4–129 on page 4–96: updated table and added Note 10. • Updated Table 4–131 and Table 4–132 on page 4–100. • Updated Table 4–110 on page 4–74. • Updated Table 4–123 on page 4–85. • Updated Table 4–124 on page 4–87. through Table 4–126 on page 4–92. • Added Note 10 to Table 4–129 on page 4–96. • Moved Table 4–127 on page 4–94 to correct order in the chapter. • Updated Table 4–131 on page 4–100 through Table 4–132 on page 4–100. • Deleted t_{XZ} and t_{ZX} from Figure 4–4. • Waveform was added to Figure 4–6. • The minimum and maximum duty cycle values in Note 3 of Table 4–8 were moved to a new Table 4–9. • Changes were made to values in SSTL-3 Class I and II rows in Table 4–17. • Note 1 was added to Table 4–34. • Added t_{SU_R} and t_{SU_C} rows in Table 4–38. • Changed Table 4–55 title from “EP1S10 Column Pin Fast Regional Clock External I/O Timing Parameters” to “EP1S10 External I/O Timing on Column Pins Using Fast Regional Clock Networks.” • Changed values in Tables 4–46, 4–48 to 4–51, 4–128, and 4–131. • Added t_{ARESET} row in Tables 4–127 to 4–132. • Deleted -5 Speed Grade column in Tables 4–117 to 4–119 and 4–122 to 4–123. • Fixed differential waveform in Figure 4–1. • Added “Definition of I/O Skew” section. • Added t_{SU} and t_{CO_C} rows and made changes to values in t_{PRE} and t_{CLKHL} rows in Table 4–46. • Values changed in the t_{SU} and t_H rows in Table 4–47. • Values changed in the $t_{M4KCLKHL}$ row in Table 4–49. • Values changed in the $t_{MRAMCLKHL}$ row in Table 4–50. • Added Table 4–51 to “Internal Timing Parameters” section. • The timing information is preliminary in Tables 4–55 through 4–96. • Table 4–111 was separated into 3 tables: Tables 4–111 to 4–113.
	November 2003, v2.2	• Updated Tables 4–127 through 4–129.

2. Stratix Architecture

S51002-3.2

Functional Description

Stratix® devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device's logic array.

Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

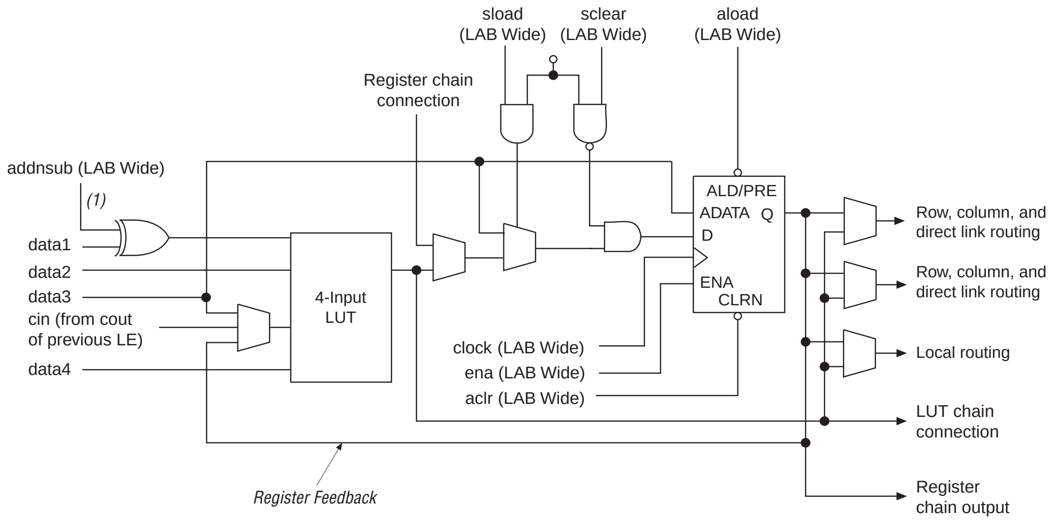
Each Stratix device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with asynchronous preset load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–6). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

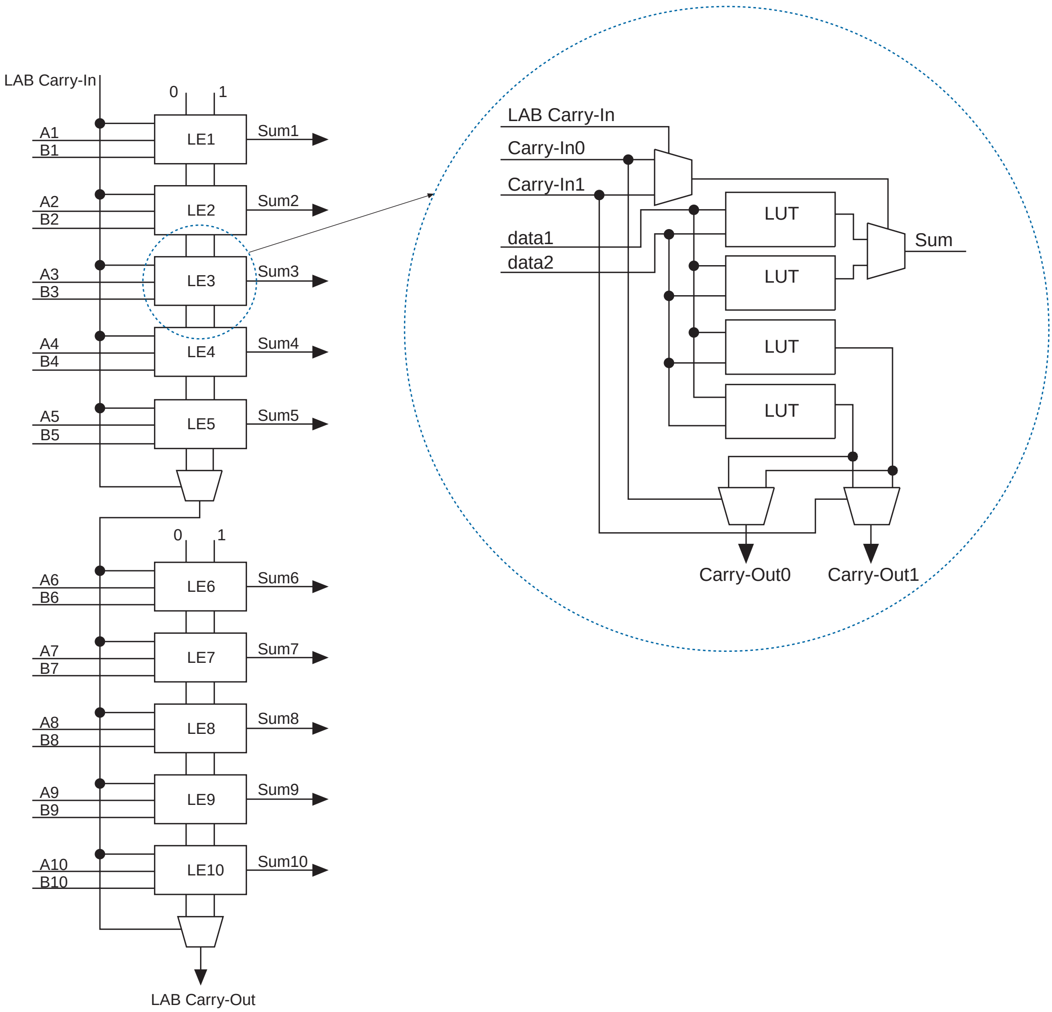
Figure 2–6. LE in Normal Mode



Note to Figure 2–6:

(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Figure 2–8. Carry Select Chain



Clear & Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix devices support simultaneous preset/

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–5 and 2–6 summarize the possible M4K RAM block configurations.

Table 2–5. M4K RAM Block Configurations (Simple Dual-Port)

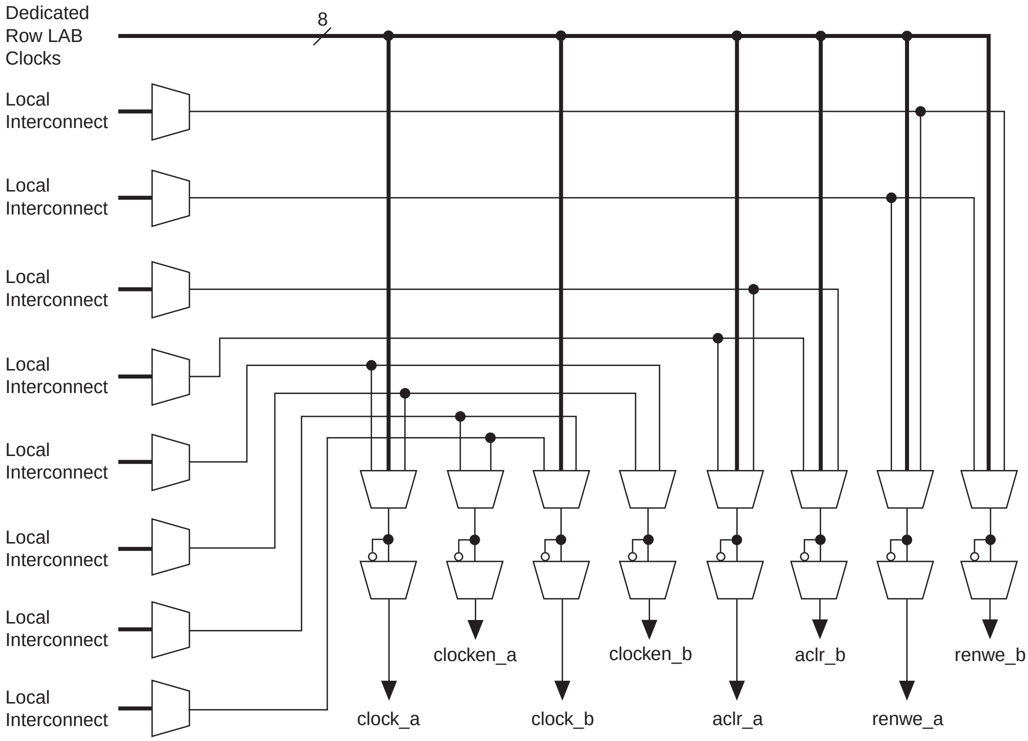
Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

Table 2–6. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Figure 2–19. M-RAM Block Control Signals



One of the M-RAM block's horizontal sides drive the address and control signal (clock, renwe, byteena, etc.) inputs. Typically, the horizontal side closest to the device perimeter contains the interfaces. The one exception is when two M-RAM blocks are paired next to each other. In this case, the side of the M-RAM block opposite the common side of the two blocks contains the input interface. The top and bottom sides of any M-RAM block contain data input and output interfaces to the logic array. The top side has 72 data inputs and 72 data outputs for port B, and the bottom side has another 72 data inputs and 72 data outputs for port A. Figure 2–20 shows an example floorplan for the EP1S60 device and the location of the M-RAM interfaces.

Output Selection Multiplexer

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

Output Registers

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]`. Output registers can be used in any mode.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

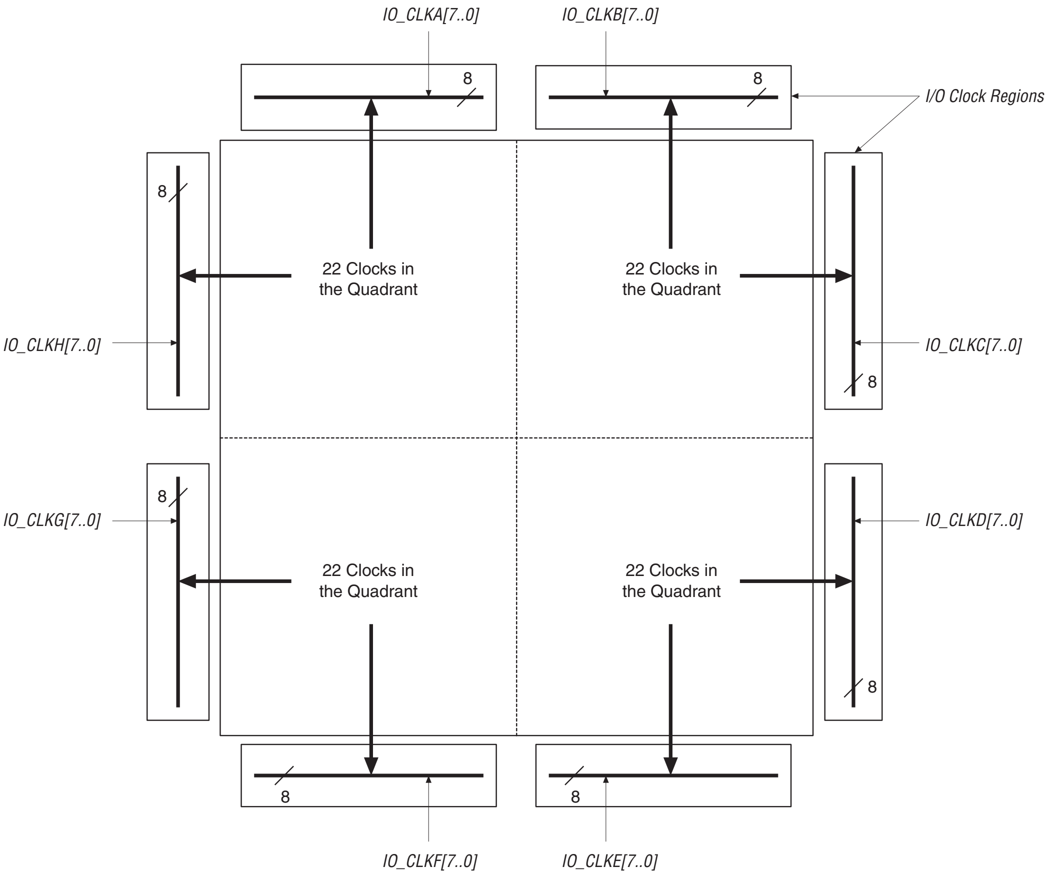
- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

☞ Each DSP block can only support one mode. Mixed modes in the same DSP block is not supported.

Simple Multiplier Mode

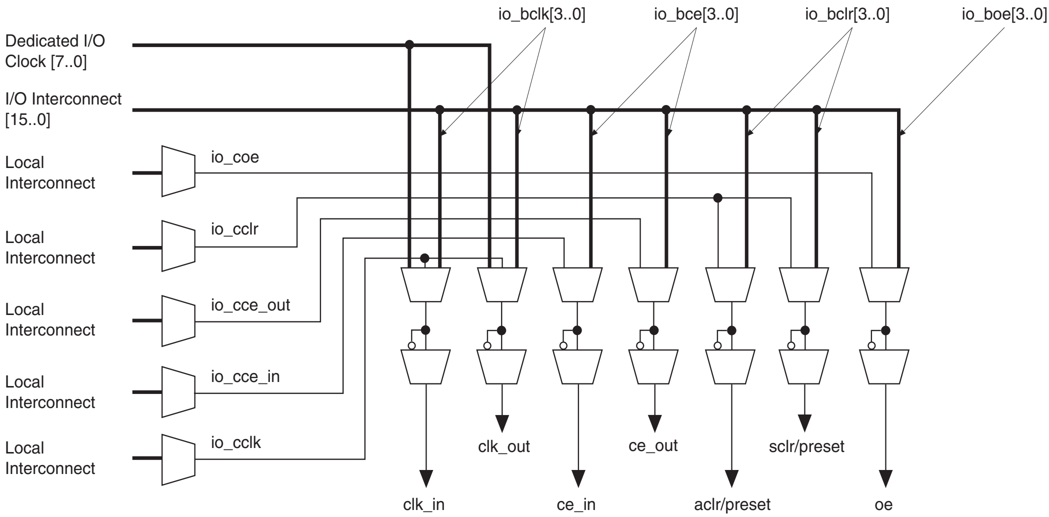
In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18×18-bit multipliers or eight 9×9-bit multipliers can drive their results directly out of one DSP block. See Figure 2–35.

Figure 2–47. EP1S10, EP1S20 & EP1S25 Device I/O Clock Groups



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 2–63 illustrates the control signal selection.

Figure 2–63. Control Signal Selection per IOE



In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–64 shows the IOE in bidirectional configuration.

For more information on I/O standards supported by Stratix devices, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook, Volume 2*.

Stratix devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in Figure 2–70. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in Table 2–31 except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. Table 2–32 shows I/O standard support for each I/O bank.

However, there is additional resistance present between the device ball and the input of the receiver buffer, as shown in Figure 2–72. This resistance is because of package trace resistance (which can be calculated as the resistance from the package ball to the pad) and the parasitic layout metal routing resistance (which is shown between the pad and the intersection of the on-chip termination and input buffer).

Figure 2–72. Differential Resistance of LVDS Differential Pin Pair (R_D)

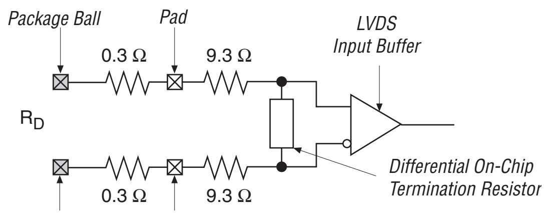


Table 2–35 defines the specification for internal termination resistance for commercial devices.

Table 2–35. Differential On-Chip Termination

Symbol	Description	Conditions	Resistance			Unit
			Min	Typ	Max	
R_D *(2)*	Internal differential termination for LVDS	Commercial *(1)*, *(3)*	110	135	165	W
		Industrial *(2)*, *(3)*	100	135	170	W

Notes to Table 2–35:

(1) Data measured over minimum conditions (T_j = 0 C, V_{CCIO} +5%) and maximum conditions (T_j = 85 C, V_{CCIO} = –5%).

(2) Data measured over minimum conditions (T_j = –40 C, V_{CCIO} +5%) and maximum conditions (T_j = 100 C, V_{CCIO} = –5%).

(3) LVDS data rate is supported for 840 Mbps using internal differential termination.

MultiVolt I/O Interface

The Stratix architecture supports the MultiVolt I/O interface feature, which allows Stratix devices in all packages to interface with systems of different supply voltages.

The Stratix `VCCINT` pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The `VCCIO` pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements.

Figure 3–5. External Temperature-Sensing Diode

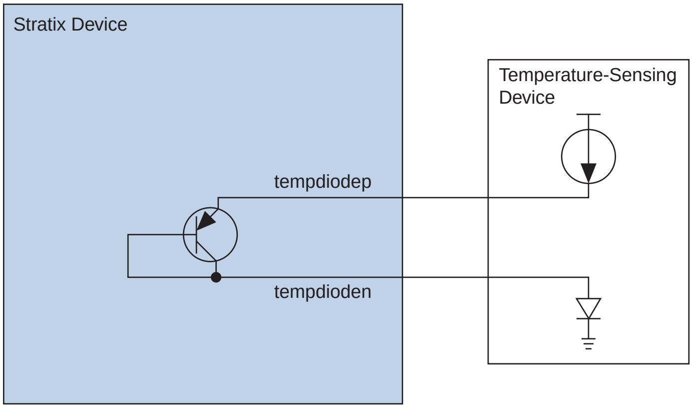


Table 3–6 shows the specifications for bias voltage and current of the Stratix temperature sensing diode.

Table 3–6. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
I_{BIAS} high	80	100	120	µA
I_{BIAS} low	8	10	12	µA
$V_{BP} – V_{BN}$	0.3		0.9	V
V_{BN}		0.7		V
Series resistance			3	W

Table 4–20. SSTL-2 Class I Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.18		3.0	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.35			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(3)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(3)*			V_{TT} – 0.57	V

Table 4–21. SSTL-2 Class II Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.35			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(3)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(3)*			V_{TT} – 0.76	V

Table 4–22. SSTL-3 Class I Specifications (Part 1 of 2)						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.2	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.4			V

Table 4–31. CTT I/O Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		2.05	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ≤V_{OUT} ≤ V_{CCIO}	–10		10	µA

Table 4–32. Bus Hold Parameters										
Parameter	**Conditions**	**V_{CCIO} Level**								**Unit**
		1.5 V		**1.8 V**		**2.5 V**		**3.3 V**		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Low sustaining current	V_{IN} > V_{IL} (maximum)	25		30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)	-25		–30		–50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}		160		200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}		-160		–200		–300		–500	µA
Bus-hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

Table 4–36. Stratix Performance (Part 2 of 2) Notes (1), (2)

Applications		Resources Used			Performance				
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Units
TriMatrix memory M-RAM block	True dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	175.74	MHz
	Single port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Single port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
DSP block	9 × 9-bit multiplier *(3)*	0	0	1	335.0	293.94	255.68	217.24	MHz
	18 × 18-bit multiplier *(4)*	0	0	1	278.78	237.41	206.52	175.50	MHz
	36 × 36-bit multiplier *(4)*	0	0	1	148.25	134.71	117.16	99.59	MHz
	36 × 36-bit multiplier *(5)*	0	0	1	278.78	237.41	206.52	175.5	MHz
	18-bit, 4-tap FIR filter	0	0	1	278.78	237.41	206.52	175.50	MHz
Larger Designs	8-bit, 16-tap parallel FIR filter	58	0	4	141.26	133.49	114.88	100.28	MHz
	8-bit, 1,024-point FFT function	870	5	1	261.09	235.51	205.21	175.22	MHz

Notes to Table 4–36:

(1) These design performance numbers were obtained using the Quartus II software.
(2) Numbers not listed will be included in a future version of the data sheet.
(3) This application uses registered inputs and outputs.
(4) This application uses registered multiplier input and output stages within the DSP block.
(5) This application uses registered multiplier input, pipeline, and output stages within the DSP block.

Table 4–43. Routing Delay Internal Timing Microparameter Descriptions (Part 2 of 2)	
Symbol	**Parameter**
t_{C4}	Delay for a C4 line with average loading; covers a distance of four LAB rows.
t_{C8}	Delay for a C8 line with average loading; covers a distance of eight LAB rows.
t_{C16}	Delay for a C16 line with average loading; covers a distance of 16 LAB rows.
t_{LOCAL}	Local interconnect delay, for connections within a LAB, and for the final routing hop of connections to LABs, DSP blocks, RAM blocks and I/Os.

Table 4–44. LE Internal Timing Microparameters

Parameter	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	10		10		11		13		ps
t_H	100		100		114		135		ps
t_{CO}		156		176		202		238	ps
t_{LUT}		366		459		527		621	ps
t_{CLR}	100		100		114		135		ps
t_{PRE}	100		100		114		135		ps
t_{CLKHL}	1000		1111		1190		1400		ps

Table 4–45. IOE Internal TSU Microparameter by Device Density (Part 1 of 2)

Device	Symbol	-5		-6		-7		-8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
EP1S10	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	176		80		80		80		ps
EP1S20	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	76		80		80		80		ps
EP1S25	t_{SU_R}	276		280		280		280		ps
	t_{SU_C}	276		280		280		280		ps
EP1S30	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	176		180		180		180		ps

Tables 4–61 through 4–66 show the external timing parameters on column and row pins for EP1S20 devices.

Table 4–61. EP1S20 External I/O Timing on Column Pins Using Fast Regional Clock Networks Note (1)									
Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.065		2.245		2.576		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.283	4.622	2.283	4.916	2.283	5.310	NA	NA	ns
t_{XZ}	2.223	4.496	2.223	4.784	2.223	5.186	NA	NA	ns
t_{ZX}	2.223	4.496	2.223	4.784	2.223	5.186	NA	NA	ns

Table 4–62. EP1S20 External I/O Timing on Column Pins Using Regional Clock Networks Note (1)									
Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.541		1.680		1.931		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.597	5.146	2.597	5.481	2.597	5.955	NA	NA	ns
t_{XZ}	2.537	5.020	2.537	5.349	2.537	5.831	NA	NA	ns
t_{ZX}	2.537	5.020	2.537	5.349	2.537	5.831	NA	NA	ns
$t_{INSUPLL}$	0.777		0.818		0.937		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.296	2.690	1.296	2.801	1.296	2.876	NA	NA	ns
t_{XZPLL}	1.236	2.564	1.236	2.669	1.236	2.752	NA	NA	ns
t_{ZXPLL}	1.236	2.564	1.236	2.669	1.236	2.752	NA	NA	ns

Table 4–75. EP1S30 External I/O Timing on Column Pins Using Global Clock Networks (Part 2 of 2)									
Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{XZ}	2.754	5.406	2.754	5.848	2.754	6.412	2.754	7.159	ns
t_{ZX}	2.754	5.406	2.754	5.848	2.754	6.412	2.754	7.159	ns
$t_{INSUPLL}$	1.265		1.236		1.403		1.756		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.068	2.302	1.068	2.483	1.068	2.510	1.068	2.423	ns
t_{XZPLL}	1.008	2.176	1.008	2.351	1.008	2.386	1.008	2.308	ns
t_{ZXPLL}	1.008	2.176	1.008	2.351	1.008	2.386	1.008	2.308	ns

Table 4–76. EP1S30 External I/O Timing on Row Pins Using Fast Regional Clock Networks									
Parameters	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.616		2.808		3.223		3.797		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.542	5.114	2.542	5.502	2.542	5.965	2.542	6.581	ns
t_{XZ}	2.569	5.168	2.569	5.558	2.569	6.033	2.569	6.663	ns
t_{ZX}	2.569	5.168	2.569	5.558	2.569	6.033	2.569	6.663	ns