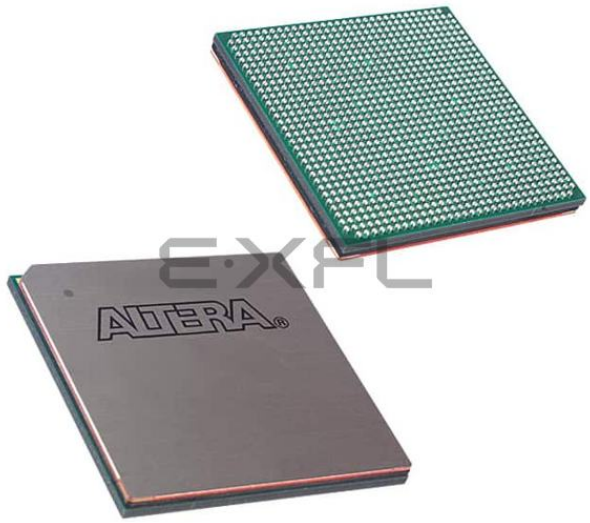

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3247
Number of Logic Elements/Cells	32470
Total RAM Bits	3317184
Number of I/O	726
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s30f1020c6n

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Designs.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

2. Stratix Architecture

S51002-3.2

Functional Description

Stratix® devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device's logic array.

Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with

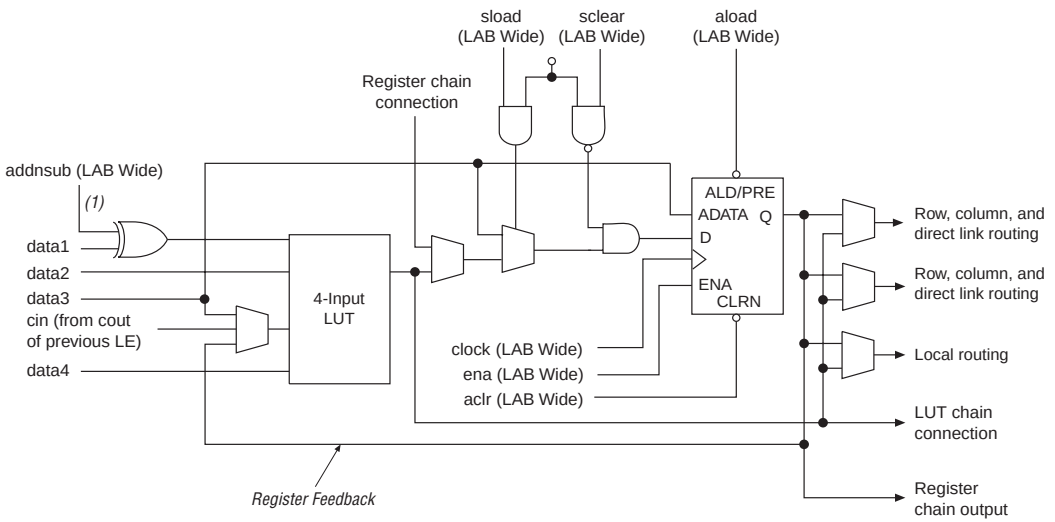
asynchronous preset load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The addnsub control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–6). The Quartus II Compiler automatically selects the carry-in or the data3 signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the data3 input of the LE. LEs in normal mode support packed registers.

Figure 2–6. LE in Normal Mode



Note to Figure 2–6:
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

TriMatrix memory architecture can implement pipelined RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (WREN) signal derived from the global or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM WREN signal while ensuring its data and address signals meet setup and hold time specifications relative to the WREN signal. The output registers can be bypassed. Flow-through reading is possible in the simple dual-port mode of M512 and M4K RAM blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple TriMatrix memory blocks. For example, two 256 × 16-bit RAM blocks can be combined to form a 256 × 32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words available in one memory block. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

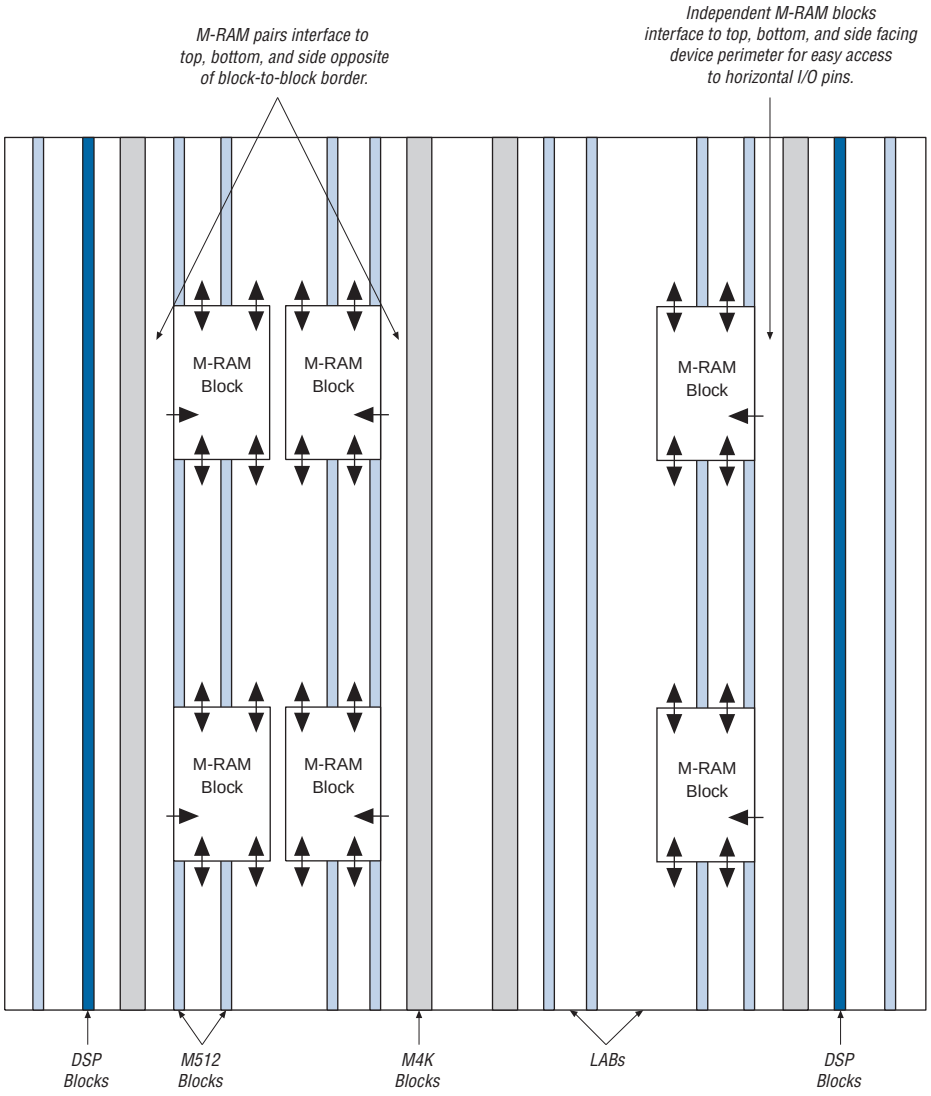
Clear Signals

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

Parity Bit Support

The memory blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. In the M4K and M-RAM blocks, byte enables are also available for data input masking during write operations.

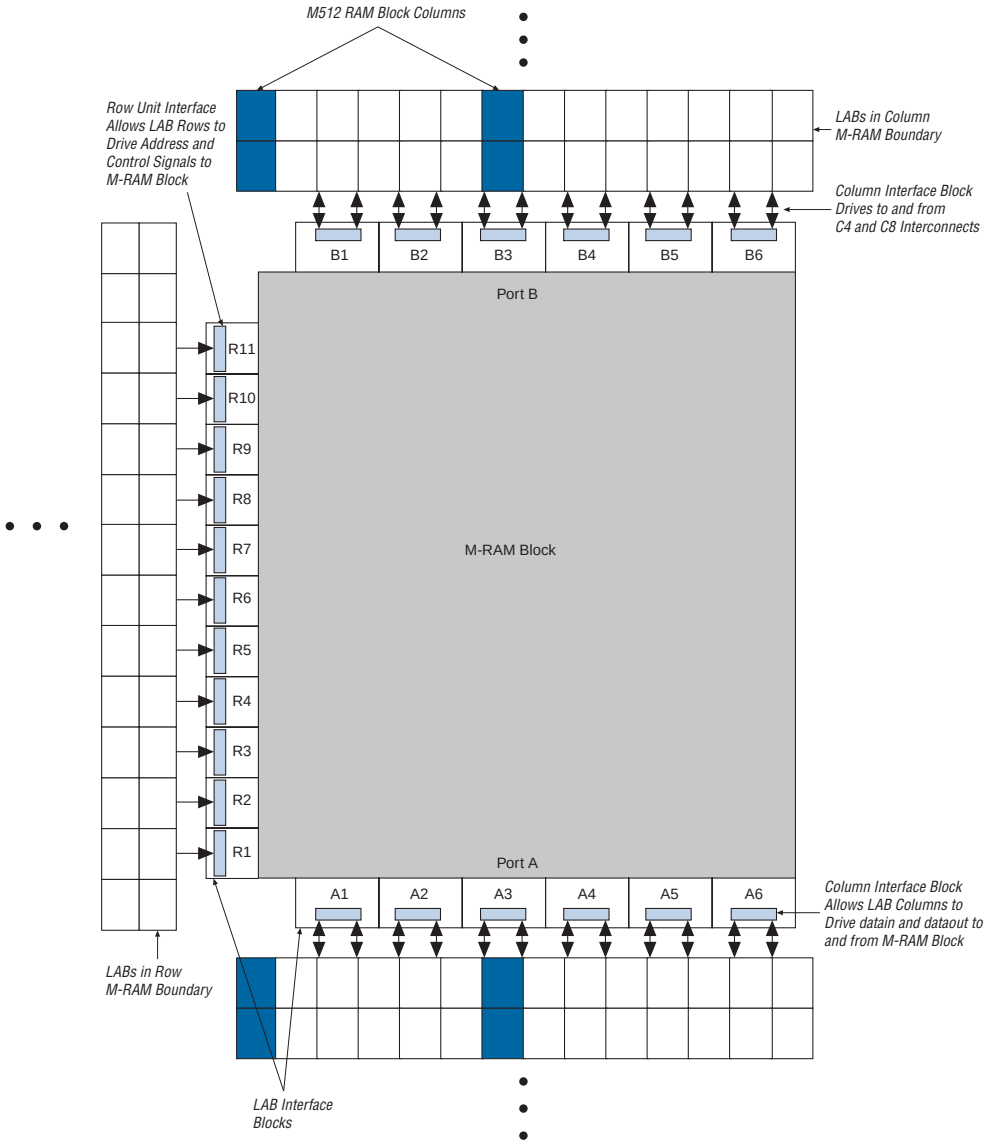
Figure 2–20. EP1S60 Device with M-RAM Interface Locations Note (1)



Note to Figure 2–20:
(1) Device shown is an EP1S60 device. The number and position of M-RAM blocks varies in other devices.

The M-RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. For independent M-RAM blocks, up to 10 direct link address and control signal input connections to the M-RAM block are possible from the left adjacent LABs for M-RAM

Figure 2–21. Left-Facing M-RAM to Interconnect Interface Notes (1), (2)



Notes to Figure 2–21:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

(2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these blocks have the same fundamental building block: the multiplier. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix device has two columns of DSP blocks to efficiently implement DSP functions faster than LE-based implementations. Larger Stratix devices have more DSP blocks per column (see Table 2–13). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any matched sign multiplications (either unsigned by unsigned or signed by signed), but the capabilities for dynamic and mixed sign multiplications are handled differently. The following list provides the largest functions that can fit into a single DSP block.

- 36 × 36-bit unsigned by unsigned multiplication
- 36 × 36-bit signed by signed multiplication
- 35 × 36-bit unsigned by signed multiplication
- 36 × 35-bit signed by unsigned multiplication
- 36 × 35-bit signed by dynamic sign multiplication
- 35 × 36-bit dynamic sign by signed multiplication
- 35 × 36-bit unsigned by dynamic sign multiplication
- 36 × 35-bit dynamic sign by unsigned multiplication
- 35 × 35-bit dynamic sign multiplication when the sign controls for each operand are different
- 36 × 36-bit dynamic sign multiplication when the same sign control is used for both operands

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 2–29 shows one of the columns with surrounding LAB rows.

Figure 2–29. DSP Blocks Arranged in Columns

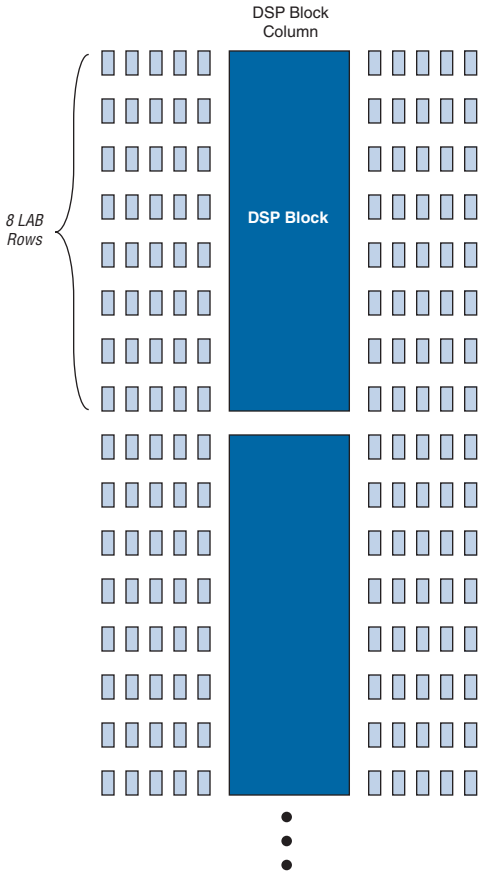
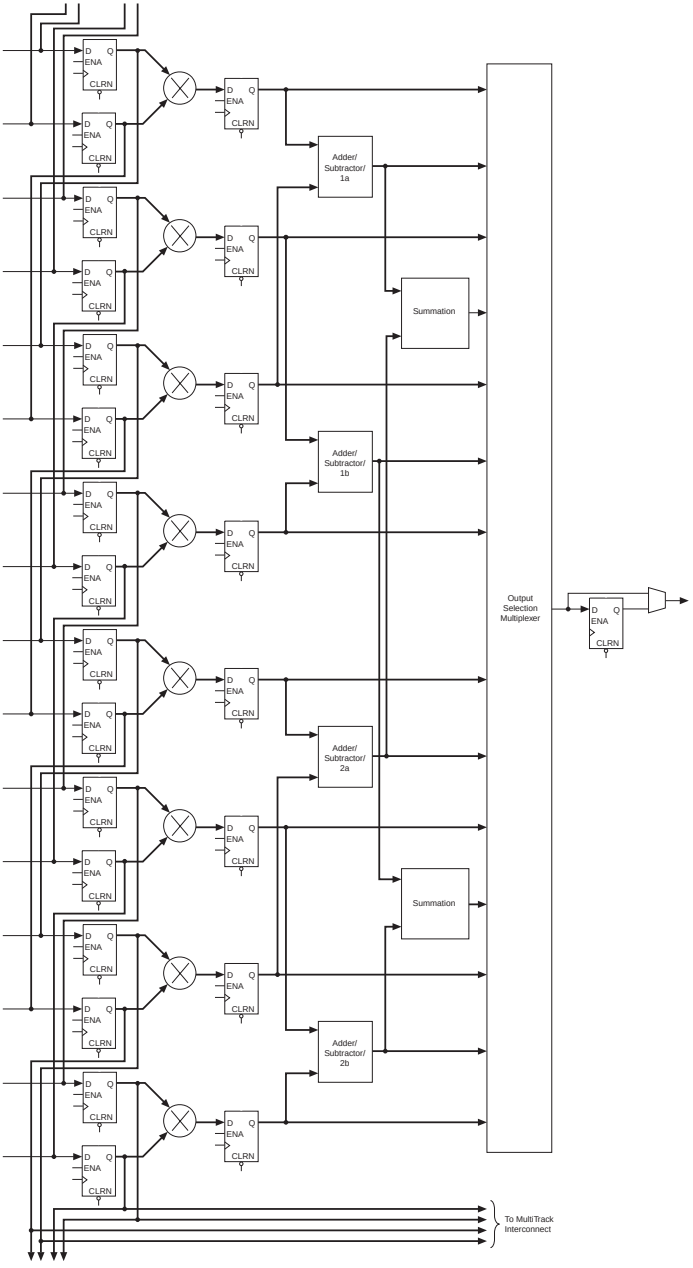


Figure 2–31. DSP Block Diagram for 9 × 9-Bit Configuration



Adder/Subtractor/Accumulator

The adder/subtractor/accumulator is the first level of the adder/output block and can be used as an accumulator or as an adder/subtractor.

Adder/Subtractor
Each adder/subtractor/accumulator block can perform addition or subtraction using the `addnsub` independent control signal for each first-level adder in 18 × 18-bit mode. There are two `addnsub[1..0]` signals available in a DSP block for any configuration. For 9 × 9-bit mode, one `addnsub[1..0]` signal controls the top two one-level adders and another `addnsub[1..0]` signal controls the bottom two one-level adders. A high `addnsub` signal indicates addition, and a low signal indicates subtraction. The `addnsub` control signal can be unregistered or registered once or twice when feeding the adder blocks to match data path pipelines.

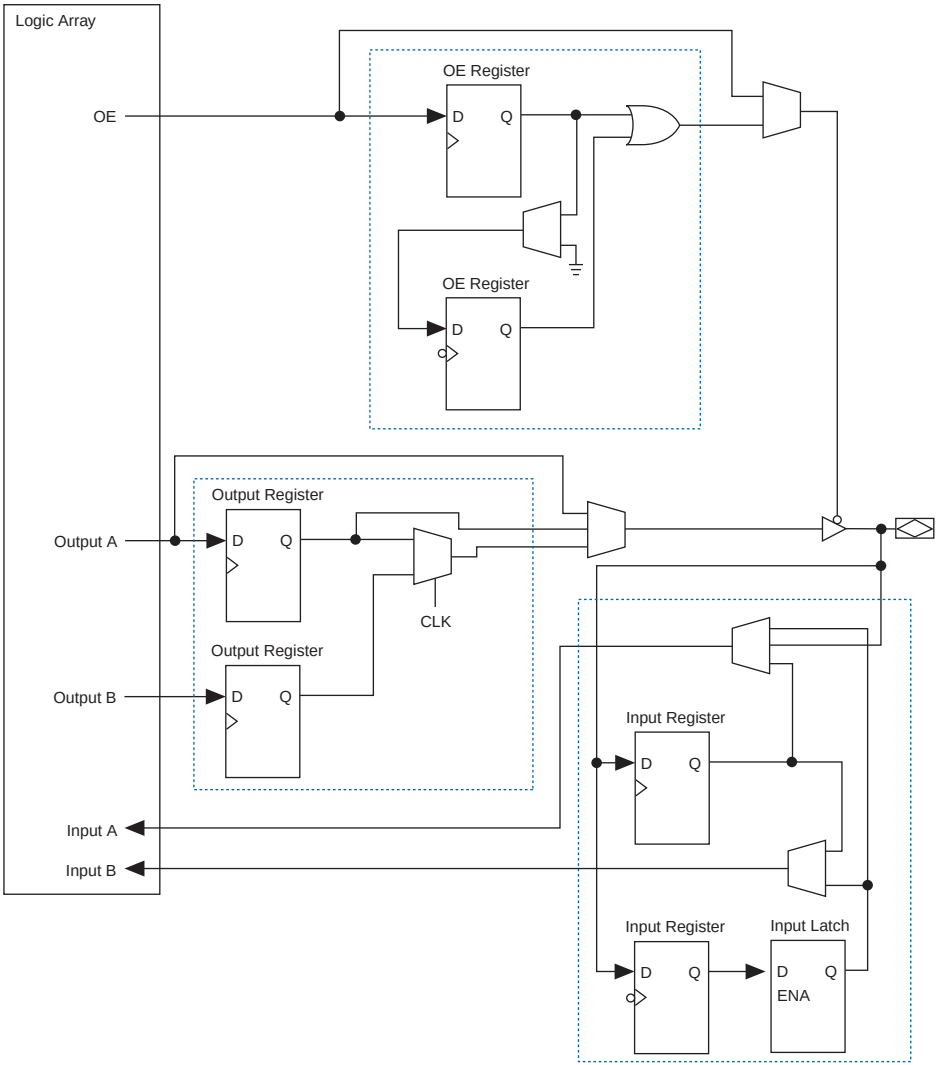
The `signa` and `signb` signals serve the same function as the multiplier block `signa` and `signb` signals. The only difference is that these signals can be registered up to two times. These signals are tied to the same `signa` and `signb` signals from the multiplier and must be connected to the same clocks and control signals.

Accumulator
When configured for accumulation, the adder/output block output feeds back to the accumulator as shown in Figure 2–34. The `accum_sload[1..0]` signal synchronously loads the multiplier result to the accumulator output. This signal can be unregistered or registered once or twice. Additionally, the `overflow` signal indicates the accumulator has overflowed or underflowed in accumulation mode. This signal is always registered and must be externally latched in LEs if the design requires a latched `overflow` signal.

Summation

The output of the adder/subtractor/accumulator block feeds to an optional summation block. This block sums the outputs of the DSP block multipliers. In 9 × 9-bit mode, there are two summation blocks providing the sums of two sets of four 9 × 9-bit multipliers. In 18 × 18-bit mode, there is one summation providing the sum of one set of four 18 × 18-bit multipliers.

Figure 2–59. Stratix IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–60 shows how a row I/O block connects to the logic array. Figure 2–61 shows how a column I/O block connects to the logic array.

I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Bus Hold

Each Stratix device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Table 2–29 shows bus hold support for different pin types.

Table 2–29. Bus Hold Support

Pin Type	Bus Hold
I/O pins	✓
CLK[15..0]	
CLK[0,1,2,3,8,9,10,11]	
FCLK	✓
FPLL[7..10]CLK	

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when using open-drain outputs with the GTL+ I/O standard or when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state. See the *DC & Switching Characteristics* chapter of the *Stratix Device Handbook, Volume 1* for the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix device I/O pin provides an optional programmable pull-up resistor during user mode. If this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the output pin's bank. Table 2–30 shows which pin types support the weak pull-up resistor feature.

Table 2–30. Programmable Weak Pull-Up Resistor Support

Pin Type	Programmable Weak Pull-Up Resistor
I/O pins	✓
CLK[15..0]	
FCLK	✓
FPLL[7..10]CLK	
Configuration pins	
JTAG pins	✓ *(1)*

Note to Table 2–30:
(1) TDO pins do not support programmable weak pull-up resistors.

Advanced I/O Standard Support

Stratix device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP (1× and 2×)
- LVDS
- LVPECL
- 3.3-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output column clock pins only)
- GTL/GTL+
- 1.5-V HSTL Class I and II

configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 2 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC}, the POR time is 2 ms.

The nIO_PULLUP pin enables a built-in weak pull-up resistor to pull all user I/O pins to V_{CCIO} before and during device configuration. If nIO_PULLUP is connected to V_{CC} during configuration, the weak pull-ups on all user I/O pins are disabled. If connected to ground, the pull-ups are enabled during configuration. The nIO_PULLUP pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

VCCSEL is a dedicated input that is used to choose whether all dedicated configuration and JTAG input pins can accept 1.5 V/1.8 V or 2.5 V/3.3 V during configuration. A logic low sets 3.3 V/2.5 V, and a logic high sets 1.8 V/1.5 V. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, PLL_ENA, CONF_DONE, nSTATUS. The VCCSEL pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

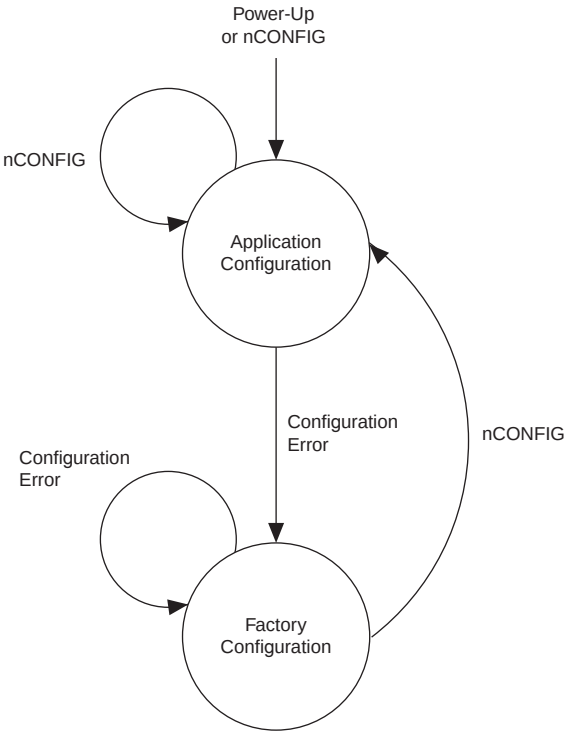
The VCCSEL signal does not control the dual-purpose configuration pins such as the DATA[7..0] and PPA pins (nWS, nRS, CS, nCS, and RDYnBSY). During configuration, these dual-purpose pins will drive out voltage levels corresponding to the V_{CCIO} supply voltage that powers the I/O bank containing the pin. After configuration, the dual-purpose pins use I/O standards specified in the user design.

TDO and nCEO drive out at the same voltages as the V_{CCIO} supply that powers the I/O bank containing the pin. Users must select the V_{CCIO} supply for bank containing TDO accordingly. For example, when using the ByteBlaster™ MV cable, the V_{CCIO} for the bank containing TDO must be powered up at 3.3 V.

Local Update Mode

Local update mode is a simplified version of the remote update. This feature is intended for simple systems that need to load a single application configuration immediately upon power up without loading the factory configuration first. Local update designs have only one application configuration to load, so it does not require a factory configuration to determine which application configuration to use. Figure 3–4 shows the transition diagram for local update mode.

Figure 3–4. Local Update Transition Diagram



Stratix Automated Single Event Upset (SEU) Detection

Stratix devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. FPGA devices that operate at high elevations or in close proximity to earth's North or South Pole require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 4–8. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	0.75 × V_{CCIO}		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		0.25 × V_{CCIO}	V

Notes to Tables 4–1 through 4–8:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns, or overshoot to the voltage shown in Table 4–9, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.

(5) V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(7) Typical values are for T_A = 25°C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

(10) Drive strength is programmable according to the values shown in the *Stratix Architecture* chapter of the *Stratix Device Handbook, Volume 1*.

Table 4–9. Overshoot Input Voltage with Respect to Duty Cycle (Part 1 of 2)

Vin (V)	Maximum Duty Cycle (%)
4.0	100
4.1	90
4.2	50

Tables 4–85 through 4–90 show the external timing parameters on column and row pins for EP1S60 devices.

Table 4–85. EP1S60 External I/O Timing on Column Pins Using Fast Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.029		3.277		3.733		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.446	4.871	2.446	5.215	2.446	5.685	NA	NA	ns
t_{XZ}	2.386	4.745	2.386	5.083	2.386	5.561	NA	NA	ns
t_{ZX}	2.386	4.745	2.386	5.083	2.386	5.561	NA	NA	ns

Table 4–86. EP1S60 External I/O Timing on Column Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.491		2.691		3.060		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.767	5.409	2.767	5.801	2.767	6.358	NA	NA	ns
t_{XZ}	2.707	5.283	2.707	5.669	2.707	6.234	NA	NA	ns
t_{ZX}	2.707	5.283	2.707	5.669	2.707	6.234	NA	NA	ns
$t_{INSUPLL}$	1.233		1.270		1.438		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.078	2.278	1.078	2.395	1.078	2.428	NA	NA	ns
t_{XZPLL}	1.018	2.152	1.018	2.263	1.018	2.304	NA	NA	ns
t_{ZXPLL}	1.018	2.152	1.018	2.263	1.018	2.304	NA	NA	ns

Table 4–97. Output Pin Timing Skew Definitions (Part 2 of 2)	
Symbol	**Definition**
t_{LR_HIO}	Across all HIO banks (1, 2, 5, 6); across four similar type I/O banks
t_{TB_VIO}	Across all VIO banks (3, 4, 7, 8); across four similar type I/O banks
$t_{OVERALL}$	Output timing skew for all I/O pins on the device.

Notes to Table 4–97:
(1) See Figure 4–5 on page 4–57.
(2) See Figure 4–6 on page 4–58.

Table 4–98 shows the I/O skews when using the same global or regional clock to feed IOE registers in I/O banks around each device. These values can be used for calculating the timing budget on the output (write) side of a memory interface. These values already factor in the package skew.

Table 4–98. Output Skew for Stratix by Device Density			
Symbol	**Skew (ps)** *(1)*		
	EP1S10 to EP1S30	**EP1S40**	**EP1S60 & EP1S80**
t_{SB_HIO}	90	290	500
t_{SB_VIO}	160	290	500
t_{SS_HIO}	90	460	600
t_{SS_VIO}	180	520	630
t_{LR_HIO}	150	490	600
t_{TB_VIO}	190	580	670
$t_{OVERALL}$	430	630	880

Note to Table 4–98:
(1) The skew numbers in Table 4–98 account for worst case package skews.

The scaling factors for column output pin timing in Tables 4–111 to 4–113 are shown in units of time per pF unit of capacitance (ps/pF). Add this delay to the t_{CO} or combinatorial timing path for output or bidirectional pins in addition to the I/O adder delays shown in Tables 4–103 through 4–108 and the IOE programmable delays in Tables 4–109 and 4–110.

Table 4–111. Output Delay Adder for Loading on LVTTL/LVCMOS Output Buffers *Note (1)*

Conditions		Output Pin Adder Delay (ps/pF)				
Parameter	**Value**	**3.3-V LVTTL**	**2.5-V LVTTL**	**1.8-V LVTTL**	**1.5-V LVTTL**	**LVCMOS**
Drive Strength	24mA	15	–	–	-	8
	16mA	25	18	–	–	–
	12mA	30	25	25	–	15
	8mA	50	35	40	35	20
	4mA	60	–	–	80	30
	2mA	–	75	120	160	60

Note to Table 4–111:
(1) The timing information in this table is preliminary.

Table 4–112. Output Delay Adder for Loading on SSTL/HSTL Output Buffers *Note (1)*

Conditions	Output Pin Adder Delay (ps/pF)			
	SSTL-3	**SSTL-2**	**SSTL-1.8**	**1.5-V HSTL**
Class I	25	25	25	25
Class II	25	20	25	20

Note to Table 4–112:
(1) The timing information in this table is preliminary.

Table 4–113. Output Delay Adder for Loading on GTL+/GTL/CTT/PCI Output Buffers *Note (1)*

Conditions		Output Pin Adder Delay (ps/pF)				
Parameter	**Value**	**GTL+**	**GTL**	**CTT**	**PCI**	**AGP**
VCCIO Voltage Level	3.3V	18	18	25	20	20
	2.5V	15	18	-	-	-

Note to Table 4–113:
(1) The timing information in this table is preliminary.

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 4 of 4) Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{DUTY}	LVDS (J = 2 through 10)	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (J =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100			100	µs

Notes to Table 4–125:

(1) When J = 4, 7, 8, and 10, the SERDES block is used.

(2) When J = 2 or J = 1, the SERDES is bypassed.