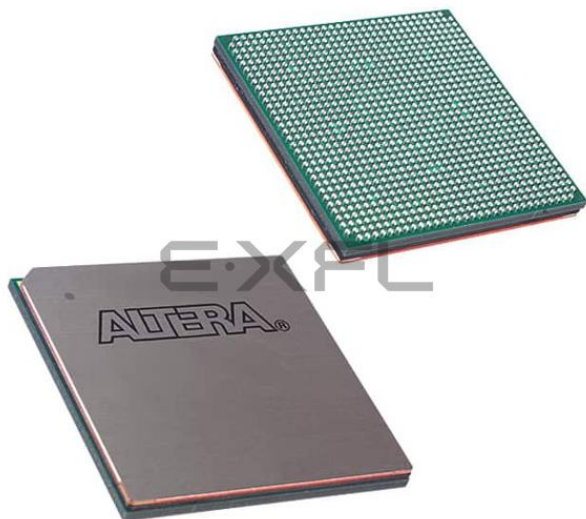




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3247
Number of Logic Elements/Cells	32470
Total RAM Bits	3317184
Number of I/O	726
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s30f1020i6ga

Stratix devices are available in space-saving FineLine BGA® and ball-grid array (BGA) packages (see [Tables 1–3](#) through [1–5](#)). All Stratix devices support vertical migration within the same package (for example, you can migrate between the EP1S10, EP1S20, and EP1S25 devices in the 672-pin BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migrational. The Quartus® II software can automatically cross reference and place all pins except differential pins for migration when given a device migration list. You must use the pin-outs for each device to verify the differential placement migration. A future version of the Quartus II software will support differential pin migration.

Table 1–3. Stratix Package Options & I/O Pin Counts

Device	672-Pin BGA	956-Pin BGA	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP1S10	345		335	345	426		
EP1S20	426		361	426	586		
EP1S25	473			473	597	706	
EP1S30		683			597	726	
EP1S40		683			615	773	822
EP1S60		683				773	1,022
EP1S80		683				773	1,203

Note to [Table 1–3](#):

- (1) All I/O pin counts include 20 dedicated clock input pins (clk[15..0]p, clk0n, clk2n, clk9n, and clk11n) that can be used for data inputs.

Table 1–4. Stratix BGA Package Sizes

Dimension	672 Pin	956 Pin
Pitch (mm)	1.27	1.27
Area (mm ²)	1,225	1,600
Length × width (mm × mm)	35 × 35	40 × 40

Table 2–9. M-RAM Block Configurations (True Dual-Port)

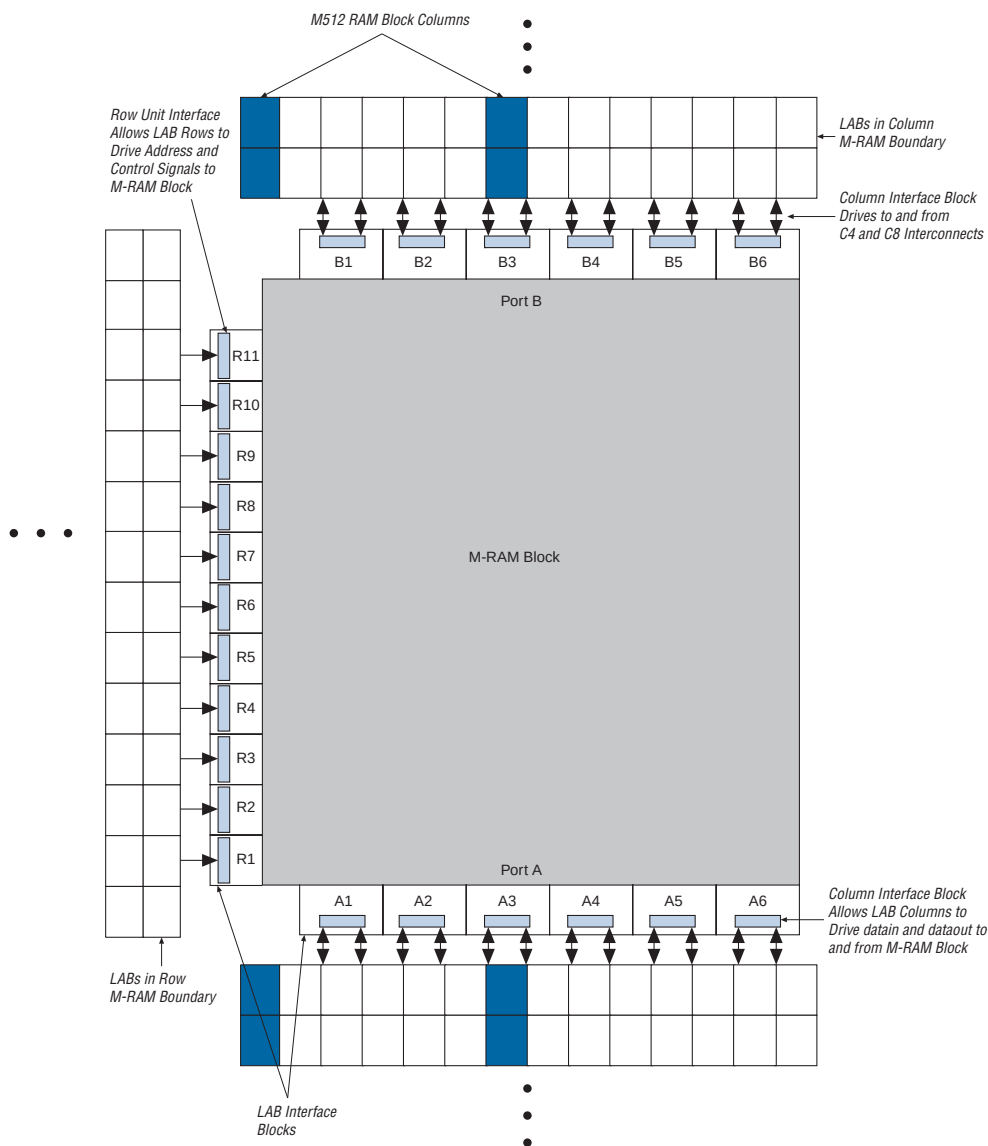
Port A	Port B			
	64K × 9	32K × 18	16K × 36	8K × 72
64K × 9	✓	✓	✓	✓
32K × 18	✓	✓	✓	✓
16K × 36	✓	✓	✓	✓
8K × 72	✓	✓	✓	✓

The read and write operation of the memory is controlled by the `WREN` signal, which sets the ports into either read or write modes. There is no separate read enable (`RE`) signal.

Writing into RAM is controlled by both the `WREN` and byte enable (`byteena`) signals for each port. The default value for the `byteena` signal is high, in which case writing is controlled only by the `WREN` signal. The byte enables are available for the $\times 18$, $\times 36$, and $\times 72$ modes. In the $\times 144$ simple dual-port mode, the two sets of `byteena` signals (`byteena_a` and `byteena_b`) are combined to form the necessary 16 byte enables. Tables 2–10 and 2–11 summarize the byte selection.

Table 2–10. Byte Enable for M-RAM Blocks *Notes (1), (2)*

<code>byteena[3..0]</code>	<code>datain $\times 18$</code>	<code>datain $\times 36$</code>	<code>datain $\times 72$</code>
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

Figure 2–21. Left-Facing M-RAM to Interconnect Interface *Notes (1), (2)***Notes to Figure 2–21:**

- (1) Only R24 and C16 interconnects cross the M-RAM block boundaries.
- (2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

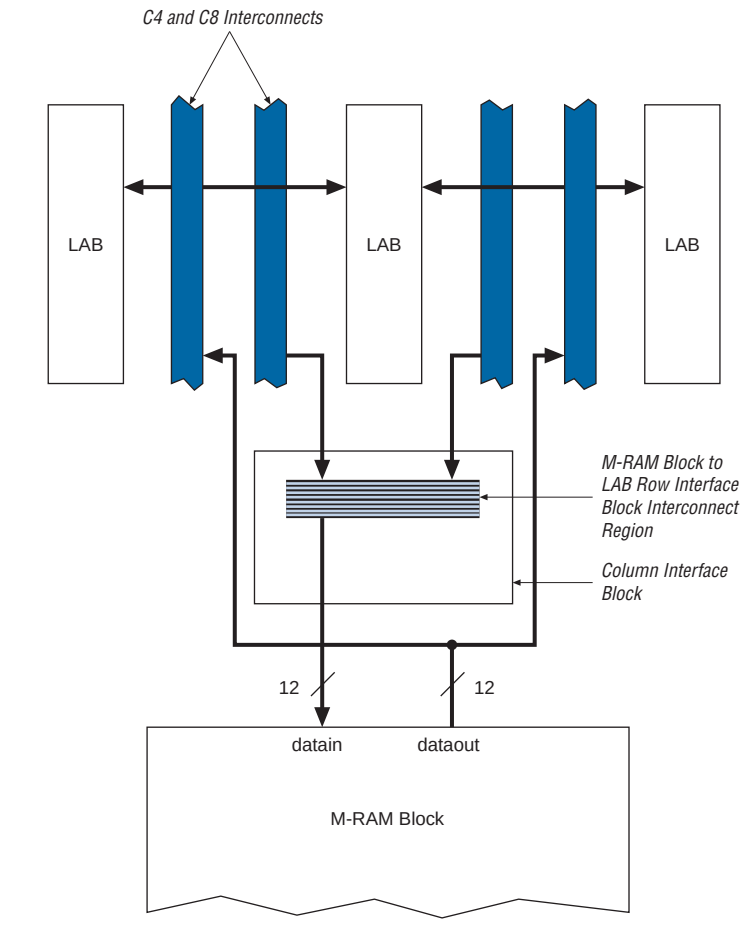
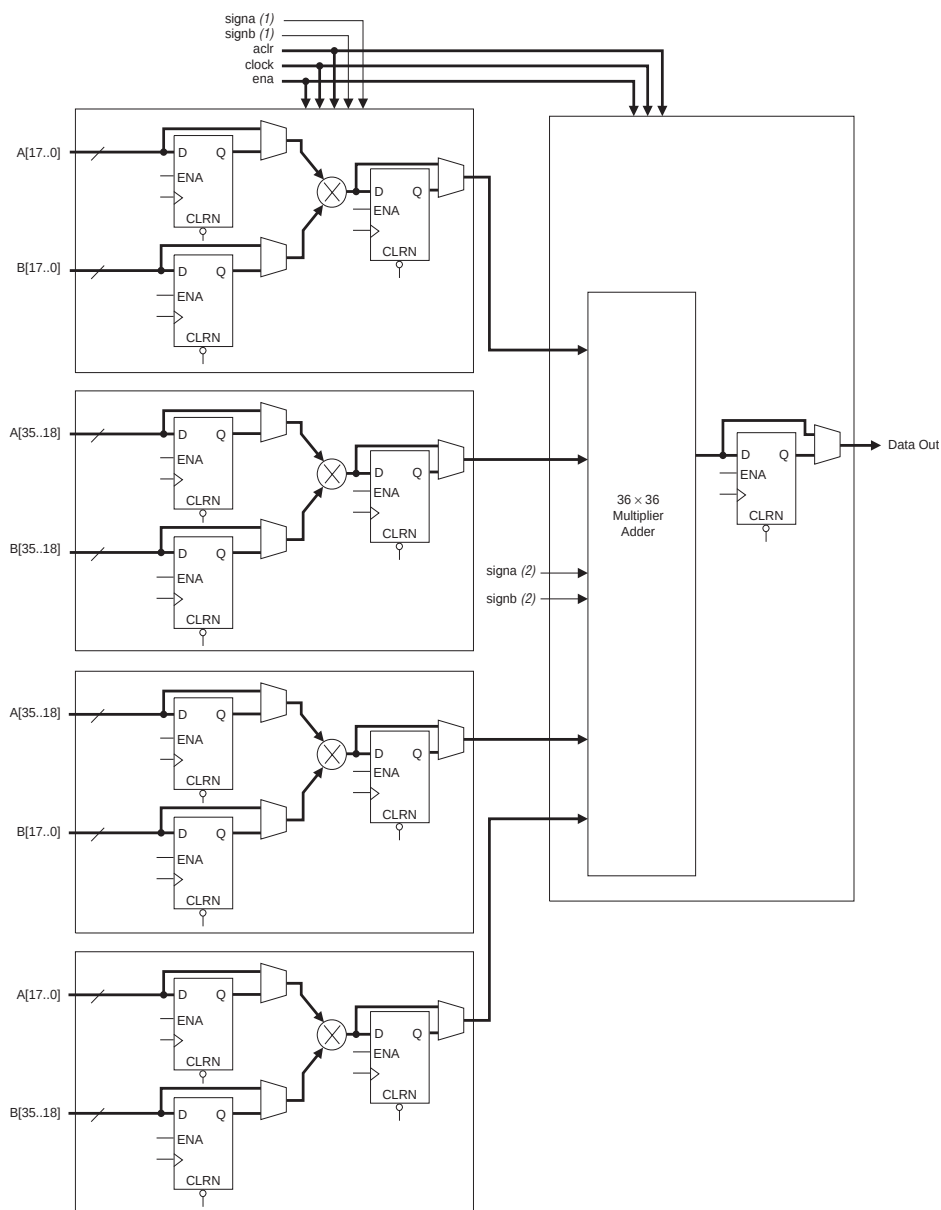
Figure 2–23. M-RAM Column Unit Interface to Interconnect

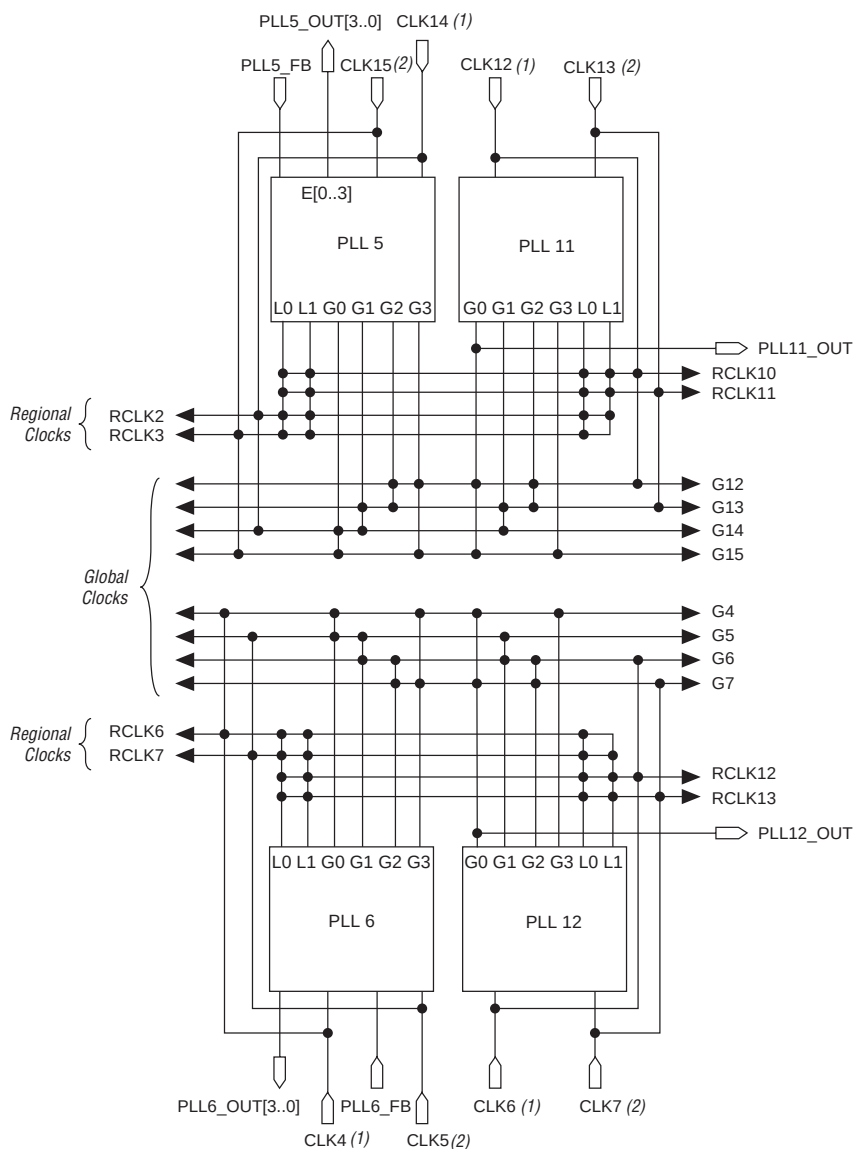
Figure 2–36. 36×36 Multiply Mode



Notes to Figure 2–36:

- (1) These signals are not registered or registered once to match the pipeline.
- (2) These signals are not registered, registered once, or registered twice for latency to match the pipeline.

Figure 2–51. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs *Note (1)*



Notes to Figure 2–51:

- (1) PLLs 1 to 4 and 7 to 10 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs.
- (2) CLK4, CLK6, CLK12, and CLK14 feed the corresponding PLL's `inc1k0` port.
- (3) CLK5, CLK7, CLK13, and CLK15 feed the corresponding PLL's `inc1k1` port.
- (4) The EP1S40 device in the 780-pin FineLine BGA package does not support PLLs 11 and 12.

Clock Multiplication & Division

Each Stratix device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times \text{post-scale counter})$ scaling factors. The input clock is divided by a pre-scale divider, n , and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{\text{IN}} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale counter, n , and one multiply counter, m , per PLL, with a range of 1 to 512 on each. There are two post-scale counters (l) for regional clock output ports, four counters (g) for global clock output ports, and up to four counters (e) for external clock outputs, all ranging from 1 to 1024 with a 50% duty cycle setting. The post-scale counters range from 1 to 512 with any non-50% duty cycle setting. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix device enhanced PLLs support a flexible clock switchover capability. [Figure 2–53](#) shows a block diagram of the switchover circuit. The switchover circuit is configurable, so you can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

Programmable Pull-Up Resistor

Each Stratix device I/O pin provides an optional programmable pull-up resistor during user mode. If this feature is enabled for an I/O pin, the pull-up resistor (typically 25 k Ω) weakly holds the output to the V_{CCIO} level of the output pin's bank. Table 2–30 shows which pin types support the weak pull-up resistor feature.

Table 2–30. Programmable Weak Pull-Up Resistor Support	
Pin Type	Programmable Weak Pull-Up Resistor
I/O pins	✓
CLK [15 . . 0]	
FCLK	✓
FPLL [7 . . 10] CLK	
Configuration pins	
JTAG pins	✓ (1)

Note to Table 2–30:

(1) TDO pins do not support programmable weak pull-up resistors.

Advanced I/O Standard Support

Stratix device IOEs support the following I/O standards:

- LVTTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP (1× and 2×)
- LVDS
- LVPECL
- 3.3-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output column clock pins only)
- GTL/GTL+
- 1.5-V HSTL Class I and II



- (1) **Figure 2-70** is a top view of the silicon die. This will correspond to a top-down view for non-flip-chip packages, but will be a reverse view for flip-chip packages.
- (2) **Figure 2-70** is a graphic representation only. See the device pin-outs on the web (www.altera.com) and the Quartus II software for exact locations.
- (3) Banks 9 through 12 are enhanced PLL external clock output banks.
- (4) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL Class I and II, GTL, SSTL-18 Class II, PCI, PCI-X 1.0, and AGP 1x/2x.
- (5) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix and Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2*.



Stratix, Stratix II, Cyclone®, and Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix, Stratix II, Cyclone, and Cyclone II devices are in the 18th or after they will fail configuration. This does not affect SignalTap II.



For more information on JTAG, see the following documents:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

SignalTap II Embedded Logic Analyzer

Stratix devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix architecture are configured with CMOS SRAM elements. Altera® devices are reconfigurable. Because every device is tested with a high-coverage production test program, you do not have to perform fault testing and can focus on simulation and design verification.

Stratix devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices that configure Stratix devices via a serial data stream. Stratix devices can be configured in under 100 ms using 8-bit parallel data at 100 MHz. The Stratix device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy. After a Stratix device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Operating Modes

The Stratix architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after

configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 2 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC} , the POR time is 2 ms.

The nIO_PULLUP pin enables a built-in weak pull-up resistor to pull all user I/O pins to V_{CCIO} before and during device configuration. If nIO_PULLUP is connected to V_{CC} during configuration, the weak pull-ups on all user I/O pins are disabled. If connected to ground, the pull-ups are enabled during configuration. The nIO_PULLUP pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

VCCSEL is a dedicated input that is used to choose whether all dedicated configuration and JTAG input pins can accept 1.5 V/1.8 V or 2.5 V/3.3 V during configuration. A logic low sets 3.3 V/2.5 V, and a logic high sets 1.8 V/1.5 V. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, $nCONFIG$, nCE , DCLK, PLL_ENA , $CONF_DONE$, $nSTATUS$. The VCCSEL pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

The VCCSEL signal does not control the dual-purpose configuration pins such as the $DATA[7..0]$ and PPA pins (nWS , nRS , CS , nCS , and $RDYnBSY$). During configuration, these dual-purpose pins will drive out voltage levels corresponding to the V_{CCIO} supply voltage that powers the I/O bank containing the pin. After configuration, the dual-purpose pins use I/O standards specified in the user design.

TDO and $nCEO$ drive out at the same voltages as the V_{CCIO} supply that powers the I/O bank containing the pin. Users must select the V_{CCIO} supply for bank containing TDO accordingly. For example, when using the ByteBlaster™ MV cable, the V_{CCIO} for the bank containing TDO must be powered up at 3.3 V.

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCIO}	Output supply voltage		1.65	1.95	V
V _{IH}	High-level input voltage		0.65 × V _{CCIO}	2.25	V
V _{IL}	Low-level input voltage		–0.3	0.35 × V _{CCIO}	V
V _{OH}	High-level output voltage	I _{OH} = –2 to –8 mA (10)	V _{CCIO} – 0.45		V
V _{OL}	Low-level output voltage	I _{OL} = 2 to 8 mA (10)		0.45	V

Table 4–8. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCIO}	Output supply voltage		1.4	1.6	V
V _{IH}	High-level input voltage		0.65 × V _{CCIO}	V _{CCIO} + 0.3	V
V _{IL}	Low-level input voltage		–0.3	0.35 × V _{CCIO}	V
V _{OH}	High-level output voltage	I _{OH} = –2 mA (10)	0.75 × V _{CCIO}		V
V _{OL}	Low-level output voltage	I _{OL} = 2 mA (10)		0.25 × V _{CCIO}	V

Notes to Tables 4–1 through 4–8:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
- (3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns, or overshoot to the voltage shown in Table 4–9, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.
- (4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
- (5) V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (7) Typical values are for T_A = 25°C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.
- (8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).
- (9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.
- (10) Drive strength is programmable according to the values shown in the *Stratix Architecture* chapter of the *Stratix Device Handbook, Volume 1*.

Table 4–9. Overshoot Input Voltage with Respect to Duty Cycle (Part 1 of 2)

V _{in} (V)	Maximum Duty Cycle (%)
4.0	100
4.1	90
4.2	50

Table 4–22. SSTL-3 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.4$	V
V_{OH}	High-level output voltage	$I_{OH} = -8 \text{ mA}$ (3)	$V_{TT} + 0.6$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8 \text{ mA}$ (3)			$V_{TT} - 0.6$	V

Table 4–23. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
$V_{IH(DC)}$	High-level DC input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
$V_{IL(DC)}$	Low-level DC input voltage		-0.3		$V_{REF} - 0.2$	V
$V_{IH(AC)}$	High-level AC input voltage		$V_{REF} + 0.4$			V
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.4$	V
V_{OH}	High-level output voltage	$I_{OH} = -16 \text{ mA}$ (3)	$V_{TT} + 0.8$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16 \text{ mA}$ (3)			$V_{TT} - 0.8$	V

Table 4–24. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage (4)		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage (4)				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = -0.5 \text{ mA}$	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	$I_{OUT} = 1.5 \text{ mA}$			$0.1 \times V_{CCIO}$	V

Table 4–25. 3.3-V AGP 1× Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage (4)		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage (4)				$0.3 \times V_{CCIO}$	V

Table 4–40. M512 Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{M512RC}	Synchronous read cycle time
t_{M512WC}	Synchronous write cycle time
$t_{M512WERESU}$	Write or read enable setup time before clock
$t_{M512WEREH}$	Write or read enable hold time after clock
$t_{M512CLKENSU}$	Clock enable setup time before clock
$t_{M512CLKENH}$	Clock enable hold time after clock
$t_{M512DATASU}$	Data setup time before clock
$t_{M512DATAH}$	Data hold time after clock
$t_{M512WADDRSU}$	Write address setup time before clock
$t_{M512WADDRH}$	Write address hold time after clock
$t_{M512RADDRSU}$	Read address setup time before clock
$t_{M512RADDRH}$	Read address hold time after clock
$t_{M512DATACO1}$	Clock-to-output delay when using output registers
$t_{M512DATACO2}$	Clock-to-output delay without output registers
$t_{M512CLKHL}$	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown in Table 4–36 on page 4–20 and as reported by the timing analyzer in the Quartus II software.
$t_{M512CLR}$	Minimum clear pulse width

Table 4–41. M4K Block Internal Timing Microparameter Descriptions (Part 1 of 2)

Symbol	Parameter
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KCLKENSU}$	Clock enable setup time before clock
$t_{M4KCLKENH}$	Clock enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock

Stratix External I/O Timing

These timing parameters are for both column IOE and row IOE pins. In EP1S30 devices and above, you can decrease the t_{SU} time by using the FPLLCLK, but may get positive hold time in EP1S60 and EP1S80 devices. You should use the Quartus II software to verify the external devices for any pin.

Tables 4–55 through 4–60 show the external timing parameters on column and row pins for EP1S10 devices.

Table 4–55. EP1S10 External I/O Timing on Column Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.238		2.325		2.668		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.240	4.549	2.240	4.836	2.240	5.218	NA	NA	ns
t_{XZ}	2.180	4.423	2.180	4.704	2.180	5.094	NA	NA	ns
t_{ZX}	2.180	4.423	2.180	4.704	2.180	5.094	NA	NA	ns

Table 4–56. EP1S10 External I/O Timing on Column Pins Using Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max			
t_{INSU}	1.992		2.054		2.359		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.395	4.795	2.395	5.107	2.395	5.527	NA	NA	ns
t_{XZ}	2.335	4.669	2.335	4.975	2.335	5.403	NA	NA	ns
t_{ZX}	2.335	4.669	2.335	4.975	2.335	5.403	NA	NA	ns
$t_{INSUPLL}$	0.975		0.985		1.097		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA	NA	ns
$t_{OUTCOPLL}$	1.262	2.636	1.262	2.680	1.262	2.769	NA	NA	ns
t_{XZPLL}	1.202	2.510	1.202	2.548	1.202	2.645	NA	NA	ns
t_{ZXPLL}	1.202	2.510	1.202	2.548	1.202	2.645	NA	NA	ns

Tables 4–85 through 4–90 show the external timing parameters on column and row pins for EP1S60 devices.

Table 4–85. EP1S60 External I/O Timing on Column Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.029		3.277		3.733		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.446	4.871	2.446	5.215	2.446	5.685	NA	NA	ns
t_{xZ}	2.386	4.745	2.386	5.083	2.386	5.561	NA	NA	ns
t_{ZX}	2.386	4.745	2.386	5.083	2.386	5.561	NA	NA	ns

Table 4–86. EP1S60 External I/O Timing on Column Pins Using Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.491		2.691		3.060		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.767	5.409	2.767	5.801	2.767	6.358	NA	NA	ns
t_{xZ}	2.707	5.283	2.707	5.669	2.707	6.234	NA	NA	ns
t_{ZX}	2.707	5.283	2.707	5.669	2.707	6.234	NA	NA	ns
t_{INSUPLL}	1.233		1.270		1.438		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
t_{OUTCOPLL}	1.078	2.278	1.078	2.395	1.078	2.428	NA	NA	ns
t_{xZPLL}	1.018	2.152	1.018	2.263	1.018	2.304	NA	NA	ns
t_{ZXPLL}	1.018	2.152	1.018	2.263	1.018	2.304	NA	NA	ns

Table 4–108. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,571		1,650		1,650		1,650	ps
	4 mA		594		624		624		624	ps
	8 mA		208		218		218		218	ps
	12 mA		0		0		0		0	ps
3.3-V LVTTTL	4 mA		1,571		1,650		1,650		1,650	ps
	8 mA		1,393		1,463		1,463		1,463	ps
	12 mA		596		626		626		626	ps
	16 mA		562		590		590		590	ps
2.5-V LVTTTL	2 mA		2,562		2,690		2,690		2,690	ps
	8 mA		1,343		1,410		1,410		1,410	ps
	12 mA		864		907		907		907	ps
	16 mA		945		992		992		992	ps
1.8-V LVTTTL	2 mA		6,306		6,621		6,621		6,621	ps
	8 mA		3,369		3,538		3,538		3,538	ps
	12 mA		2,932		3,079		3,079		3,079	ps
1.5-V LVTTTL	2 mA		9,759		10,247		10,247		10,247	ps
	4 mA		6,830		7,172		7,172		7,172	ps
	8 mA		5,699		5,984		5,984		5,984	ps
GTL+			–333		–350		–350		–350	ps
CTT			591		621		621		621	ps
SSTL-3 Class I			267		280		280		280	ps
SSTL-3 Class II			–346		–363		–363		–363	ps
SSTL-2 Class I			481		505		505		505	ps
SSTL-2 Class II			–58		–61		–61		–61	ps
SSTL-18 Class I			2,207		2,317		2,317		2,317	ps
1.5-V HSTL Class I			1,966		2,064		2,064'		2,064	ps
1.8-V HSTL Class I			1,208		1,268		1,460		1,720	ps

The scaling factors for column output pin timing in Tables 4–111 to 4–113 are shown in units of time per pF unit of capacitance (ps/pF). Add this delay to the t_{CO} or combinatorial timing path for output or bidirectional pins in addition to the I/O adder delays shown in Tables 4–103 through 4–108 and the IOE programmable delays in Tables 4–109 and 4–110.

Table 4–111. Output Delay Adder for Loading on LVTTTL/LVCMOS Output Buffers *Note (1)*

Conditions		Output Pin Adder Delay (ps/pF)				
Parameter	Value	3.3-V LVTTTL	2.5-V LVTTTL	1.8-V LVTTTL	1.5-V LVTTTL	LVCMOS
Drive Strength	24mA	15	–	–	–	8
	16mA	25	18	–	–	–
	12mA	30	25	25	–	15
	8mA	50	35	40	35	20
	4mA	60	–	–	80	30
	2mA	–	75	120	160	60

Note to Table 4–111:

- (1) The timing information in this table is preliminary.

Table 4–112. Output Delay Adder for Loading on SSTL/HSTL Output Buffers *Note (1)*

Conditions	Output Pin Adder Delay (ps/pF)			
	SSTL-3	SSTL-2	SSTL-1.8	1.5-V HSTL
Class I	25	25	25	25
Class II	25	20	25	20

Note to Table 4–112:

- (1) The timing information in this table is preliminary.

Table 4–113. Output Delay Adder for Loading on GTL+/GTL/CTT/PCI Output Buffers *Note (1)*

Conditions		Output Pin Adder Delay (ps/pF)				
Parameter	Value	GTL+	GTL	CTT	PCI	AGP
VCCIO Voltage Level	3.3V	18	18	25	20	20
	2.5V	15	18	–	–	–

Note to Table 4–113:

- (1) The timing information in this table is preliminary.

High-Speed I/O Specification

Table 4–124 provides high-speed timing specifications definitions.

Table 4–124. High-Speed Timing Specifications & Terminology	
High-Speed Timing Specification	Terminology
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. $(TUI = 1/(\text{Receiver Input Clock Frequency} \times \text{Multiplication Factor}) = t_C/w)$.
f_{HSDR}	Maximum LVDS data transfer rate ($f_{HSDR} = 1/TUI$).
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid to be captured correctly. The setup and hold times determine the ideal strobe position within the sampling window. $SW = t_{SW}(\text{max}) - t_{SW}(\text{min})$.
Input jitter (peak-to-peak)	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak-to-peak)	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.
J	Deserialization factor (width of internal data bus).
W	PLL multiplication factor.

Tables 4–131 through 4–133 describe the Stratix device fast PLL specifications.

Table 4–131. Fast PLL Specifications for -5 & -6 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{IN}	CLKIN frequency (1), (2), (3)	10	717	MHz
f_{INPFD}	Input frequency to PFD	10	500	MHz
f_{OUT}	Output frequency for internal global or regional clock (3)	9.375	420	MHz
f_{OUT_DIFFIO}	Output frequency for external clock driven out on a differential I/O data channel (2)	(5)	(5)	
f_{VCO}	VCO operating frequency	300	1,000	MHz
t_{INDUTY}	CLKIN duty cycle	40	60	%
$t_{INJITTER}$	Period jitter for CLKIN pin		±200	ps
t_{DUTY}	Duty cycle for DFFIO 1 × CLKOUT pin (6)	45	55	%
t_{JITTER}	Period jitter for DIFFIO clock out (6)		(5)	ps
t_{LOCK}	Time required for PLL to acquire lock	10	100	μs
m	Multiplication factors for m counter (6)	1	32	Integer
l_0, l_1, g_0	Multiplication factors for l_0, l_1 , and g_0 counter (7), (8)	1	32	Integer
t_{ARESET}	Minimum pulse width on areset signal	10		ns

Table 4–132. Fast PLL Specifications for -7 Speed Grades (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{IN}	CLKIN frequency (1), (3)	10	640	MHz
f_{INPFD}	Input frequency to PFD	10	500	MHz
f_{OUT}	Output frequency for internal global or regional clock (4)	9.375	420	MHz
f_{OUT_DIFFIO}	Output frequency for external clock driven out on a differential I/O data channel	(5)	(5)	MHz
f_{VCO}	VCO operating frequency	300	700	MHz
t_{INDUTY}	CLKIN duty cycle	40	60	%
$t_{INJITTER}$	Period jitter for CLKIN pin		±200	ps
t_{DUTY}	Duty cycle for DFFIO 1 × CLKOUT pin (6)	45	55	%