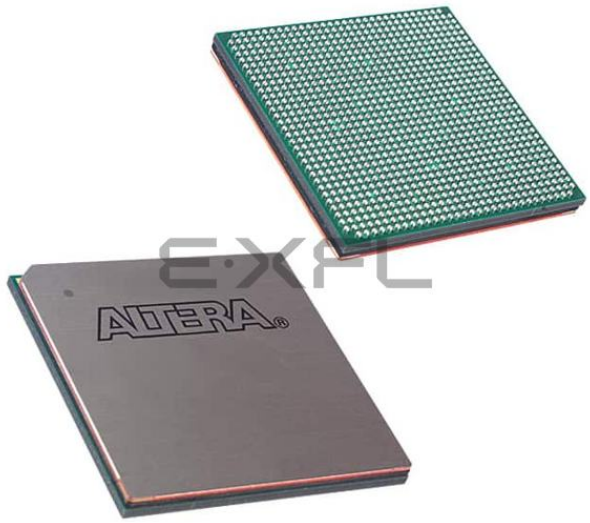

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3247
Number of Logic Elements/Cells	32470
Total RAM Bits	3317184
Number of I/O	726
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s30f1020i6n

2. Stratix Architecture

S51002-3.2

Functional Description

Stratix® devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device's logic array.

Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with

The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix devices.

Table 2–1. Stratix Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP1S10	4 / 94	2 / 60	1	2 / 6	40	30
EP1S20	6 / 194	2 / 82	2	2 / 10	52	41
EP1S25	6 / 224	3 / 138	2	2 / 10	62	46
EP1S30	7 / 295	3 / 171	4	2 / 12	67	57
EP1S40	8 / 384	3 / 183	4	2 / 14	77	61
EP1S60	10 / 574	4 / 292	6	2 / 18	90	73
EP1S80	11 / 767	4 / 364	9	2 / 22	101	91

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, local interconnect, LUT chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix LAB.

functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 2–14 for more information on LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition, and subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The Stratix LE can operate in one of the following modes:

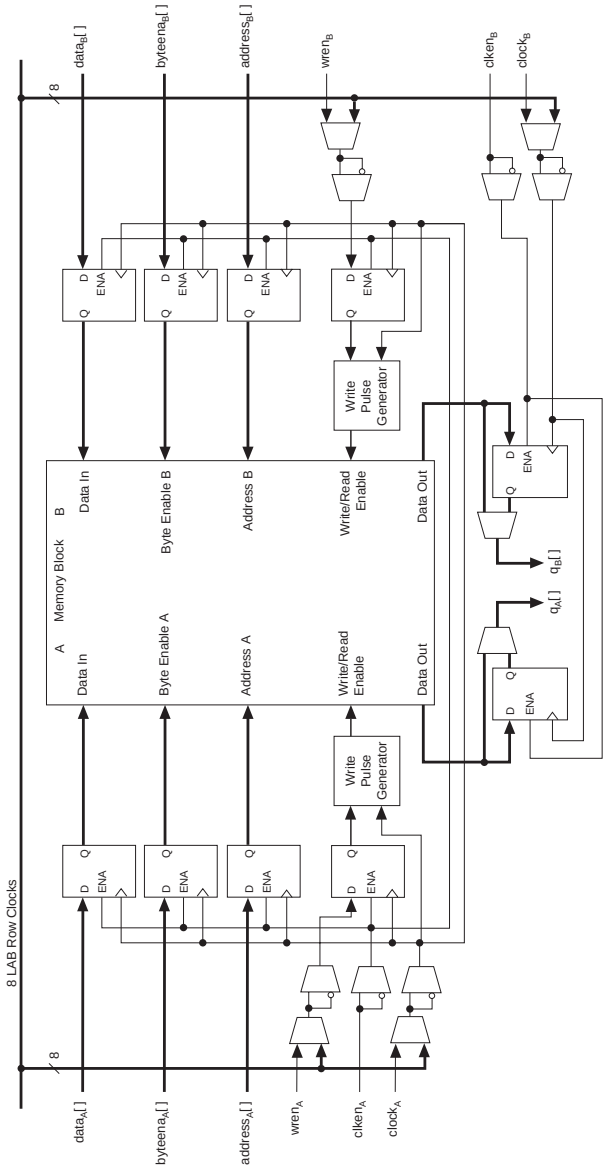
- Normal mode
- Dynamic arithmetic mode

Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0` and `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear,

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–25 and 2–26 show the memory block in input/output clock mode.

Figure 2–25. Input/Output Clock Mode in True Dual-Port Mode Notes (1), (2)

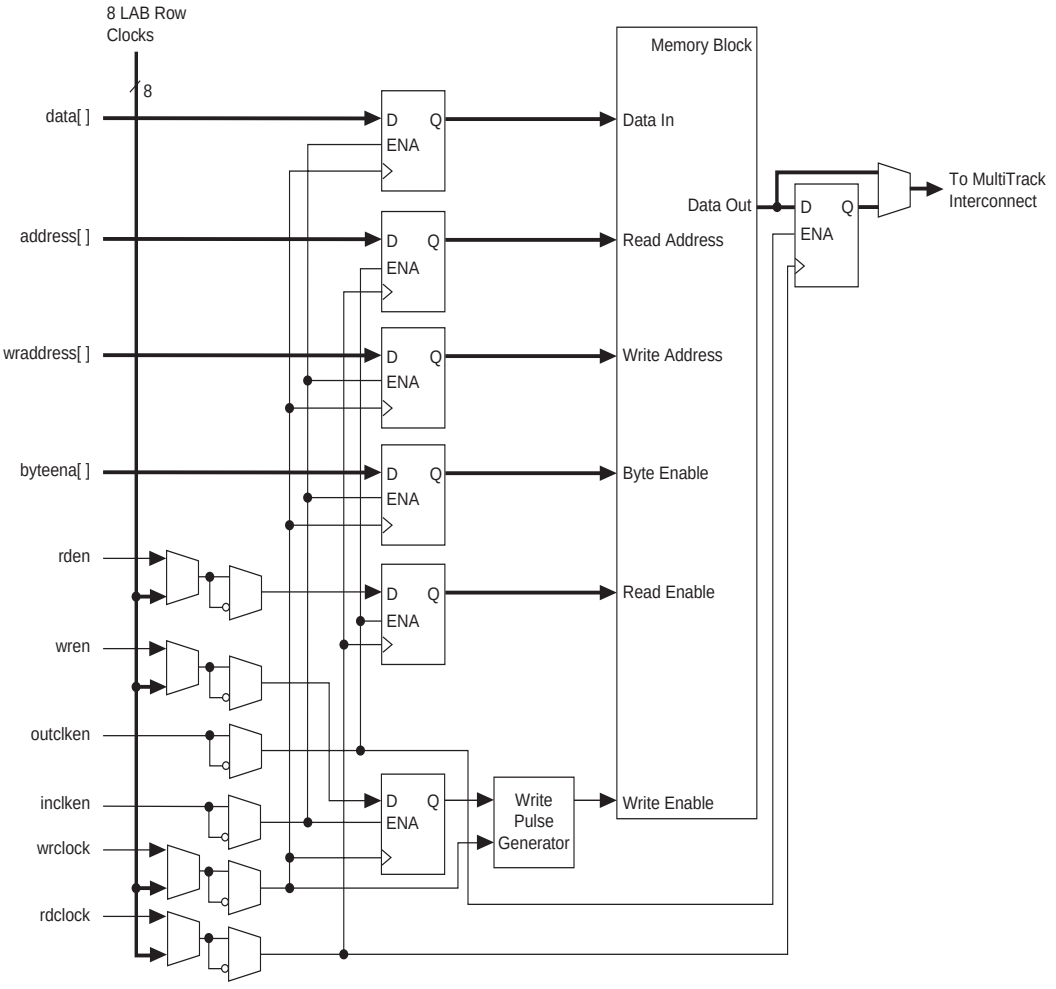


Notes to Figure 2–25:

(1) All registers shown have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Figure 2–27. Read/Write Clock Mode in Simple Dual-Port Mode Notes (1), (2)

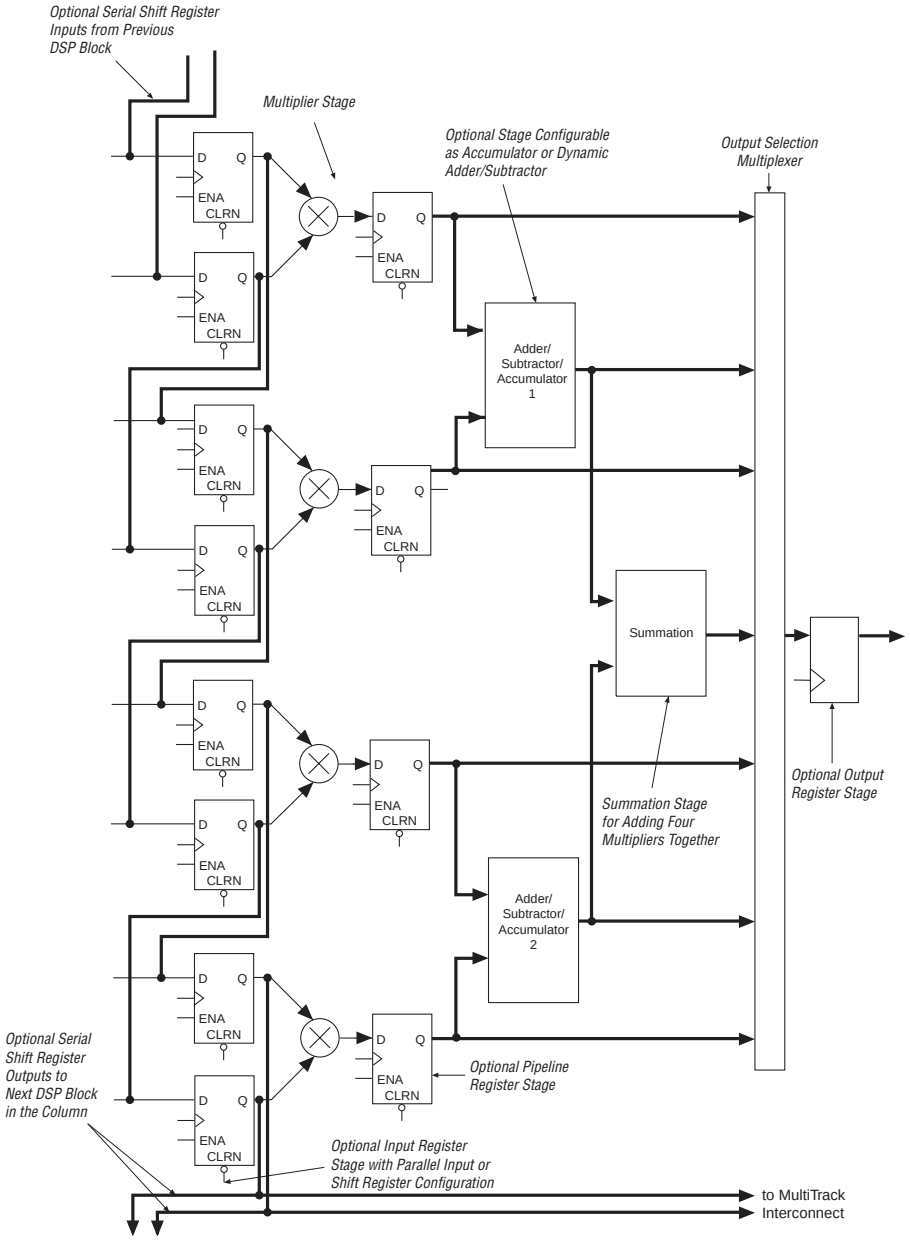


Notes to Figure 2–27:

(1) All registers shown except the `rden` register have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Figure 2–30. DSP Block Diagram for 18 × 18-Bit Configuration



clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–17.

Table 2–17. DSP Block Signal Sources & Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
1	signa	A1[17..0]	OA[17..0]
2	aclr0 accum_sload0	B1[17..0]	OB[17..0]
3	addnsub1 clock0 ena0	A2[17..0]	OC[17..0]
4	aclr1 clock1 ena1	B2[17..0]	OD[17..0]
5	aclr2 clock2 ena2	A3[17..0]	OE[17..0]
6	sign_b clock3 ena3	B3[17..0]	OF[17..0]
7	clear3 accum_sload1	A4[17..0]	OG[17..0]
8	addnsub3	B4[17..0]	OH[17..0]

PLLs & Clock Networks

Stratix devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), and 8 dedicated fast regional clock networks (for EP1S10, EP1S20, and EP1S25 devices), and 16 dedicated fast regional clock networks (for EP1S30 EP1S40, and EP1S60, and EP1S80 devices). These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within Stratix devices.

provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–18 shows the PLLs available for each Stratix device.

Table 2–18. Stratix Device PLL Availability

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5 *(1)*	6 *(1)*	11 *(2)*	12 *(2)*
EP1S10	✓	✓	✓	✓					✓	✓		
EP1S20	✓	✓	✓	✓					✓	✓		
EP1S25	✓	✓	✓	✓					✓	✓		
EP1S30	✓	✓	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓		
EP1S40	✓	✓	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓	✓ *(3)*	✓ *(3)*
EP1S60	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP1S80	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 2–18:

(1) PLLs 5 and 6 each have eight single-ended outputs or four differential outputs.

(2) PLLs 11 and 12 each have one single-ended output.

(3) EP1S30 and EP1S40 devices do not support these PLLs in the 780-pin FineLine BGA® package.

Clock Multiplication & Division

Each Stratix device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times$ post-scale counter) scaling factors. The input clock is divided by a pre-scale divider, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale counter, n, and one multiply counter, m, per PLL, with a range of 1 to 512 on each. There are two post-scale counters (l) for regional clock output ports, four counters (g) for global clock output ports, and up to four counters (e) for external clock outputs, all ranging from 1 to 1024 with a 50% duty cycle setting. The post-scale counters range from 1 to 512 with any non-50% duty cycle setting. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix device enhanced PLLs support a flexible clock switchover capability. Figure 2–53 shows a block diagram of the switchover circuit.The switchover circuit is configurable, so you can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

The pllenable pin is a dedicated pin that enables/disables PLLs. When the pllenable pin is low, the clock output ports are driven by GND and all the PLLs go out of lock. When the pllenable pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the pllenable signal by connecting the pllenable input port of the altpll megafunction to the common pllenable input pin.

The areset signals are reset/resynchronization inputs for each PLL. The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the areset signal in designs if any of the following conditions are true:

- PLL Reconfiguration or Clock switchover enables in the design.
- Phase relationships between output clocks need to be maintained after a loss of lock condition

The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value than desired as the PLL locks. If the system cannot tolerate this, the clkena signal can disable the output clocks until the PLL locks.

The pfdena signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or a clkloss status signal to trigger pfdena.

The clkena signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own clkena signal. The clkena signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the *g* and *l* counters. The clkena signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. Figure 2–57 shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the clkena signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a

Stratix devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 2–73). Figure 2–62 illustrates the signal paths through the I/O block.

Figure 2–62. Signal Path through the I/O Block

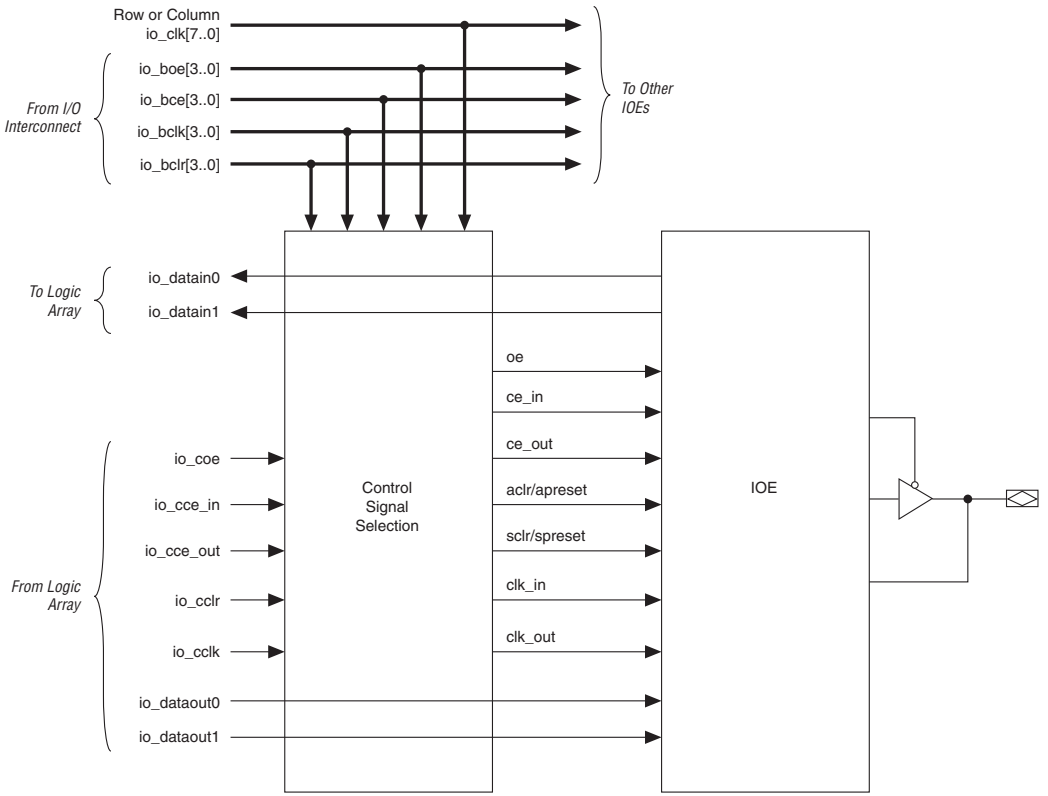
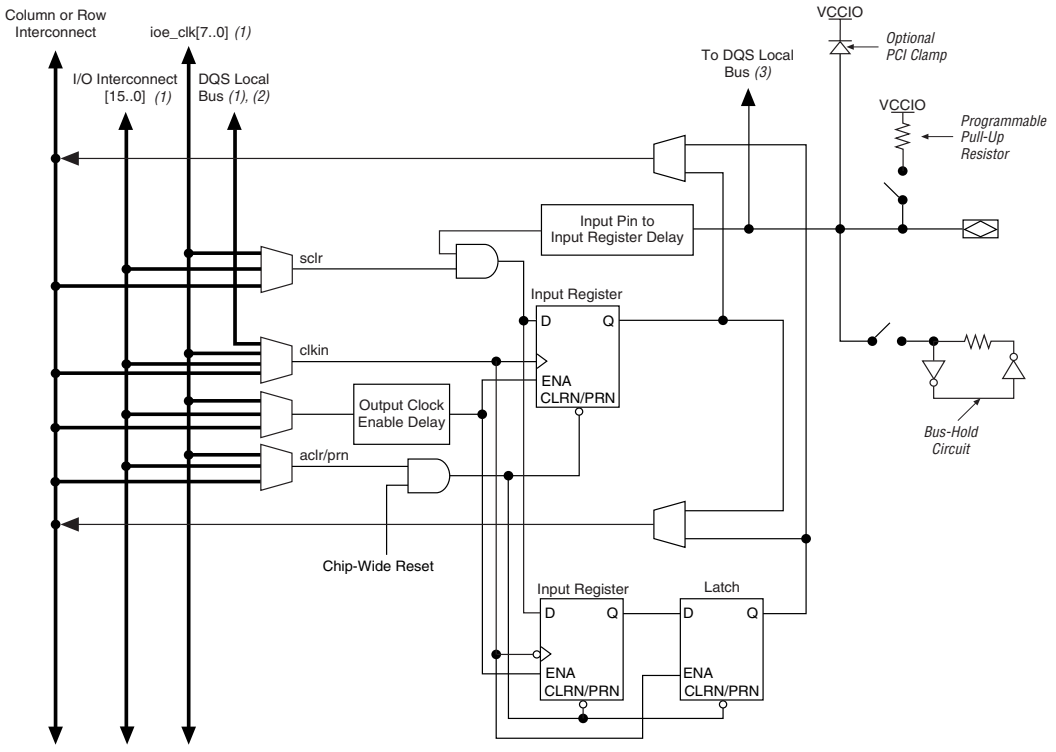


Figure 2–65. Stratix IOE in DDR Input I/O Configuration Note (1)



Notes to Figure 2–65:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.

Tables 2–25 and 2–26 show the performance specification for DDR SDRAM, RLDRAM II, QDR SRAM, QDRII SRAM, and ZBT SRAM interfaces in EP1S10 through EP1S40 devices and in EP1S60 and EP1S80 devices. The DDR SDRAM and QDR SRAM numbers in Table 2–25 have been verified with hardware characterization with third-party DDR SDRAM and QDR SRAM devices over temperature and voltage extremes.

Table 2–25. External RAM Support in EP1S10 through EP1S40 Devices

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)						
		-5 Speed Grade	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade	
		Flip-Chip	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond
DDR SDRAM *(1)*, *(2)*	SSTL-2	200	167	133	133	100	100	100
DDR SDRAM - side banks *(2)*, *(3)*, *(4)*	SSTL-2	150	133	110	133	100	100	100
RLDRAM II *(4)*	1.8-V HSTL	200	*(5)*	*(5)*	*(5)*	*(5)*	*(5)*	*(5)*
QDR SRAM *(6)*	1.5-V HSTL	167	167	133	133	100	100	100
QDRII SRAM *(6)*	1.5-V HSTL	200	167	133	133	100	100	100
ZBT SRAM *(7)*	LVTTL	200	200	200	167	167	133	133

Notes to Table 2–25:

(1) These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).

(2) For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*

(3) DDR SDRAM is supported on the Stratix device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.

(4) These performance specifications are preliminary.

(5) This device does not support RLDRAM II.

(6) For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

(7) For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

Table 2–32. I/O Support by Bank (Part 2 of 2)

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
SSTL-3 Class II	✓	✓	✓
AGP (1× and 2×)	✓		✓
CTT	✓	✓	✓

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different standard independently. Each bank also has dedicated VREF pins to support any one of the voltage-referenced standards (such as SSTL-3) independently.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

Differential On-Chip Termination

Stratix devices provide differential on-chip termination (LVDS I/O standard) to reduce reflections and maintain signal integrity. Differential on-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections. The internal termination is designed using transistors in the linear region of operation.

Stratix devices support internal differential termination with a nominal resistance value of 137.5 Ω for LVDS input receiver buffers. LVPECL signals require an external termination resistor. Figure 2–71 shows the device with differential termination.

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 2 of 2) Note (1)

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S25	672-pin FineLine BGA 672-pin BGA	Transmitter (2)	56	624 (4)	14	14	14	14
				624 (3)	28	28	28	28
		Receiver	58	624 (4)	14	15	15	14
				624 (3)	29	29	29	29
	780-pin FineLine BGA	Transmitter (2)	70	840 (4)	18	17	17	18
				840 (3)	35	35	35	35
		Receiver	66	840 (4)	17	16	16	17
				840 (3)	33	33	33	33
	1,020-pin FineLine BGA	Transmitter (2)	78	840 (4)	19	20	20	19
				840 (3)	39	39	39	39
		Receiver	78	840 (4)	19	20	20	19
				840 (3)	39	39	39	39

Notes to Table 2–37:

(1) The first row for each transmitter or receiver reports the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP1S10 device, PLL 1 can drive a maximum of five channels at 840 Mbps or a maximum of 10 channels at 840 Mbps. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) The number of channels listed includes the transmitter clock output (`tx_outclock`) channel. If the design requires a DDR clock, it can use an extra data channel.

(3) These channels span across two I/O banks per side of the device. When a center PLL clocks channels in the opposite bank on the same side of the device it is called cross-bank PLL support. Both center PLLs can clock cross-bank channels simultaneously if, for example, PLL_1 is clocking all receiver channels and PLL_2 is clocking all transmitter channels. You cannot have two adjacent PLLs simultaneously clocking cross-bank receiver channels or two adjacent PLLs simultaneously clocking transmitter channels. Cross-bank allows for all receiver channels on one side of the device to be clocked on one clock while all transmitter channels on the device are clocked on the other center PLL. Crossbank PLLs are supported at full-speed, 840 Mbps. For wire-bond devices, the full-speed is 624 Mbps.

(4) These values show the channels available for each PLL without crossing another bank.

When you span two I/O banks using cross-bank support, you can route only two load enable signals total between the PLLs. When you enable `rx_data_align`, you use both `rxloadena` and `txloadena` of a PLL. That leaves no `loadena` for the second PLL.

Table 4–2. Stratix Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C

Table 4–3. Stratix Device DC Operating Conditions Note (7) (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All memory blocks in power-down mode)	V_I = ground, no load, no toggling inputs				mA
		EP1S10. V_I = ground, no load, no toggling inputs		37		mA
		EP1S20. V_I = ground, no load, no toggling inputs		65		mA
		EP1S25. V_I = ground, no load, no toggling inputs		90		mA
		EP1S30. V_I = ground, no load, no toggling inputs		114		mA
		EP1S40. V_I = ground, no load, no toggling inputs		145		mA
		EP1S60. V_I = ground, no load, no toggling inputs		200		mA
		EP1S80. V_I = ground, no load, no toggling inputs		277		mA

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–37 through 4–42 describe the Stratix device internal timing microparameters for LEs, IOEs, TriMatrix™ memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–37. LE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinatorial LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Register minimum clock high or low time. The maximum core clock frequency can be calculated by $1/(2 \times t_{CLKHL})$.

Table 4–38. IOE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU_R}	Row IOE input register setup time
t_{SU_C}	Column IOE input register setup time
t_{H}	IOE input and output register hold time after clock
t_{CO_R}	Row IOE input and output register clock-to-output delay
t_{CO_C}	Column IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinatorial output pin
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Register minimum clock high or low time. The maximum I/O clock frequency can be calculated by $1/(2 \times t_{CLKHL})$. Performance may also be affected by I/O timing, use of PLL, and I/O programmable settings.

Table 4–40. M512 Block Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{M512RC}	Synchronous read cycle time
t_{M512WC}	Synchronous write cycle time
$t_{M512WERESU}$	Write or read enable setup time before clock
$t_{M512WEREH}$	Write or read enable hold time after clock
$t_{M512CLKENSU}$	Clock enable setup time before clock
$t_{M512CLKENH}$	Clock enable hold time after clock
$t_{M512DATASU}$	Data setup time before clock
$t_{M512DATAH}$	Data hold time after clock
$t_{M512WADDRSU}$	Write address setup time before clock
$t_{M512WADDRH}$	Write address hold time after clock
$t_{M512RADDRSU}$	Read address setup time before clock
$t_{M512RADDRH}$	Read address hold time after clock
$t_{M512DATACO1}$	Clock-to-output delay when using output registers
$t_{M512DATACO2}$	Clock-to-output delay without output registers
$t_{M512CLKHL}$	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown in Table 4–36 on page 4–20 and as reported by the timing analyzer in the Quartus II software.
$t_{M512CLR}$	Minimum clear pulse width

Table 4–41. M4K Block Internal Timing Microparameter Descriptions (Part 1 of 2)	
Symbol	**Parameter**
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KCLKENSU}$	Clock enable setup time before clock
$t_{M4KCLKENH}$	Clock enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock

Table 4–95. EP1S80 External I/O Timing on Row Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.295		2.454		2.767		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.917	5.732	2.917	6.148	2.917	6.705	NA	NA	ns
t_{XZ}	2.944	5.786	2.944	6.204	2.944	6.773	NA	NA	ns
t_{ZX}	2.944	5.786	2.944	6.204	2.944	6.773	NA	NA	ns
$t_{INSUPLL}$	1.011		1.161		1.372		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.808	3.169	1.808	3.209	1.808	3.233	NA	NA	ns
t_{XZPLL}	1.835	3.223	1.835	3.265	1.835	3.301	NA	NA	ns
t_{ZXPLL}	1.835	3.223	1.835	3.265	1.835	3.301	NA	NA	ns

Table 4–96. EP1S80 External I/O Timing on Rows Using Pin Global Clock Networks Note (1)

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.362		1.451		1.613		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.457	6.665	3.457	7.151	3.457	7.859	NA	NA	ns
t_{XZ}	3.484	6.719	3.484	7.207	3.484	7.927	NA	NA	ns
t_{ZX}	3.484	6.719	3.484	7.207	3.484	7.927	NA	NA	ns
$t_{INSUPLL}$	o.994		1.143		1.351		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.821	3.186	1.821	3.227	1.821	3.254	NA	NA	ns
t_{XZPLL}	1.848	3.240	1.848	3.283	1.848	3.322	NA	NA	ns
t_{ZXPLL}	1.848	3.240	1.848	3.283	1.848	3.322	NA	NA	ns

Note to Tables 4–91 to 4–96:
(1) Only EP1S25, EP1S30, and EP1S40 devices have the -8 speed grade.