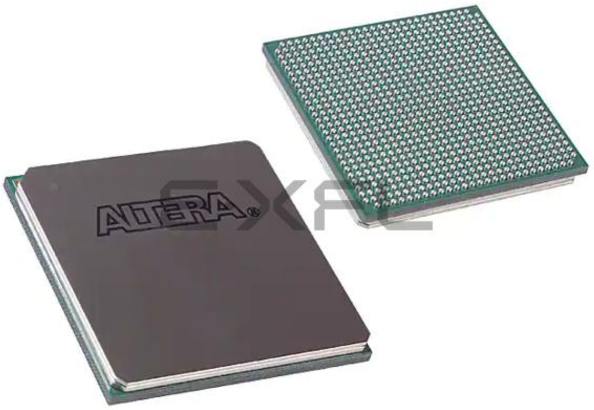
Intel - EP1S30F780C6N Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3247
Number of Logic Elements/Cells	32470
Total RAM Bits	3317184
Number of I/O	597
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s30f780c6n

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Designs.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
“Subheading Title”	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: “Typographic Conventions.”
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
↵	The angled arrow indicates you should press the Enter key.
👣	The feet direct you to more information on a particular topic.

Table 1–1. Stratix Device Features — EP1S10, EP1S20, EP1S25, EP1S30

Feature	EP1S10	EP1S20	EP1S25	EP1S30
LEs	10,570	18,460	25,660	32,470
M512 RAM blocks (32 × 18 bits)	94	194	224	295
M4K RAM blocks (128 × 36 bits)	60	82	138	171
M-RAM blocks (4K × 144 bits)	1	2	2	4
Total RAM bits	920,448	1,669,248	1,944,576	3,317,184
DSP blocks	6	10	10	12
Embedded multipliers *(1)*	48	80	80	96
PLLs	6	6	6	10
Maximum user I/O pins	426	586	706	726

Table 1–2. Stratix Device Features — EP1S40, EP1S60, EP1S80

Feature	EP1S40	EP1S60	EP1S80
LEs	41,250	57,120	79,040
M512 RAM blocks (32 × 18 bits)	384	574	767
M4K RAM blocks (128 × 36 bits)	183	292	364
M-RAM blocks (4K × 144 bits)	4	6	9
Total RAM bits	3,423,744	5,215,104	7,427,520
DSP blocks	14	18	22
Embedded multipliers *(1)*	112	144	176
PLLs	12	12	12
Maximum user I/O pins	822	1,022	1,238

Note to Tables 1–1 and 1–2:

(1) This parameter lists the total number of 9 × 9-bit multipliers for each device. For the total number of 18 × 18-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 2. For the total number of 36 × 36-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 8.

functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 2–14 for more information on LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition, and subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The Stratix LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

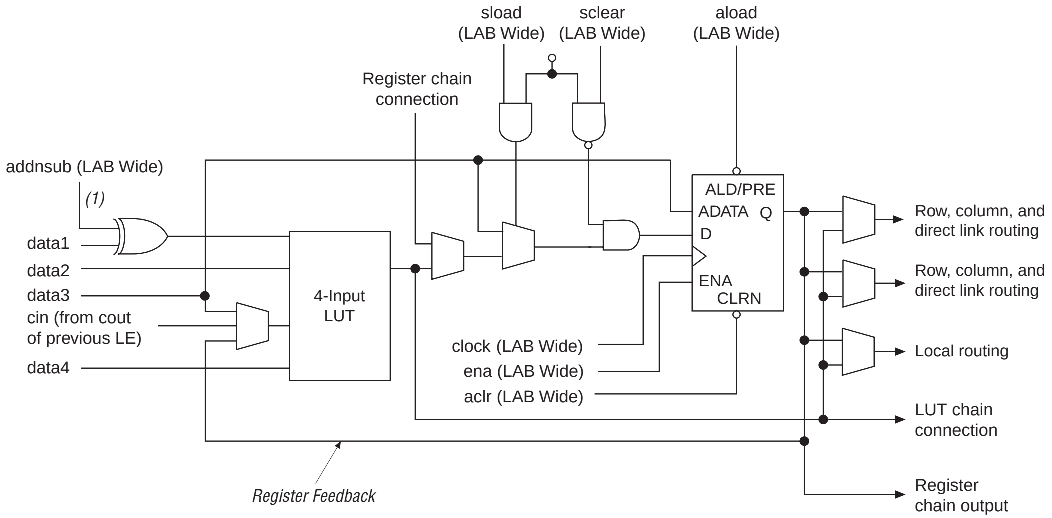
Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0` and `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–6). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

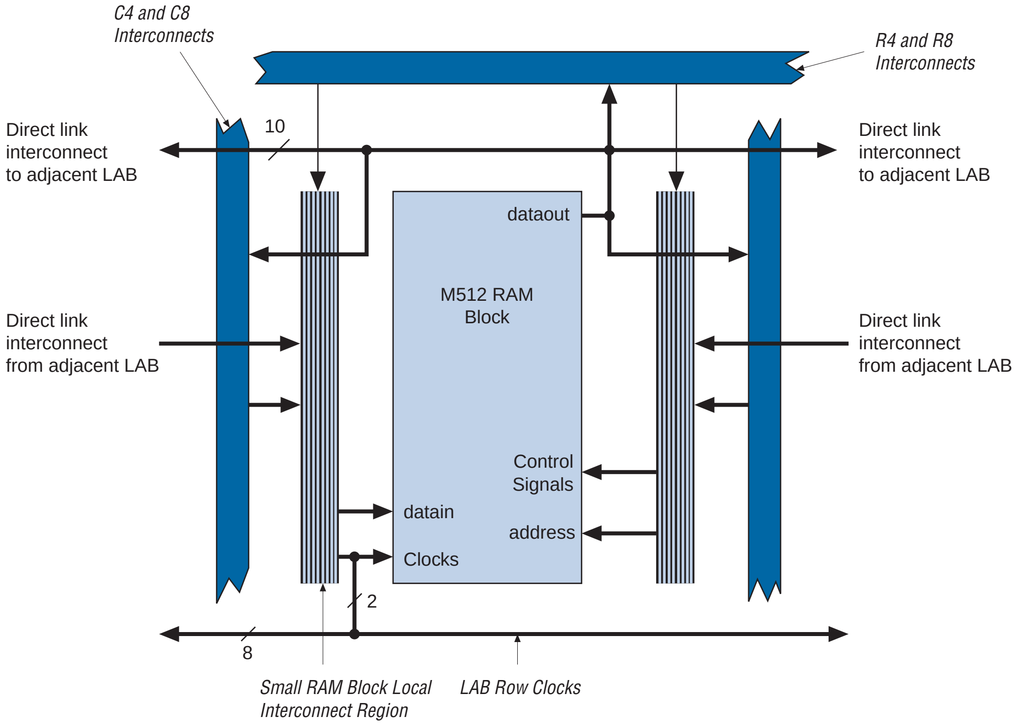
Figure 2–6. LE in Normal Mode



Note to Figure 2–6:

(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Figure 2–16. M512 RAM Block LAB Row Interface



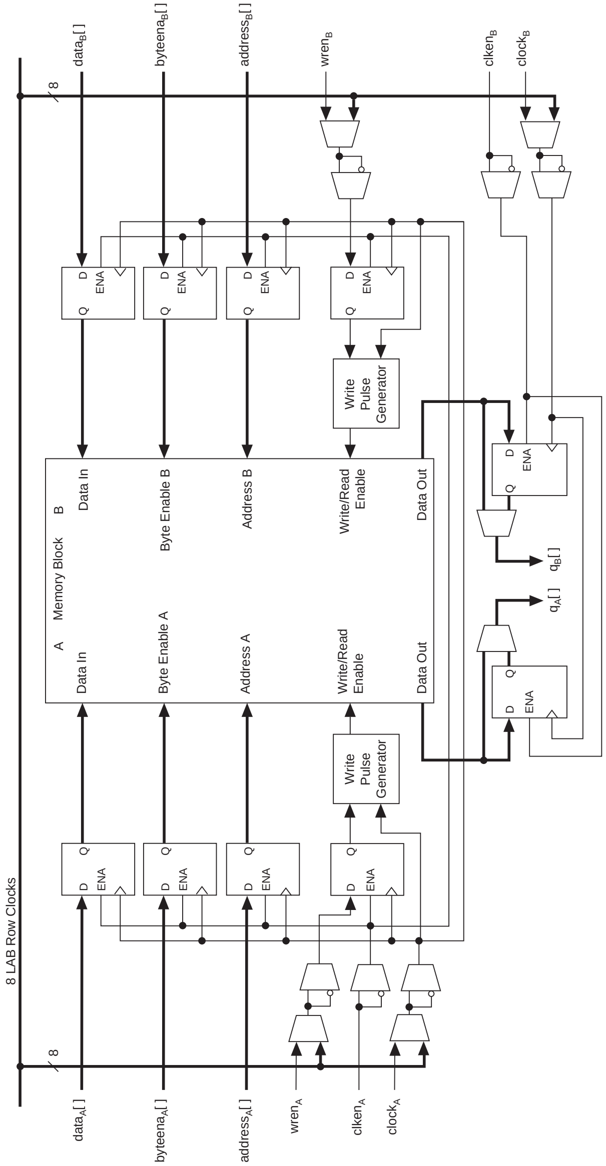
M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Figure 2–25. Input/Output Clock Mode in True Dual-Port Mode Notes (1), (2)



Notes to Figure 2–25:

(1) All registers shown have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these blocks have the same fundamental building block: the multiplier. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix device has two columns of DSP blocks to efficiently implement DSP functions faster than LE-based implementations. Larger Stratix devices have more DSP blocks per column (see Table 2–13). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any matched sign multiplications (either unsigned by unsigned or signed by signed), but the capabilities for dynamic and mixed sign multiplications are handled differently. The following list provides the largest functions that can fit into a single DSP block.

- 36 × 36-bit unsigned by unsigned multiplication
- 36 × 36-bit signed by signed multiplication
- 35 × 36-bit unsigned by signed multiplication
- 36 × 35-bit signed by unsigned multiplication
- 36 × 35-bit signed by dynamic sign multiplication
- 35 × 36-bit dynamic sign by signed multiplication
- 35 × 36-bit unsigned by dynamic sign multiplication
- 36 × 35-bit dynamic sign by unsigned multiplication
- 35 × 35-bit dynamic sign multiplication when the sign controls for each operand are different
- 36 × 36-bit dynamic sign multiplication when the same sign control is used for both operands

☞ This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 2–29 shows one of the columns with surrounding LAB rows.

Figure 2–31. DSP Block Diagram for 9 × 9-Bit Configuration

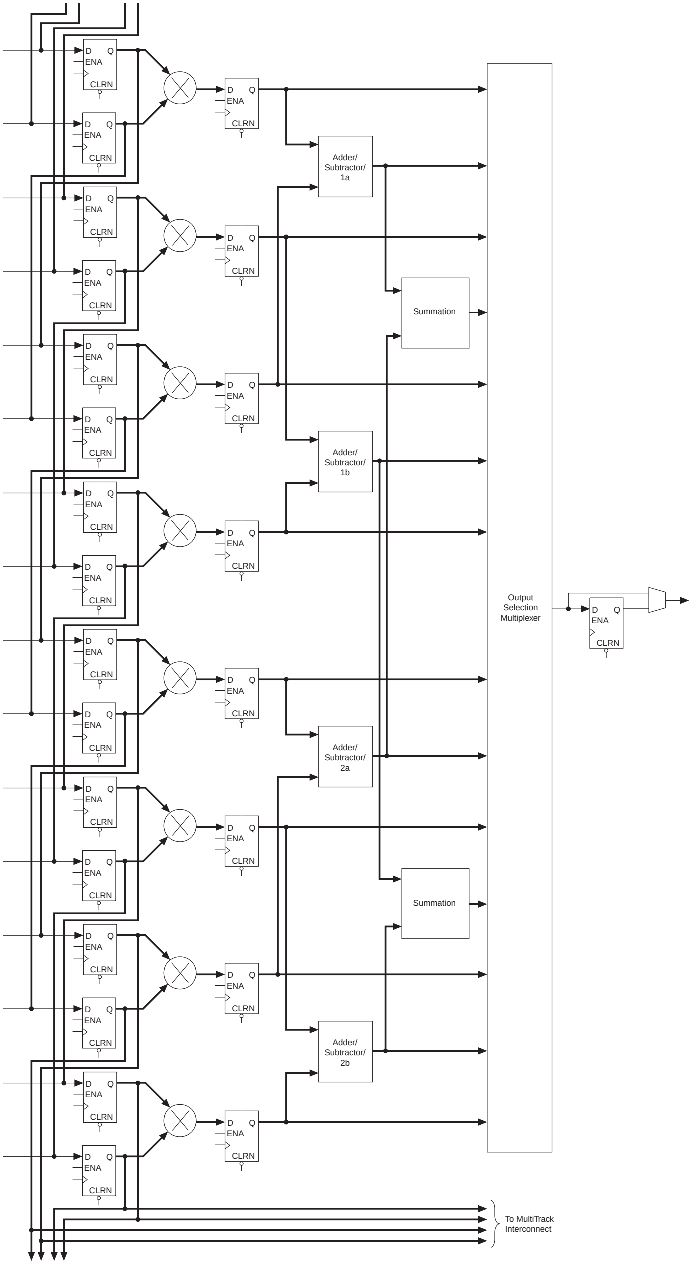
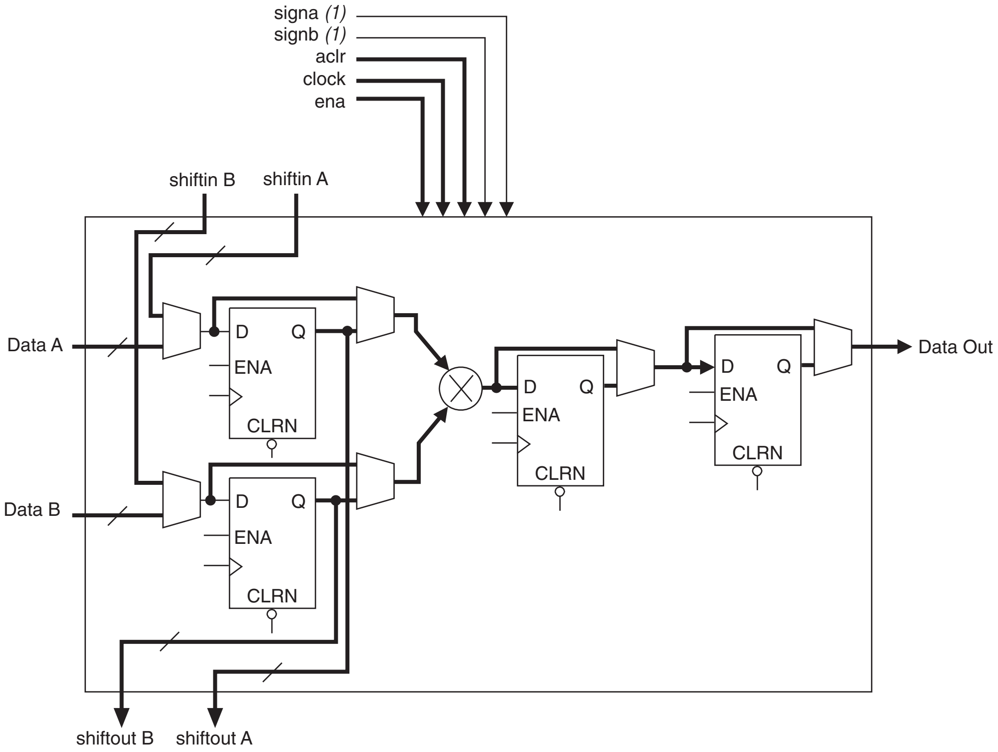


Figure 2–35. Simple Multiplier Mode



Note to Figure 2–35:

(1) These signals are not registered or registered once to match the data path pipeline.

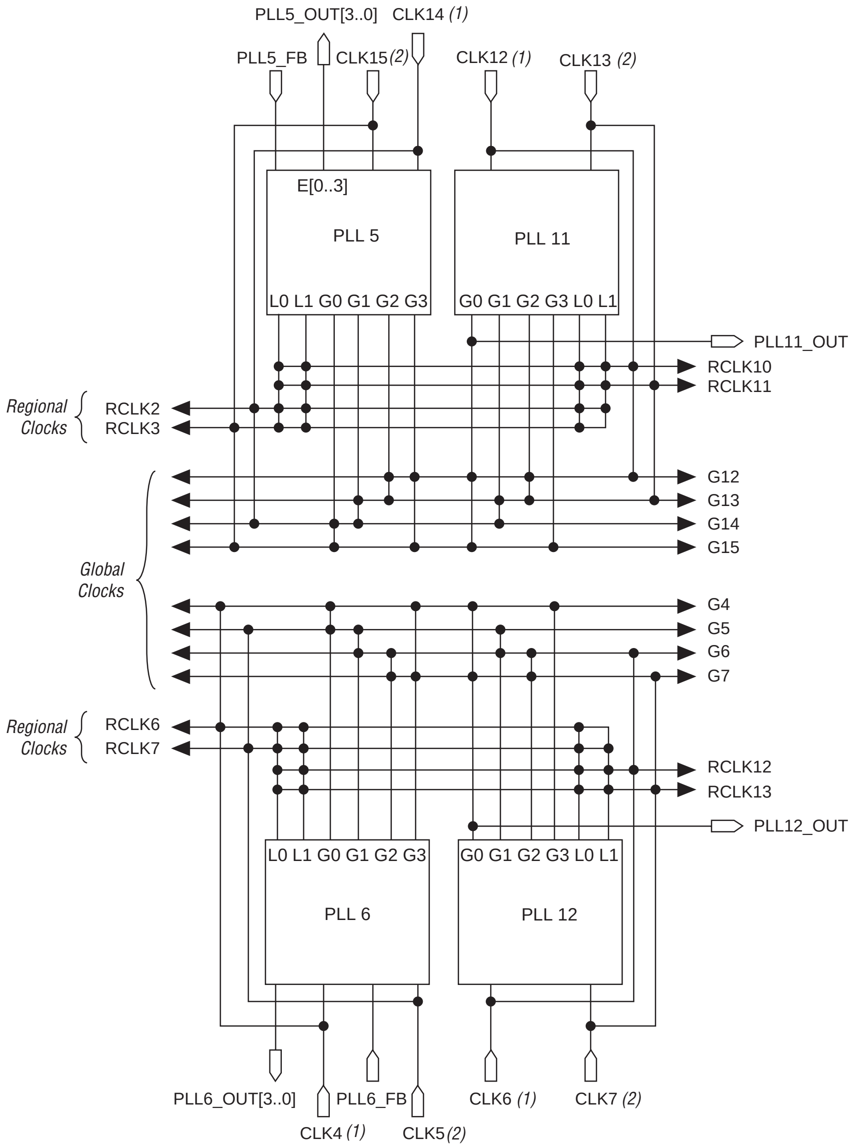
DSP blocks can also implement one 36 × 36-bit multiplier in multiplier mode. DSP blocks use four 18 × 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 × 36-bit multiplier. In 36 × 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 × 36-bit multiplier. Figure 2–36 shows the 36 × 36-bit multiply mode.

There are 16 dedicated clock pins (`CLK[15..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figure 2–42. Enhanced and fast PLL outputs can also drive the global and regional clock networks.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources within the device—IOEs, LEs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–42 shows the 16 dedicated `CLK` pins driving global clock networks.

Figure 2–51. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs Note (1)



Notes to Figure 2–51:

(1) PLLs 1 to 4 and 7 to 10 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs.

(2) `CLK4`, `CLK6`, `CLK12`, and `CLK14` feed the corresponding PLL's `inclk0` port.

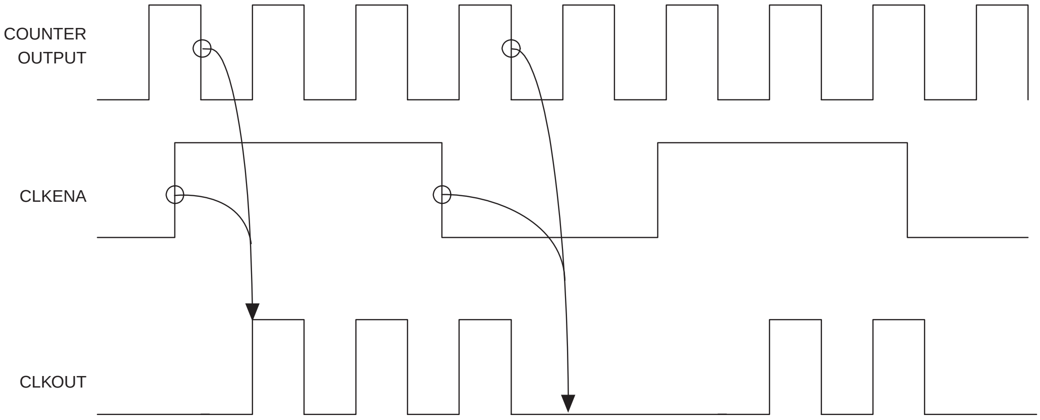
(3) `CLK5`, `CLK7`, `CLK13`, and `CLK15` feed the corresponding PLL's `inclk1` port.

(4) The EP1S40 device in the 780-pin FineLine BGA package does not support PLLs 11 and 12.

resynchronization or relock period. The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The `extclkena` signals work in the same way as the `clkena` signals, but they control the external clock output counters (*e*0, *e*1, *e*2, and *e*3). Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the `FBIN` pin.

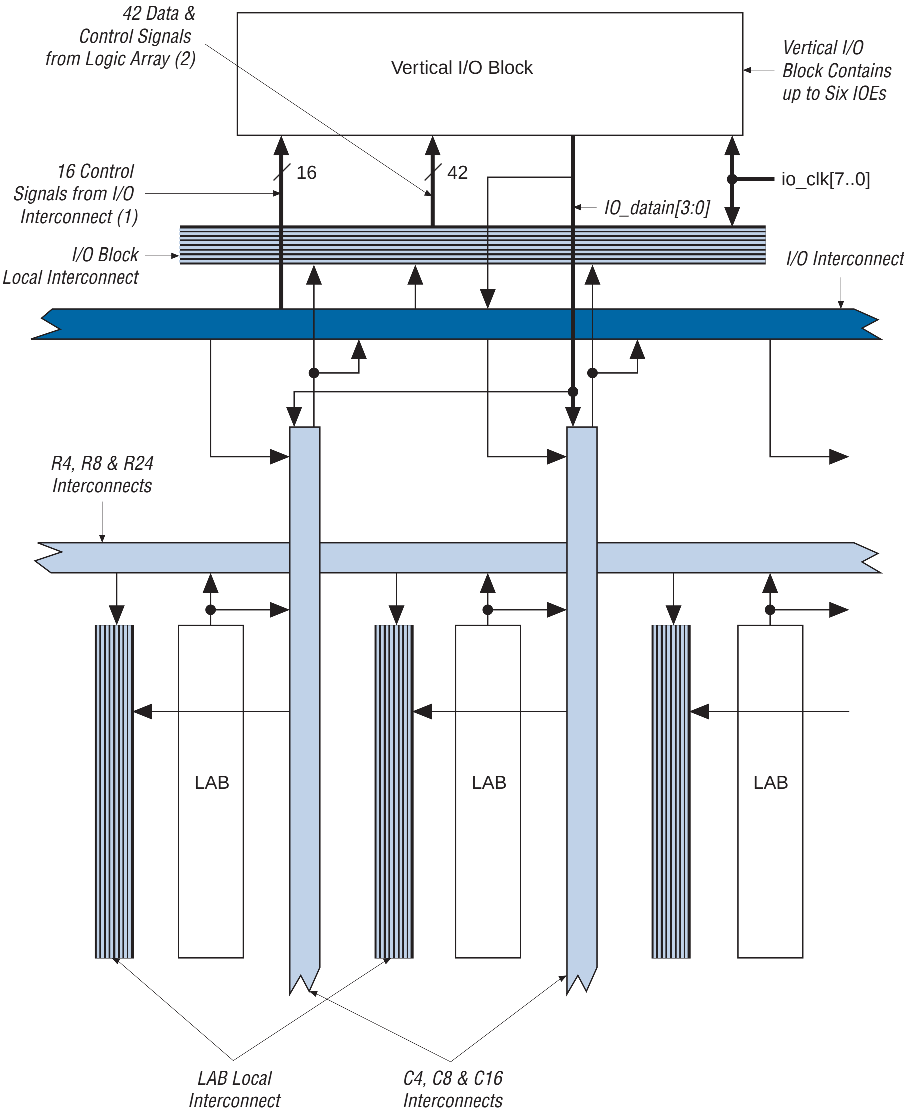
Figure 2–57. extclkena Signals



Fast PLLs

Stratix devices contain up to eight fast PLLs with high-speed serial interfacing ability, along with general-purpose features. Figure 2–58 shows a diagram of the fast PLL.

Figure 2–61. Column I/O Block Connection to the Interconnect

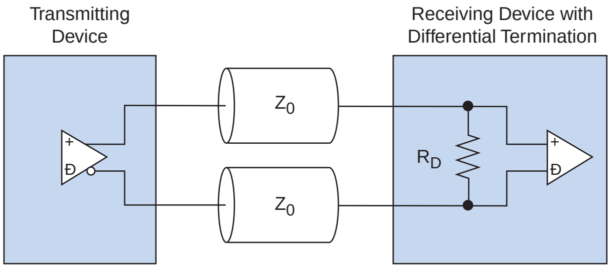


Notes to Figure 2–61:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 42 data and control signals consist of 12 data out lines; six lines each for DDR applications `io_dataouta[5..0]` and `io_dataoutb[5..0]`, six output enables `io_coe[5..0]`, six input clock enables `io_cce_in[5..0]`, six output clock enables `io_cce_out[5..0]`, six clocks `io_cclk[5..0]`, and six clear signals `io_cclr[5..0]`.

Figure 2–71. LVDS Input Differential On-Chip Termination



I/O banks on the left and right side of the device support LVDS receiver (far-end) differential termination.

Table 2–33 shows the Stratix device differential termination support.

Table 2–33. Differential Termination Supported by I/O Banks

Differential Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)
Differential termination *(1)*, *(2)*	LVDS		✓

Notes to Table 2–33:

(1) Clock pin `CLK0`, `CLK2`, `CLK9`, `CLK11`, and pins `FPLL[7..10]CLK` do not support differential termination.

(2) Differential termination is only supported for LVDS because of a 3.3-V V_{CCIO}.

Table 2–34 shows the termination support for different pin types.

Table 2–34. Differential Termination Support Across Pin Types

Pin Type	R_D
Top and bottom I/O banks (3, 4, 7, and 8)	
`DIFFIO_RX[]`	✓
`CLK[0,2,9,11],CLK[4-7],CLK[12-15]`	
`CLK[1,3,8,10]`	✓
`FCLK`	
`FPLL[7..10]CLK`	

The differential on-chip resistance at the receiver input buffer is 118 Ω ±20 %.

Table 2–37 shows the number of channels that each fast PLL can clock in EP1S10, EP1S20, and EP1S25 devices. Tables 2–38 through Table 2–41 show this information for EP1S30, EP1S40, EP1S60, and EP1S80 devices.

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 1 of 2) *Note (1)*

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S10	484-pin FineLine BGA	Transmitter *(2)*	20	840 *(4)*	5	5	5	5
				840 *(3)*	10	10	10	10
		Receiver	20	840 *(4)*	5	5	5	5
				840 *(3)*	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter *(2)*	36	624 *(4)*	9	9	9	9
				624 *(3)*	18	18	18	18
		Receiver	36	624 *(4)*	9	9	9	9
				624 *(3)*	18	18	18	18
	780-pin FineLine BGA	Transmitter *(2)*	44	840 *(4)*	11	11	11	11
				840 *(3)*	22	22	22	22
		Receiver	44	840 *(4)*	11	11	11	11
				840 *(3)*	22	22	22	22
EP1S20	484-pin FineLine BGA	Transmitter *(2)*	24	840 *(4)*	6	6	6	6
				840 *(3)*	12	12	12	12
		Receiver	20	840 *(4)*	5	5	5	5
				840 *(3)*	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter *(2)*	48	624 *(4)*	12	12	12	12
				624 *(3)*	24	24	24	24
		Receiver	50	624 *(4)*	13	12	12	13
				624 *(3)*	25	25	25	25
	780-pin FineLine BGA	Transmitter *(2)*	66	840 *(4)*	17	16	16	17
				840 *(3)*	33	33	33	33
		Receiver	66	840 *(4)*	17	16	16	17
				840 *(3)*	33	33	33	33

configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

`PORSEL` is a dedicated input pin used to select POR delay times of 2 ms or 100 ms during power-up. When the `PORSEL` pin is connected to ground, the POR time is 100 ms; when the `PORSEL` pin is connected to V_{CC}, the POR time is 2 ms.

The `nIO_PULLUP` pin enables a built-in weak pull-up resistor to pull all user I/O pins to V_{CCIO} before and during device configuration. If `nIO_PULLUP` is connected to V_{CC} during configuration, the weak pull-ups on all user I/O pins are disabled. If connected to ground, the pull-ups are enabled during configuration. The `nIO_PULLUP` pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

`VCCSEL` is a dedicated input that is used to choose whether all dedicated configuration and JTAG input pins can accept 1.5 V/1.8 V or 2.5 V/3.3 V during configuration. A logic low sets 3.3 V/2.5 V, and a logic high sets 1.8 V/1.5 V. `VCCSEL` affects the following pins: `TDI`, `TMS`, `TCK`, `TRST`, `MSEL0`, `MSEL1`, `MSEL2`, `nCONFIG`, `nCE`, `DCLK`, `PLL_ENA`, `CONF_DONE`, `nSTATUS`. The `VCCSEL` pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

The `VCCSEL` signal does not control the dual-purpose configuration pins such as the `DATA[7..0]` and PPA pins (`nWS`, `nRS`, `CS`, `nCS`, and `RDYnBSY`). During configuration, these dual-purpose pins will drive out voltage levels corresponding to the V_{CCIO} supply voltage that powers the I/O bank containing the pin. After configuration, the dual-purpose pins use I/O standards specified in the user design.

`TDO` and `nCEO` drive out at the same voltages as the V_{CCIO} supply that powers the I/O bank containing the pin. Users must select the V_{CCIO} supply for bank containing `TDO` accordingly. For example, when using the ByteBlaster™ MV cable, the V_{CCIO} for the bank containing `TDO` must be powered up at 3.3 V.

Table 4–47. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PIPE2OUTREG2ADD}$		2,002		2,203		2,533		2,980	ps
$t_{PIPE2OUTREG4ADD}$		2,899		3,189		3,667		4,314	ps
t_{PD9}		3,709		4,081		4,692		5,520	ps
t_{PD18}		4,795		5,275		6,065		7,135	ps
t_{PD36}		7,495		8,245		9,481		11,154	ps
t_{CLR}	450		500		575		676		ps
t_{CLKHL}	1,350		1,500		1,724		2,029		ps

Table 4–48. M512 Block Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{M512RC}		3,340		3,816		4,387		5,162	ps
t_{M512WC}		3,138		3,590		4,128		4,860	ps
$t_{M512WERESU}$	110		123		141		166		ps
$t_{M512WEREH}$	34		38		43		51		ps
$t_{M512CLKENSU}$	215		215		247		290		ps
$t_{M512CLKENH}$	–70		–70		–81		–95		ps
$t_{M512DATASU}$	110		123		141		166		ps
$t_{M512DATAH}$	34		38		43		51		ps
$t_{M512WADDRSU}$	110		123		141		166		ps
$t_{M512WADDRH}$	34		38		43		51		ps
$t_{M512RADDRSU}$	110		123		141		166		ps
$t_{M512RADDRH}$	34		38		43		51		ps
$t_{M512DATACO1}$		424		472		541		637	ps
$t_{M512DATACO2}$		3,366		3,846		4,421		5,203	ps
$t_{M512CLKHL}$	1,000		1,111		1,190		1,400		ps
$t_{M512CLR}$	170		189		217		255		ps

Table 4–102. Reporting Methodology For Minimum Timing For Single-Ended Output Pins (Part 2 of 2) Notes (1), (2), (3)

I/O Standard	Loading and Termination							Measurement Point
	R_{UP} Ω	R_{DN} Ω	R_S Ω	R_T Ω	V_{CCIO} (V)	VTT (V)	C_L (pF)	V_{MEAS}
3.3-V CTT	–	–	25	50	3.600	1.650	30	1.650

Notes to Table 4–102:

(1) Input measurement point at internal node is 0.5 × V_{CCINT}.

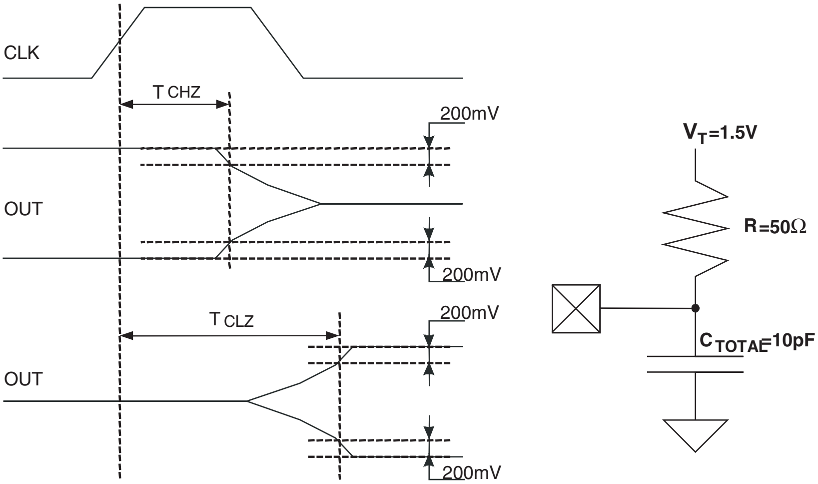
(2) Output measuring point for data is V_{MEAS}. When two values are given, the first is the measurement point on the rising edge and the other is for the falling edge.

(3) Input stimulus edge rate is 0 to V_{CCINT} in 0.5 ns (internal signal) from the driver preceding the I/O buffer.

(4) The first value is for the output rising edge and the second value is for the output falling edge. The hyphen (-) indicates infinite resistance or disconnection.

Figure 4–8 shows the measurement setup for output disable and output enable timing. The T_{CHZ} stands for clock to high Z time delay and is the same as T_{XZ}. The T_{CLZ} stands for clock to low Z (driving) time delay and is the same as T_{ZX}.

Figure 4–8. Measurement Setup for T_{XZ} and T_{ZX}



Tables 4–105 through 4–108 show the output adder delays associated with column and row I/O pins for both fast and slow slew rates. If an I/O standard is selected other than 3.3-V LVTTL 4mA or LVCMOS 2 mA with a fast slew rate, add the selected delay to the external t_{OUTCO}, $t_{OUTCOPLL}$, t_{XZ}, t_{ZX}, t_{XZPLL}, and t_{ZXPLL} I/O parameters shown in Table 4–55 on page 4–36 through Table 4–96 on page 4–56.

Table 4–105. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2)

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,895		1,990		1,990		1,990	ps
	4 mA		956		1,004		1,004		1,004	ps
	8 mA		189		198		198		198	ps
	12 mA		0		0		0		0	ps
	24 mA		–157		–165		–165		–165	ps
3.3-V LVTTL	4 mA		1,895		1,990		1,990		1,990	ps
	8 mA		1,347		1,414		1,414		1,414	ps
	12 mA		636		668		668		668	ps
	16 mA		561		589		589		589	ps
	24 mA		0		0		0		0	ps
2.5-V LVTTL	2 mA		2,517		2,643		2,643		2,643	ps
	8 mA		834		875		875		875	ps
	12 mA		504		529		529		529	ps
	16 mA		194		203		203		203	ps
1.8-V LVTTL	2 mA		1,304		1,369		1,369		1,369	ps
	8 mA		960		1,008		1,008		1,008	ps
	12 mA		960		1,008		1,008		1,008	ps
1.5-V LVTTL	2 mA		6,680		7,014		7,014		7,014	ps
	4 mA		3,275		3,439		3,439		3,439	ps
	8 mA		1,589		1,668		1,668		1,668	ps
GTL			16		17		17		17	ps
GTL+			9		9		9		9	ps
3.3-V PCI			50		52		52		52	ps
3.3-V PCI-X 1.0			50		52		52		52	ps
Compact PCI			50		52		52		52	ps
AGP 1×			50		52		52		52	ps
AGP 2×			1,895		1,990		1,990		1,990	ps

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 2 of 4) Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (Clock frequency) (PCML) $f_{HSCLK} = f_{HSDR} / W$	W = 4 to 30 (Serdes used)	10		100	10		100	10		77.75	10		77.75	MHz
	W = 2 (Serdes bypass)	50		200	50		200	50		150	50		150	MHz
	W = 2 (Serdes used)	150		200	150		200	150		155.5	150		155.5	MHz
	W = 1 (Serdes bypass)	100		250	100		250	100		200	100		200	MHz
	W = 1 (Serdes used)	300		400	300		400	300		311	300		311	MHz
f_{HSDR} Device operation (PCML)	J = 10	300		400	300		400	300		311	300		311	Mbps
	J = 8	300		400	300		400	300		311	300		311	Mbps
	J = 7	300		400	300		400	300		311	300		311	Mbps
	J = 4	300		400	300		400	300		311	300		311	Mbps
	J = 2	100		400	100		400	100		300	100		300	Mbps
	J = 1	100		250	100		250	100		200	100		200	Mbps
TCCS	All			200			200			300			300	ps