Altera - EP1S30F780C7 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	597
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1s30f780c7

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Chapter	Date/Version	Changes Made
4		• Table 4–48 on page 4–30: added rows $t_{M512CLKSENSU}$ and $t_{M512CLKENH}$, and updated symbol names. • Updated power-up current (ICCINT) required to power a Stratix device on page 4–17. • Updated Table 4–37 on page 4–22 through Table 4–43 on page 4–27. • Table 4–49 on page 4–31: added rows $t_{M4KCLKENSU}$, $t_{M4KCLKENH}$, $t_{M4KBESU}$, and t_{M4KBEH}, deleted rows $t_{M4KRADDRASU}$ and $t_{M4KRADDRH}$, and updated symbol names. • Table 4–50 on page 4–31: added rows $t_{MRAMCLKENSU}$, $t_{MRAMCLKENH}$, $t_{MRAMBESU}$, and $t_{MRAMBEH}$, deleted rows $t_{MRAMADDRASU}$ and $t_{MRAMRADDRH}$, and updated symbol names. • Table 4–52 on page 4–34: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. • Table 4–52 on page 4–34: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. • Table 4–53 on page 4–34: updated table and added rows t_{XZPLL} and t_{ZXPLL}. • Updated Note 2 in Table 4–53 on page 4–34. • Table 4–54 on page 4–35: updated table, deleted “Conditions” column, and added rows t_{XZPLL} and t_{ZXPLL}. • Updated Note 2 in Table 4–54 on page 4–35. • Deleted Note 2 from Table 4–55 on page 4–36 through Table 4–66 on page 4–41. • Updated Table 4–55 on page 4–36 through Table 4–96 on page 4–56. Added rows T_{XZ}, T_{ZX}, T_{XZPLL}, and T_{ZXPLL}. • Added Note 4 to Table 4–101 on page 4–62. • Deleted Note 1 from Table 4–67 on page 4–42 through Table 4–84 on page 4–50. • Added new section “I/O Timing Measurement Methodology” on page 4–60. • Deleted Note 1 from Table 4–67 on page 4–42 through Table 4–84 on page 4–50. • Deleted Note 2 from Table 4–85 on page 4–51 through Table 4–96 on page 4–56. • Added Note 4 to Table 4–101 on page 4–62. • Table 4–102 on page 4–64: updated table and added Note 4. • Updated description of “External I/O Delay Parameters” on page 4–66. • Added Note 1 to Table 4–109 on page 4–73 and Table 4–110 on page 4–74. • Updated Table 4–103 on page 4–66 through Table 4–110 on page 4–74. • Deleted Note 2 from Table 4–103 on page 4–66 through Table 4–106 on page 4–69. • Added new paragraph about output adder delays on page 4–68. • Updated Table 4–110 on page 4–74. • Added Note 1 to Table 4–111 through Table 4–113 on page 4–75.

Chapter	Date/Version	Changes Made
4	October 2003, v2.1	- Added -8 speed grade information. - Updated performance information in Table 4–36. - Updated timing information in Tables 4–55 through 4–96. - Updated delay information in Tables 4–103 through 4–108. - Updated programmable delay information in Tables 4–100 and 4–103.
	July 2003, v2.0	- Updated clock rates in Tables 4–114 through 4–123. - Updated speed grade information in the introduction on page 4-1. - Corrected figures 4-1 & 4-2 and Table 4-9 to reflect how VID and VOD are specified. - Added note 6 to Table 4-32. - Updated Stratix Performance Table 4-35. - Updated EP1S60 and EP1S80 timing parameters in Tables 4-82 to 4-93. The Stratix timing models are final for all devices. - Updated Stratix IOE programmable delay chains in Tables 4-100 to 4-101. - Added single-ended I/O standard output pin delay adders for loading in Table 4-102. - Added spec for FPLL[10..7]CLK pins in Tables 4-104 and 4-107. - Updated high-speed I/O specification for J=2 in Tables 4-114 and 4-115. - Updated EPLL specification and fast PLL specification in Tables 4-116 to 4-120.
5	September 2004, v2.1	- Updated reference to device pin-outs on page 5–1 to indicate that device pin-outs are no longer included in this manual and are now available on the Altera web site.
	April 2003, v1.0	- No new changes in Stratix Device Handbook v2.0.

1. Introduction

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Introduction

The Stratix® family of FPGAs is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities of up to 79,040 logic elements (LEs) and up to 7.5 Mbits of RAM. Stratix devices offer up to 22 digital signal processing (DSP) blocks with up to 176 (9-bit × 9-bit) embedded multipliers, optimized for DSP applications that enable efficient implementation of high-performance filters and multipliers. Stratix devices support various I/O standards and also offer a complete clock management solution with its hierarchical clock structure with up to 420-MHz performance and up to 12 phase-locked loops (PLLs).

The following shows the main sections in the Stratix Device Family Data Sheet:

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–5 and 2–6 summarize the possible M4K RAM block configurations.

Table 2–5. M4K RAM Block Configurations (Simple Dual-Port)

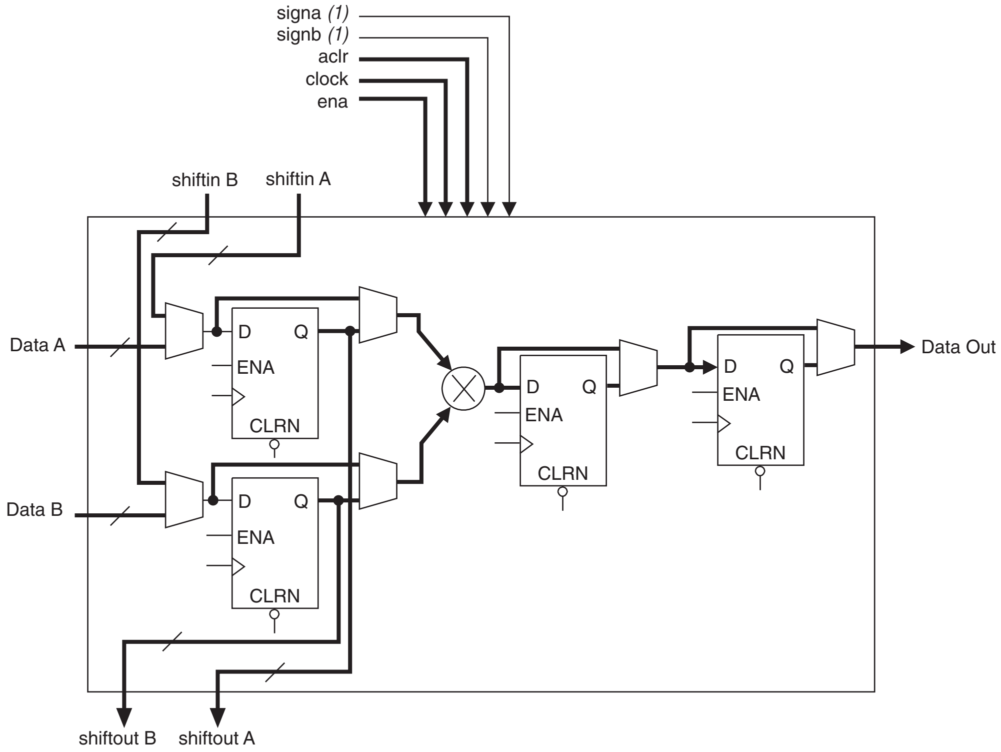
Read Port	Write Port								
	4K × 1	**2K × 2**	**1K × 4**	**512 × 8**	**256 × 16**	**128 × 32**	**512 × 9**	**256 × 18**	**128 × 36**
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

Table 2–6. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	**2K × 2**	**1K × 4**	**512 × 8**	**256 × 16**	**512 × 9**	**256 × 18**
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

When the M4K RAM block is configured as a shift register block, you can create a shift register up to 4,608 bits ($w \times m \times n$).

Figure 2–35. Simple Multiplier Mode



Note to Figure 2–35:

(1) These signals are not registered or registered once to match the data path pipeline.

DSP blocks can also implement one 36 × 36-bit multiplier in multiplier mode. DSP blocks use four 18 × 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 × 36-bit multiplier. In 36 × 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 × 36-bit multiplier. Figure 2–36 shows the 36 × 36-bit multiply mode.

provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–18 shows the PLLs available for each Stratix device.

Table 2–18. Stratix Device PLL Availability

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5 (1)	6 (1)	11 (2)	12 (2)
EP1S10	✓	✓	✓	✓					✓	✓		
EP1S20	✓	✓	✓	✓					✓	✓		
EP1S25	✓	✓	✓	✓					✓	✓		
EP1S30	✓	✓	✓	✓	✓ (3)	✓ (3)	✓ (3)	✓ (3)	✓	✓		
EP1S40	✓	✓	✓	✓	✓ (3)	✓ (3)	✓ (3)	✓ (3)	✓	✓	✓ (3)	✓ (3)
EP1S60	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP1S80	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 2–18:

(1) PLLs 5 and 6 each have eight single-ended outputs or four differential outputs.

(2) PLLs 11 and 12 each have one single-ended output.

(3) EP1S30 and EP1S40 devices do not support these PLLs in the 780-pin FineLine BGA® package.

External Clock Inputs

Each fast PLL supports single-ended or differential inputs for source synchronous transmitters or for general-purpose use. Source-synchronous receivers support differential clock inputs. The fast PLL inputs are fed by `CLK[0..3]`, `CLK[8..11]`, and `FPLL[7..10]CLK` pins, as shown in Figure 2–50 on page 2–85.

Table 2–22 shows the I/O standards supported by fast PLL input pins.

Table 2–22. Fast PLL Port I/O Standards (Part 1 of 2)

I/O Standard	Input	
	INCLK	PLLENABLE
LVTTL	✓	✓
LVCMOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X 1.0		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	
Differential SSTL		
3.3-V GTL		
3.3-V GTL+	✓	
1.5-V HSTL Class I	✓	
1.5-V HSTL Class II		
1.8-V HSTL Class I	✓	
1.8-V HSTL Class II		
SSTL-18 Class I	✓	
SSTL-18 Class II		
SSTL-2 Class I	✓	

Control Signals

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL.

If the input clock stops and causes the PLL to lose lock, then the PLL must be reset for correct phase shift operation.

For more information on high-speed differential I/O support, see "High-Speed Differential I/O Support" on page 2–130.

I/O Structure

IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Differential on-chip termination for LVDS I/O standard
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double-data rate (DDR) Registers

The IOE in Stratix devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–59 shows the Stratix IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Stratix devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 2–73). Figure 2–62 illustrates the signal paths through the I/O block.

Figure 2–62. Signal Path through the I/O Block

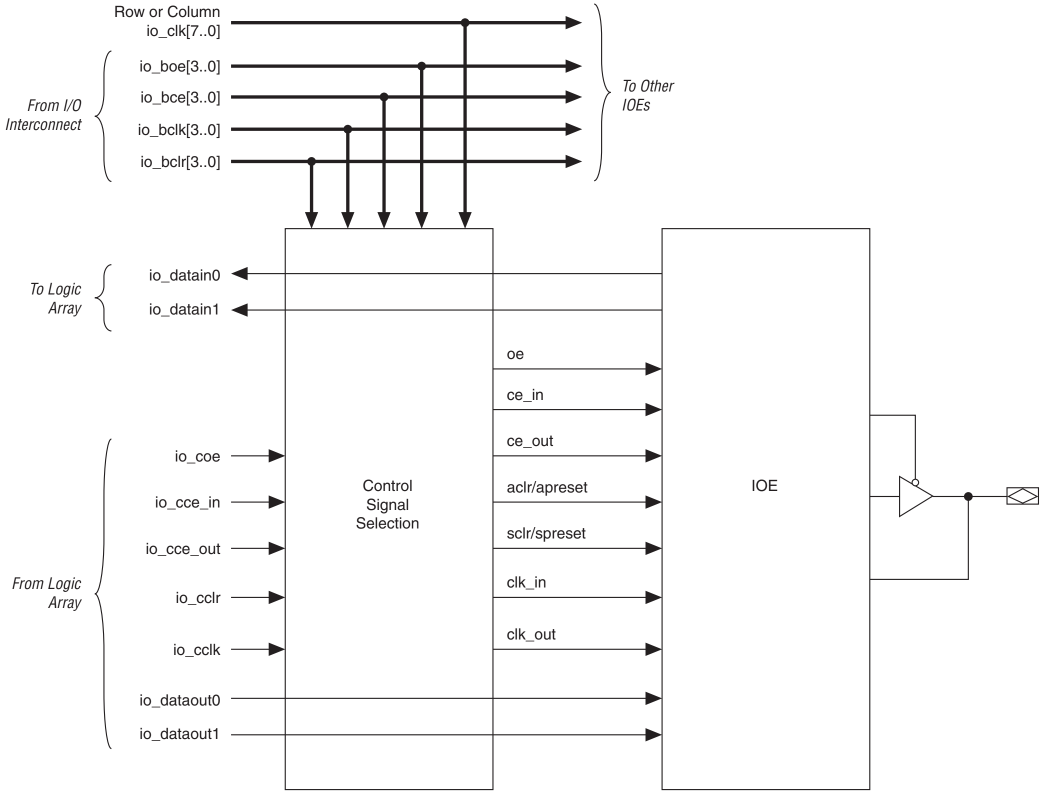


Figure 3–5. External Temperature-Sensing Diode

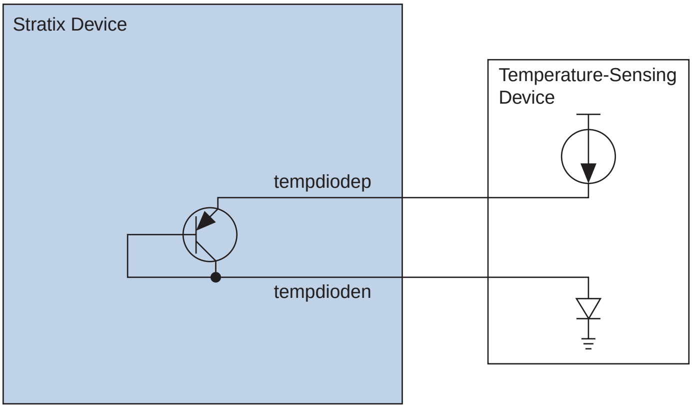


Table 3–6 shows the specifications for bias voltage and current of the Stratix temperature sensing diode.

Table 3–6. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
I_{BIAS} high	80	100	120	µA
I_{BIAS} low	8	10	12	µA
$V_{BP} – V_{BN}$	0.3		0.9	V
V_{BN}		0.7		V
Series resistance			3	W

The temperature-sensing diode works for the entire operating range shown in Figure 3–6.

Figure 3–6. Temperature vs. Temperature-Sensing Diode Voltage

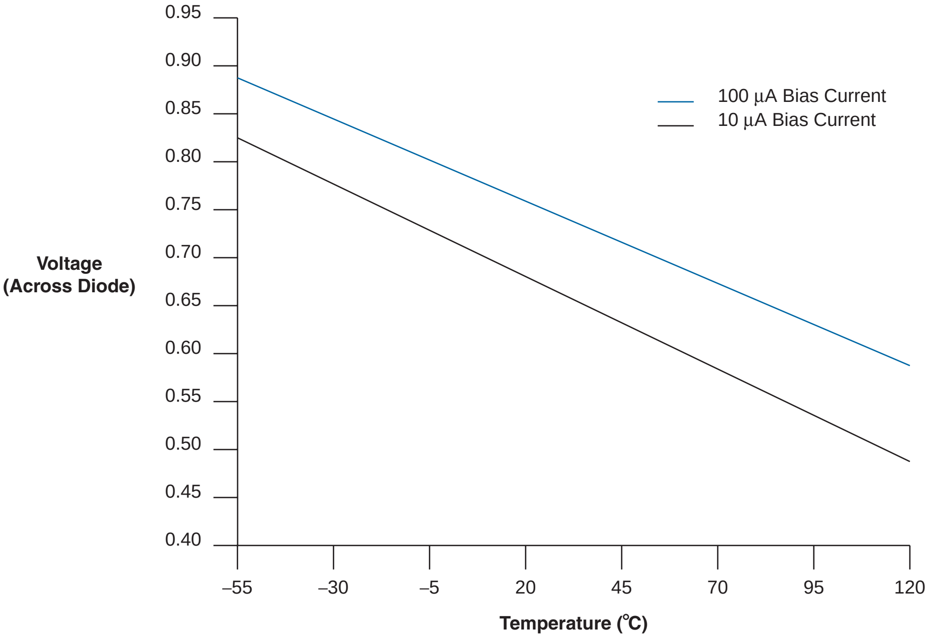


Table 4–2. Stratix Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	(4)	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	(4)	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	(4)	1.4	1.6	V
V_I	Input voltage	(3), (6)	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C

Table 4–3. Stratix Device DC Operating Conditions Note (7) (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V (8)	–10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V (8)	–10		10	μA
I_{CC0}	V_{CC} supply current (standby) (All memory blocks in power-down mode)	V_I = ground, no load, no toggling inputs				mA
		EP1S10. V_I = ground, no load, no toggling inputs		37		mA
		EP1S20. V_I = ground, no load, no toggling inputs		65		mA
		EP1S25. V_I = ground, no load, no toggling inputs		90		mA
		EP1S30. V_I = ground, no load, no toggling inputs		114		mA
		EP1S40. V_I = ground, no load, no toggling inputs		145		mA
		EP1S60. V_I = ground, no load, no toggling inputs		200		mA
		EP1S80. V_I = ground, no load, no toggling inputs		277		mA

Table 4–28. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(3)*			0.4	V

Table 4–29. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(3)*			0.4	V

Table 4–30. 1.5-V Differential HSTL Class I & Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 4–87. EP1S60 External I/O Timing on Column Pins Using Global Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.000		2.152		2.441		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.051	5.900	3.051	6.340	3.051	6.977	NA	NA	ns
t_{XZ}	2.991	5.774	2.991	6.208	2.991	6.853	NA	NA	ns
t_{ZX}	2.991	5.774	2.991	6.208	2.991	6.853	NA	NA	ns
$t_{INSUPLL}$	1.315		1.362		1.543		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.029	2.196	1.029	2.303	1.029	2.323	NA	NA	ns
t_{XZPLL}	0.969	2.070	0.969	2.171	0.969	2.199	NA	NA	ns
t_{ZXPLL}	0.969	2.070	0.969	2.171	0.969	2.199	NA	NA	ns

Table 4–88. EP1S60 External I/O Timing on Row Pins Using Fast Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.144		3.393		3.867		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.643	5.275	2.643	5.654	2.643	6.140	NA	NA	ns
t_{XZ}	2.670	5.329	2.670	5.710	2.670	6.208	NA	NA	ns
t_{ZX}	2.670	5.329	2.670	5.710	2.670	6.208	NA	NA	ns

Figure 4–6 shows the case where four IOE registers are located in two different I/O banks.

Figure 4–6. I/O Skew Across Two I/O Banks

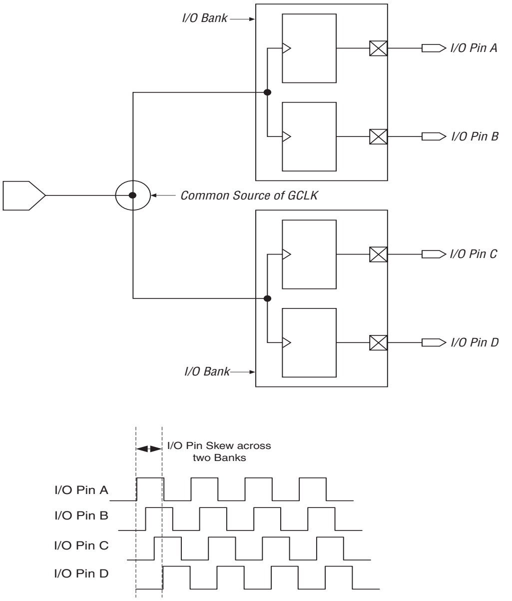


Table 4–97 defines the timing parameters used to define the timing for horizontal I/O pins (side banks 1, 2, 5, 6) and vertical I/O pins (top and bottom banks 3, 4, 7, 8). The timing parameters define the skew within an I/O bank, across two neighboring I/O banks on the same side of the device, across all horizontal I/O banks, across all vertical I/O banks, and the skew for the overall device.

Table 4–97. Output Pin Timing Skew Definitions (Part 1 of 2)

Symbol	Definition
t_{SB_HIO}	Row I/O (HIO) within one I/O bank *(1)*
t_{SB_VIO}	Column I/O (VIO) within one I/O bank *(1)*
t_{SS_HIO}	Row I/O (HIO) same side of the device, across two banks *(2)*
t_{SS_VIO}	Column I/O (VIO) same side of the device, across two banks *(2)*

Table 4–107. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	4 mA		1,822		1,913		1,913		1,913	ps
	8 mA		1,586		1,665		1,665		1,665	ps
	12 mA		686		720		720		720	ps
	16 mA		630		662		662		662	ps
	24 mA		0		0		0		0	ps
2.5-V LVTTL	2 mA		2,925		3,071		3,071		3,071	ps
	8 mA		1,496		1,571		1,571		1,571	ps
	12 mA		937		984		984		984	ps
	16 mA		1,003		1,053		1,053		1,053	ps
1.8-V LVTTL	2 mA		7,101		7,456		7,456		7,456	ps
	8 mA		3,620		3,801		3,801		3,801	ps
	12 mA		3,109		3,265		3,265		3,265	ps
1.5-V LVTTL	2 mA		10,941		11,488		11,488		11,488	ps
	4 mA		7,431		7,803		7,803		7,803	ps
	8 mA		5,990		6,290		6,290		6,290	ps
GTL			–959		–1,007		–1,007		–1,007	ps
GTL+			–438		–460		–460		–460	ps
3.3-V PCI			660		693		693		693	ps
3.3-V PCI-X 1.0			660		693		693		693	ps
Compact PCI			660		693		693		693	ps
AGP 1×			660		693		693		693	ps
AGP 2×			288		303		303		303	ps
CTT			631		663		663		663	ps
SSTL-3 Class I			301		316		316		316	ps
SSTL-3 Class II			–359		–377		–377		–377	ps
SSTL-2 Class I			523		549		549		549	ps
SSTL-2 Class II			–49		–51		–51		–51	ps
SSTL-18 Class I			2,315		2,431		2,431		2,431	ps
SSTL-18 Class II			723		759		759		759	ps
1.5-V HSTL Class I			1,687		1,771		1,771		1,771	ps
1.5-V HSTL Class II			1,095		1,150		1,150		1,150	ps
1.8-V HSTL Class I			599		629		678		744	ps
1.8-V HSTL Class II			87		102		102		102	ps

Table 4–116. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	422	390	390	MHz
2.5 V	422	422	390	390	MHz
1.8 V	422	422	390	390	MHz
1.5 V	422	422	390	390	MHz
LVCMOS	422	422	390	390	MHz
GTL+	300	250	200	200	MHz
SSTL-3 Class I	400	350	300	300	MHz
SSTL-3 Class II	400	350	300	300	MHz
SSTL-2 Class I	400	350	300	300	MHz
SSTL-2 Class II	400	350	300	300	MHz
SSTL-18 Class I	400	350	300	300	MHz
SSTL-18 Class II	400	350	300	300	MHz
1.5-V HSTL Class I	400	350	300	300	MHz
1.8-V HSTL Class I	400	350	300	300	MHz
CTT	300	250	200	200	MHz
Differential 1.5-V HSTL C1	400	350	300	300	MHz
LVPECL *(1)*	645	645	640	640	MHz
PCML *(1)*	300	275	275	275	MHz
LVDS *(1)*	645	645	640	640	MHz
HyperTransport technology *(1)*	500	500	450	450	MHz

Table 4–117. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages (Part 1 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz
LVCMOS	422	390	390	MHz
GTL	250	200	200	MHz

Table 4–117. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
GTL+	250	200	200	MHz
SSTL-3 Class I	300	250	250	MHz
SSTL-3 Class II	300	250	250	MHz
SSTL-2 Class I	300	250	250	MHz
SSTL-2 Class II	300	250	250	MHz
SSTL-18 Class I	300	250	250	MHz
SSTL-18 Class II	300	250	250	MHz
1.5-V HSTL Class I	300	180	180	MHz
1.5-V HSTL Class II	300	180	180	MHz
1.8-V HSTL Class I	300	180	180	MHz
1.8-V HSTL Class II	300	180	180	MHz
3.3-V PCI	422	390	390	MHz
3.3-V PCI-X 1.0	422	390	390	MHz
Compact PCI	422	390	390	MHz
AGP 1×	422	390	390	MHz
AGP 2×	422	390	390	MHz
CTT	250	180	180	MHz
Differential 1.5-V HSTL C1	300	180	180	MHz
LVPECL *(1)*	422	400	400	MHz
PCML *(1)*	215	200	200	MHz
LVDS *(1)*	422	400	400	MHz
HyperTransport technology *(1)*	422	400	400	MHz

Table 4–118. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[10..7]CLK Pins in Wire-Bond Packages (Part 1 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz

PLL Specifications

Tables 4–127 through 4–129 describe the Stratix device enhanced PLL specifications.

Table 4–127. Enhanced PLL Specifications for -5 Speed Grades (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	3 *(1)*, *(2)*		684	MHz
f_{INPFD}	Input frequency to PFD	3		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			±200 *(3)*	ps
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(3)*	ps
t_{FCOMP}	External feedback clock compensation time *(4)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		500	MHz
f_{OUT_EXT}	Output frequency for external clock *(3)*	0.3		526	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(6)*			±100 ps for >200-MHz `outclk` ±20 mUI for <200-MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(5)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(7)*			100	µs
t_{LOCK}	Time required to lock from end of device configuration	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		800 *(8)*	MHz
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps