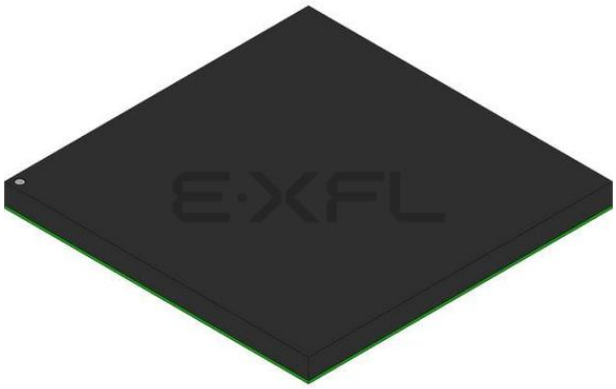

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	683
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	956-BBGA
Supplier Device Package	956-BGA (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1s40b956c7

Chapter	Date/Version	Changes Made
2	July 2005 v3.2	• Added "Clear Signals" section. • Updated "Power Sequencing & Hot Socketing" section. • Format changes.
	September 2004, v3.1	• Updated fast regional clock networks description on page 2–73. • Deleted the word preliminary from the "specification for the maximum time to relock is 100 µs" on page 2–90. • Added information about differential SSTL and HSTL outputs in "External Clock Outputs" on page 2–92. • Updated notes in Figure 2–55 on page 2–93. • Added information about *m* counter to "Clock Multiplication & Division" on page 2–101. • Updated Note 1 in Table 2–58 on page 2–101. • Updated description of "Clock Multiplication & Division" on page 2–88. • Updated Table 2–22 on page 2–102. • Added references to AN 349 and AN 329 to "External RAM Interfacing" on page 2–115. • Table 2–25 on page 2–116: updated the table, updated Notes 3 and 4. Notes 4, 5, and 6, are now Notes 5, 6, and 7, respectively. • Updated Table 2–26 on page 2–117. • Added information about PCI Compliance to page 2–120. • Table 2–32 on page 2–126: updated the table and deleted Note 1. • Updated reference to device pin-outs now being available on the web on page 2–130. • Added Notes 4 and 5 to Table 2–36 on page 2–130. • Updated Note 3 in Table 2–37 on page 2–131. • Updated Note 5 in Table 2–41 on page 2–135.
	April 2004, v3.0	• Added note 3 to rows 11 and 12 in Table 2–18. • Deleted "Stratix and Stratix GX Device PLL Availability" table. • Added I/O standards row in Table 2–28 that support max and min strength. • Row `clk [1,3,8,10]` was removed from Table 2–30. • Added checkmarks in Enhanced column for LVPECL, 3.3-V PCML, LVDS, and HyperTransport technology rows in Table 2–32. • Removed the Left and Right I/O Banks row in Table 2–34. • Changed `RCLK` values in Figures 2–50 and 2–51. • External RAM Interfacing section replaced.
	November 2003, v2.2	• Added 672-pin BGA package information in Table 2–37. • Removed support for series and parallel on-chip termination. • Termination Technology renamed differential on-chip termination. • Updated the number of channels per PLL in Tables 2-38 through 2-42. • Updated Figures 2–65 and 2–67.
	October 2003, v2.1	• Updated DDR I information. • Updated Table 2–22. • Added Tables 2–25, 2–29, 2–30, and 2–72. • Updated Figures 2–59, 2–65, and 2–67. • Updated the Lock Detect section.

Chapter	Date/Version	Changes Made
4	October 2003, v2.1	• Added -8 speed grade information. • Updated performance information in Table 4–36. • Updated timing information in Tables 4–55 through 4–96. • Updated delay information in Tables 4–103 through 4–108. • Updated programmable delay information in Tables 4–100 and 4–103.
	July 2003, v2.0	• Updated clock rates in Tables 4–114 through 4–123. • Updated speed grade information in the introduction on page 4-1. • Corrected figures 4-1 & 4-2 and Table 4-9 to reflect how VID and VOD are specified. • Added note 6 to Table 4-32. • Updated Stratix Performance Table 4-35. • Updated EP1S60 and EP1S80 timing parameters in Tables 4-82 to 4-93. The Stratix timing models are final for all devices. • Updated Stratix IOE programmable delay chains in Tables 4-100 to 4-101. • Added single-ended I/O standard output pin delay adders for loading in Table 4-102. • Added spec for FPLL[10..7]CLK pins in Tables 4-104 and 4-107. • Updated high-speed I/O specification for J=2 in Tables 4-114 and 4-115. • Updated EPLL specification and fast PLL specification in Tables 4-116 to 4-120.
5	September 2004, v2.1	• Updated reference to device pin-outs on page 5–1 to indicate that device pin-outs are no longer included in this manual and are now available on the Altera web site.
	April 2003, v1.0	• No new changes in Stratix Device Handbook v2.0.

1. Introduction

S51001-3.2

Introduction

The Stratix® family of FPGAs is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities of up to 79,040 logic elements (LEs) and up to 7.5 Mbits of RAM. Stratix devices offer up to 22 digital signal processing (DSP) blocks with up to 176 (9-bit × 9-bit) embedded multipliers, optimized for DSP applications that enable efficient implementation of high-performance filters and multipliers. Stratix devices support various I/O standards and also offer a complete clock management solution with its hierarchical clock structure with up to 420-MHz performance and up to 12 phase-locked loops (PLLs).

The following shows the main sections in the Stratix Device Family Data Sheet:

The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix devices.

Table 2–1. Stratix Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP1S10	4 / 94	2 / 60	1	2 / 6	40	30
EP1S20	6 / 194	2 / 82	2	2 / 10	52	41
EP1S25	6 / 224	3 / 138	2	2 / 10	62	46
EP1S30	7 / 295	3 / 171	4	2 / 12	67	57
EP1S40	8 / 384	3 / 183	4	2 / 14	77	61
EP1S60	10 / 574	4 / 292	6	2 / 18	90	73
EP1S80	11 / 767	4 / 364	9	2 / 22	101	91

Logic Array Blocks

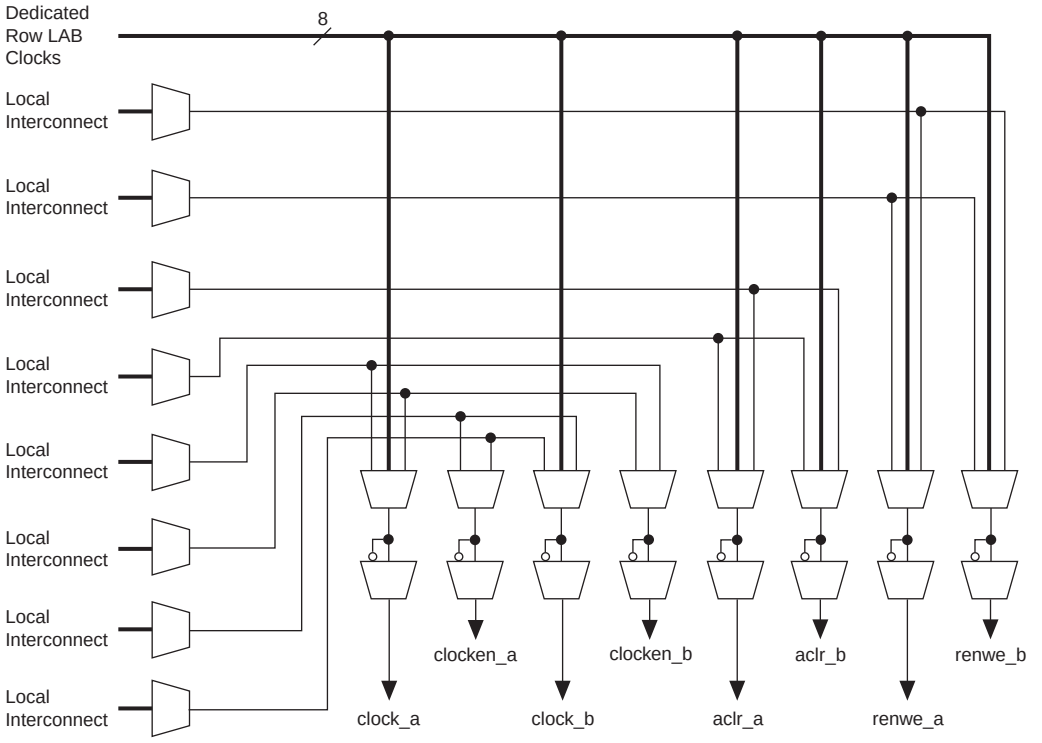
Each LAB consists of 10 LEs, LE carry chains, LAB control signals, local interconnect, LUT chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix LAB.

Figure 2–8 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix™ memory and DSP blocks. A carry chain can continue as far as a full column.

Figure 2–19. M-RAM Block Control Signals



One of the M-RAM block's horizontal sides drive the address and control signal (clock, renwe, byteena, etc.) inputs. Typically, the horizontal side closest to the device perimeter contains the interfaces. The one exception is when two M-RAM blocks are paired next to each other. In this case, the side of the M-RAM block opposite the common side of the two blocks contains the input interface. The top and bottom sides of any M-RAM block contain data input and output interfaces to the logic array. The top side has 72 data inputs and 72 data outputs for port B, and the bottom side has another 72 data inputs and 72 data outputs for port A. Figure 2–20 shows an example floorplan for the EP1S60 device and the location of the M-RAM interfaces.

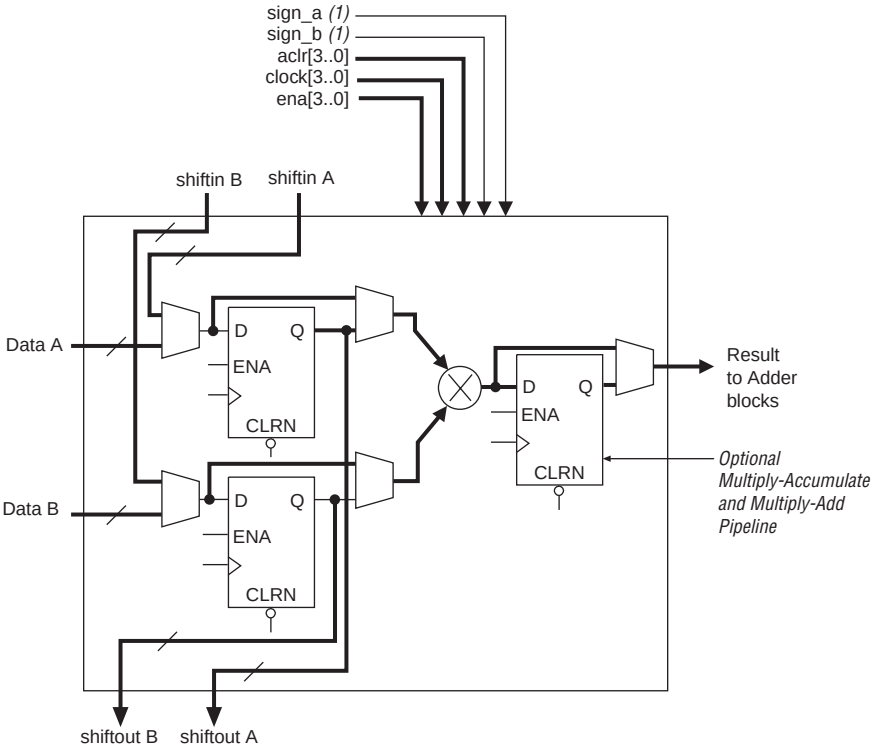
The DSP block consists of the following elements:

- Multiplier block
- Adder/output block

Multiplier Block

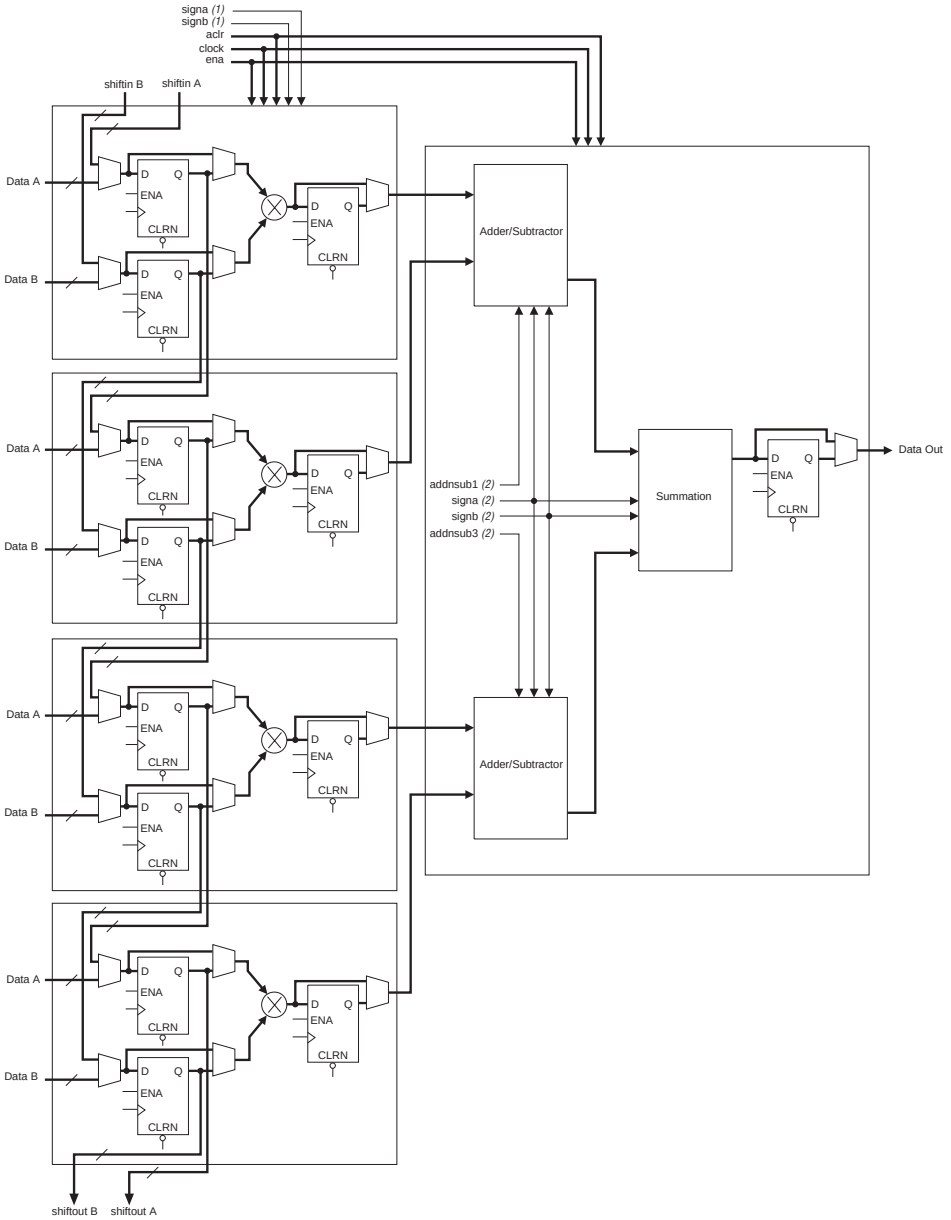
The DSP block multiplier block consists of the input registers, a multiplier, and pipeline register for pipelining multiply-accumulate and multiply-add/subtract functions as shown in Figure 2–32.

Figure 2–32. Multiplier Sub-Block within Stratix DSP Block



Note to Figure 2–32:
(1) These signals can be unregistered or registered once to match data path pipelines if required.

Figure 2–39. Four-Multipliers Adder Mode

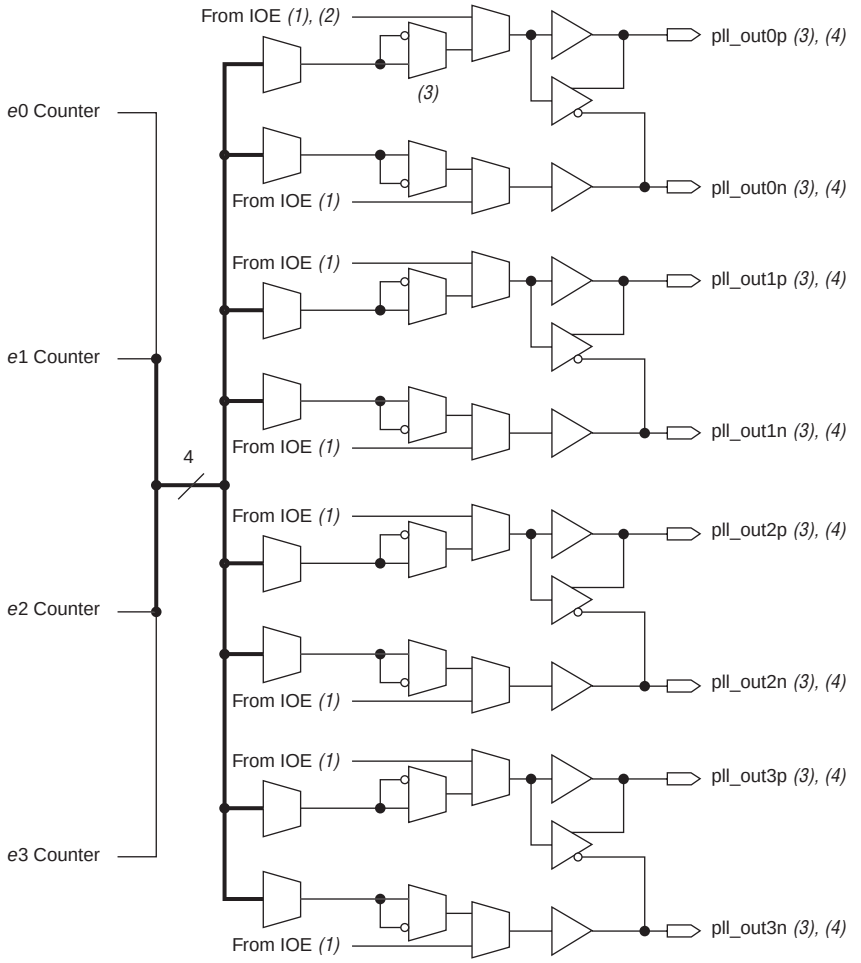


Notes to Figure 2–39:

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

Figure 2–55. External Clock Outputs for PLLs 5 & 6



Notes to Figure 2–55:

(1) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with IOE outputs.

(2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180° .

(3) EP1S10, EP1S20, and EP1S25 devices in 672-pin BGA and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., `pll_out0p`, `pll_out0n`, `pll_out1p`, and `pll_out1n`).

(4) Differential SSTL and HSTL outputs are implemented using two single-ended output buffers, which are programmed to have opposite polarity.

Clock Feedback

The following four feedback modes in Stratix device enhanced PLLs allow multiplication and/or phase and delay shifting:

- Zero delay buffer: The external clock output pin is phase-aligned with the clock input pin for zero delay. Altera recommends using the same I/O standard on the input clock and the output clocks for optimum performance.
- External feedback: The external feedback input pin, FBIN, is phase-aligned with the clock input, CLK, pin. Aligning these clocks allows you to remove clock delay and skew between devices. This mode is only possible for PLLs 5 and 6. PLLs 5 and 6 each support feedback for one of the dedicated external outputs, either one single-ended or one differential pair. In this mode, one *e* counter feeds back to the PLL FBIN input, becoming part of the feedback loop. Altera recommends using the same I/O standard on the input clock, the FBIN pin, and the output clocks for optimum performance.
- Normal mode: If an internal clock is used in this mode, it is phase-aligned to the input clock pin. The external clock output pin will have a phase delay relative to the clock input pin if connected in this mode. You define which internal clock output from the PLL should be phase-aligned to the internal clock pin.
- No compensation: In this mode, the PLL will not compensate for any clock networks or external clock outputs.

Phase & Delay Shifting

Stratix device enhanced PLLs provide advanced programmable phase and clock delay shifting. These parameters are set in the Quartus II software.

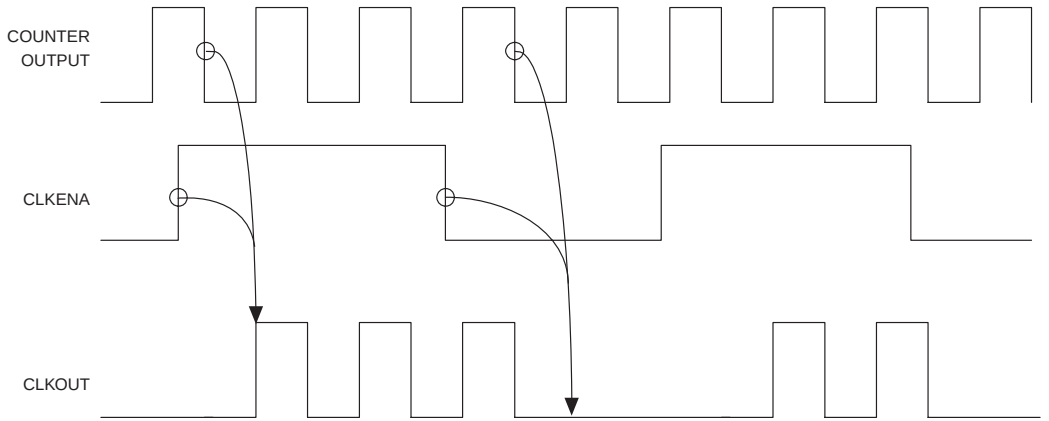
Phase Delay

The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entry. You enter a desired phase shift and the Quartus II software automatically sets the closest setting achievable. This type of phase shift is not reconfigurable during system operation. For phase shifting, enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can select phase-shifting values in time units with a resolution of 156.25 to 416.66 ps. This resolution is a function of frequency input and the multiplication and division factors (that is, it is a function of the VCO period), with the finest step being equal to an eighth (×0.125) of the VCO period. Each clock output counter can choose a different phase of the

resynchronization or relock period. The clkena signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The extclkena signals work in the same way as the clkena signals, but they control the external clock output counters (*e*0, *e*1, *e*2, and *e*3). Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the FBIN pin.

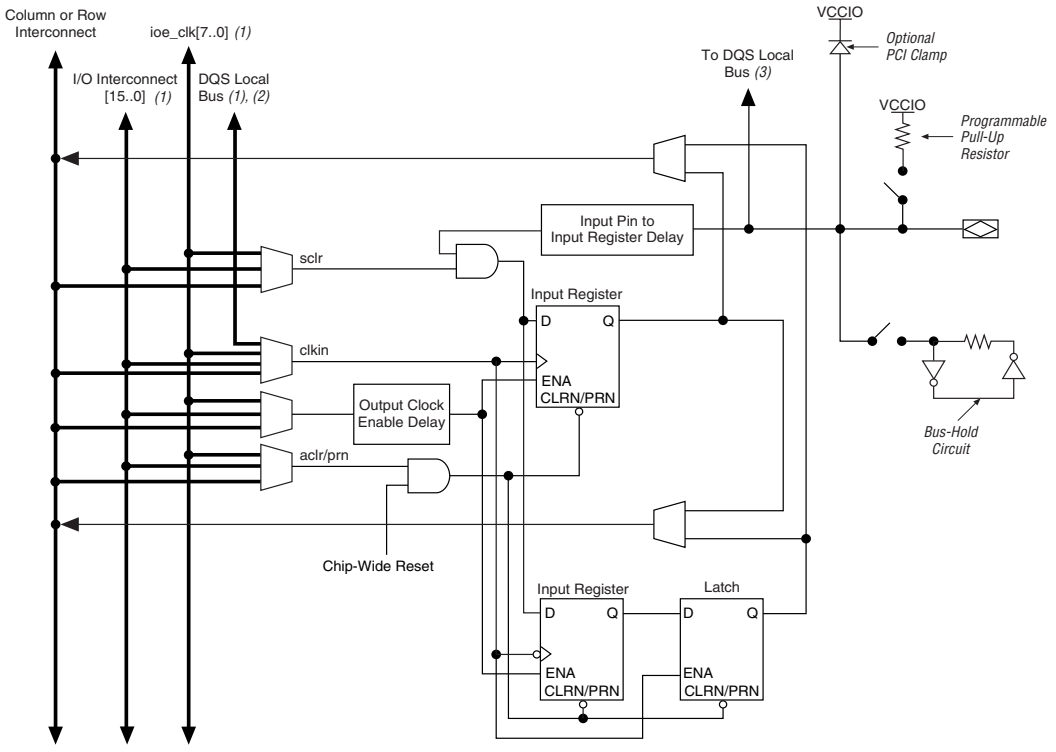
Figure 2–57. extclkena Signals



Fast PLLs

Stratix devices contain up to eight fast PLLs with high-speed serial interfacing ability, along with general-purpose features. Figure 2–58 shows a diagram of the fast PLL.

Figure 2–65. Stratix IOE in DDR Input I/O Configuration Note (1)



Notes to Figure 2–65:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.

Table 2–40. EP1S60 Differential Channels (Part 2 of 2) Note (1)

Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
1,020-pin FineLine BGA	Transmitter (4)	80 (12) (7)	840	12 (2)	10 (4)	10 (4)	12 (2)	20	20	20	20
			840 (5), (8)	22 (6)	22 (6)	22 (6)	22 (6)	20	20	20	20
	Receiver	80 (10) (7)	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5), (8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)
1,508-pin FineLine BGA	Transmitter (4)	80 (36) (7)	840	12 (8)	10 (10)	10 (10)	12 (8)	20	20	20	20
			840 (5),(8)	22 (18)	22 (18)	22 (18)	22 (18)	20	20	20	20
	Receiver	80 (36) (7)	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5),(8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)

Table 2–41. EP1S80 Differential Channels (Part 1 of 2) Note (1)

Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
956-pin BGA	Transmitter (4)	80 (40) (7)	840	10	10	10	10	20	20	20	20
			840 (5),(8)	20	20	20	20	20	20	20	20
	Receiver	80	840	20	20	20	20	10	10	10	10
			840 (5),(8)	40	40	40	40	10	10	10	10
1,020-pin FineLine BGA	Transmitter (4)	92 (12) (7)	840	10 (2)	10 (4)	10 (4)	10 (2)	20	20	20	20
			840 (5),(8)	20 (6)	20 (6)	20 (6)	20 (6)	20	20	20	20
	Receiver	90 (10) (7)	840	20	20	20	20	10 (2)	10 (3)	10 (3)	10 (2)
			840 (5),(8)	40	40	40	40	10 (2)	10 (3)	10 (3)	10 (2)

The Stratix device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix devices.

Table 3–2. Stratix Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1S10	1,317
EP1S20	1,797
EP1S25	2,157
EP1S30	2,253
EP1S40	2,529
EP1S60	3,129
EP1S80	3,777

Table 3–3. 32-Bit Stratix Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP1S10	0000	0010 0000 0000 0001	000 0110 1110	1
EP1S20	0000	0010 0000 0000 0010	000 0110 1110	1
EP1S25	0000	0010 0000 0000 0011	000 0110 1110	1
EP1S30	0000	0010 0000 0000 0100	000 0110 1110	1
EP1S40	0000	0010 0000 0000 0101	000 0110 1110	1
EP1S60	0000	0010 0000 0000 0110	000 0110 1110	1
EP1S80	0000	0010 0000 0000 0111	000 0110 1110	1

Notes to Tables 3–2 and 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Table 4–2. Stratix Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C

Table 4–3. Stratix Device DC Operating Conditions Note (7) (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All memory blocks in power-down mode)	V_I = ground, no load, no toggling inputs				mA
		EP1S10. V_I = ground, no load, no toggling inputs		37		mA
		EP1S20. V_I = ground, no load, no toggling inputs		65		mA
		EP1S25. V_I = ground, no load, no toggling inputs		90		mA
		EP1S30. V_I = ground, no load, no toggling inputs		114		mA
		EP1S40. V_I = ground, no load, no toggling inputs		145		mA
		EP1S60. V_I = ground, no load, no toggling inputs		200		mA
		EP1S80. V_I = ground, no load, no toggling inputs		277		mA

Table 4–110. Stratix IOE Programmable Delays on Row Pins Note (1)

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off		3,970		4,367		5,022		5,908	ps
	Small		3,390		3,729		4,288		5,045	ps
	Medium		2,810		3,091		3,554		4,181	ps
	Large		173		181		208		245	ps
	On		173		181		208		245	ps
Decrease input delay to input register	Off		3,900		4,290		4,933		5,804	ps
	On		0		0		0		0	ps
Decrease input delay to output register	Off		1,240		1,364		1,568		1,845	ps
	On		0		0		0		0	ps
Increase delay to output pin	Off		0		0		0		0	ps
	On		397		417		417		417	ps
Increase delay to output enable pin	Off		0		0		0		0	ps
	On		348		383		441		518	ps
Increase output clock enable delay	Off		0		0		0		0	ps
	Small		180		198		227		267	ps
	Large		260		286		328		386	ps
	On		260		286		328		386	ps
Increase input clock enable delay	Off		0		0		0		0	ps
	Small		180		198		227		267	ps
	Large		260		286		328		386	ps
	On		260		286		328		386	ps
Increase output enable clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase t_{ZX} delay to output pin	Off		0		0		0		0	ps
	On		1,993		2,092		2,092		2,092	ps

Note to Table 4–109 and Table 4–110:

(1) The delay chain delays vary for different device densities. These timing values only apply to EP1S30 and EP1S40 devices. Reference the timing information reported by the Quartus II software for other devices.

Maximum Input & Output Clock Rates

Tables 4–114 through 4–119 show the maximum input clock rate for column and row pins in Stratix devices.

Table 4–114. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Flip-Chip Packages (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	422	390	390	MHz
2.5 V	422	422	390	390	MHz
1.8 V	422	422	390	390	MHz
1.5 V	422	422	390	390	MHz
LVCMOS	422	422	390	390	MHz
GTL	300	250	200	200	MHz
GTL+	300	250	200	200	MHz
SSTL-3 Class I	400	350	300	300	MHz
SSTL-3 Class II	400	350	300	300	MHz
SSTL-2 Class I	400	350	300	300	MHz
SSTL-2 Class II	400	350	300	300	MHz
SSTL-18 Class I	400	350	300	300	MHz
SSTL-18 Class II	400	350	300	300	MHz
1.5-V HSTL Class I	400	350	300	300	MHz
1.5-V HSTL Class II	400	350	300	300	MHz
1.8-V HSTL Class I	400	350	300	300	MHz
1.8-V HSTL Class II	400	350	300	300	MHz
3.3-V PCI	422	422	390	390	MHz
3.3-V PCI-X 1.0	422	422	390	390	MHz
Compact PCI	422	422	390	390	MHz
AGP 1×	422	422	390	390	MHz
AGP 2×	422	422	390	390	MHz
CTT	300	250	200	200	MHz
Differential 1.5-V HSTL C1	400	350	300	300	MHz
LVPECL *(1)*	645	645	622	622	MHz
PCML *(1)*	300	275	275	275	MHz

Table 4–126. High-Speed I/O Specifications for Wire-Bond Packages (Part 2 of 2)

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SW	PCML (J = 4, 7, 8, 10) only	800			800			800			ps
	PCML (J = 2) only	1,200			1,200			1,200			ps
	PCML (J = 1) only	1,700			1,700			1,700			ps
	LVDS and LVPECL (J = 1) only	550			550			550			ps
	LVDS, LVPECL, HyperTransport technology (J = 2 through 10) only	500			500			500			ps
Input jitter tolerance (peak-to-peak)	All			250			250			250	ps
Output jitter (peak-to-peak)	All			200			200			200	ps
Output t_{RISE}	LVDS	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	120	170	200	120	170	200	120	170	200	ps
	LVPECL	100	135	150	100	135	150	100	135	150	ps
	PCML	80	110	135	80	110	135	80	110	135	ps
Output t_{FALL}	LVDS	80	110	120	80	110	120	80	110	120	ps
	HyperTransport	110	170	200	110	170	200	110	170	200	ps
	LVPECL	100	135	160	100	135	160	100	135	160	ps
	PCML	110	145	175	110	145	175	110	145	175	ps
t_{DUTY}	LVDS (J = 2 through10) only	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (J =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100	µs

Table 4–133. Fast PLL Specifications for -8 Speed Grades (Part 2 of 2)				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
t_{ARESET}	Minimum pulse width on `areset` signal	10		ns

Notes to Tables 4–131 through 4–133:

(1) See "Maximum Input & Output Clock Rates" on page 4–76.
(2) PLLs 7, 8, 9, and 10 in the EP1S80 device support up to 717-MHz input and output.
(3) Use this equation ($f_{OUT} = f_{IN} * ml(n \times$ post-scale counter)) in conjunction with the specified f_{INPFD} and f_{VCO} ranges to determine the allowed PLL settings.
(4) When using the SERDES, high-speed differential I/O mode supports a maximum output frequency of 210 MHz to the global or regional clocks (that is, the maximum data rate 840 Mbps divided by the smallest SERDES J factor of 4).
(5) Refer to the section "High-Speed I/O Specification" on page 4–87 for more information.
(6) This parameter is for high-speed differential I/O mode only.
(7) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16.
(8) High-speed differential I/O mode supports W = 1 to 16 and J = 4, 7, 8, or 10.

DLL Specifications

Table 4–134 reports the jitter for the DLL in the DQS phase shift reference circuit.

Table 4–134. DLL Jitter for DQS Phase Shift Reference Circuit	
Frequency (MHz)	**DLL Jitter (ps)**
197 to 200	± 100
160 to 196	± 300
100 to 159	± 500

For more information on DLL jitter, see the *DDR SRAM* section in the *Stratix Architecture* chapter of the *Stratix Device Handbook, Volume 1*.

Table 4–135 lists the Stratix DLL low frequency limit for full phase shift across all PVT conditions. The Stratix DLL can be used below these frequencies, but it will not achieve the full phase shift requested across all

Figure 5–1. Stratix Device Packaging Ordering Information