Intel - EP1S40F1508C6NGA Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	822
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s40f1508c6nga

About This Handbook

This handbook provides comprehensive information about the Altera® Stratix family of devices.

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- The Adobe Acrobat Find feature, which searches the text of a PDF document. Click the binoculars toolbar icon to open the Find dialog box.
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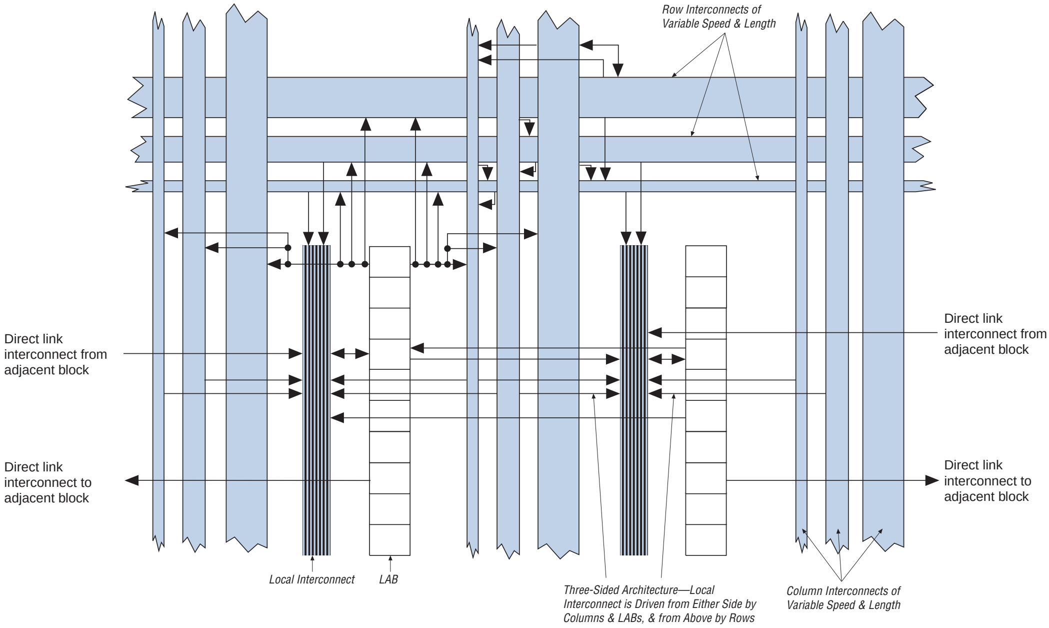
FTP site	ftp.altera.com	ftp.altera.com

Chapter	Date/Version	Changes Made
2	July 2003, v2.0	● Added reference on page 2-73 to Figures 2-50 and 2-51 for `RCLK` connections. ● Updated ranges for EPLL post-scale and pre-scale dividers on page 2-85. ● Updated PLL Reconfiguration frequency from 25 to 22 MHz on page 2-87. ● New requirement to assert are set signal each PLL when it has to re-acquire lock on either a new clock after loss of lock (page 2-96). ● Updated max input frequency for `CLK[1,3,8,10]` from 462 to 500, Table 2-24. ● Renamed impedance matching to series termination throughout. ● Updated naming convention for DQS pins on page 2-112 to match pin tables. ● Added DDR SDRAM Performance Specification on page 2-117. ● Added external reference resistor values for terminator technology (page 2-136). ● Added Terminator Technology Specification on pages 2-137 and 2-138. ● Updated Tables 2-45 to 2-49 to reflect PLL cross-bank support for high speed differential channels at full speed. ● Wire bond package performance specification for "high" speed channels was increased to 624 Mbps from 462 Mbps throughout chapter.
3	July 2005, v1.3	● Updated "Operating Modes" section. ● Updated "Temperature Sensing Diode" section. ● Updated "IEEE Std. 1149.1 (JTAG) Boundary-Scan Support" section. ● Updated "Configuration" section.
	January 2005, v1.2	● Updated limits for JTAG chain of devices.
	September 2004, v1.1	● Added new section, "Stratix Automated Single Event Upset (SEU) Detection" on page 3–12. ● Updated description of "Custom-Built Circuitry" on page 3–13.
	April 2003, v1.0	● No new changes in *Stratix Device Handbook* v2.0.
4	January 2006, v3.4	● Added Table 4–135.
	July 2005, v3.3	● Updated Tables 4–6 and 4–30. ● Updated Tables 4–103 through 4–108. ● Updated Tables 4–114 through 4–124. ● Updated Table 4–129. ● Added Table 4–130.

Chapter	Date/Version	Changes Made
4		• Table 4–48 on page 4–30: added rows $t_{M512CLKSENSU}$ and $t_{M512CLKENH}$, and updated symbol names. • Updated power-up current (ICCINT) required to power a Stratix device on page 4–17. • Updated Table 4–37 on page 4–22 through Table 4–43 on page 4–27. • Table 4–49 on page 4–31: added rows $t_{M4KCLKENSU}$, $t_{M4KCLKENH}$, $t_{M4KBESU}$, and t_{M4KBEH}, deleted rows $t_{M4KRADDRASU}$ and $t_{M4KRADDRH}$, and updated symbol names. • Table 4–50 on page 4–31: added rows $t_{MRAMCLKENSU}$, $t_{MRAMCLKENH}$, $t_{MRAMBESU}$, and $t_{MRAMBEH}$, deleted rows $t_{MRAMADDRASU}$ and $t_{MRAMRADDRH}$, and updated symbol names. • Table 4–52 on page 4–34: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. • Table 4–52 on page 4–34: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. • Table 4–53 on page 4–34: updated table and added rows t_{XZPLL} and t_{ZXPLL}. • Updated Note 2 in Table 4–53 on page 4–34. • Table 4–54 on page 4–35: updated table, deleted “Conditions” column, and added rows t_{XZPLL} and t_{ZXPLL}. • Updated Note 2 in Table 4–54 on page 4–35. • Deleted Note 2 from Table 4–55 on page 4–36 through Table 4–66 on page 4–41. • Updated Table 4–55 on page 4–36 through Table 4–96 on page 4–56. Added rows T_{XZ}, T_{ZX}, T_{XZPLL}, and T_{ZXPLL}. • Added Note 4 to Table 4–101 on page 4–62. • Deleted Note 1 from Table 4–67 on page 4–42 through Table 4–84 on page 4–50. • Added new section “I/O Timing Measurement Methodology” on page 4–60. • Deleted Note 1 from Table 4–67 on page 4–42 through Table 4–84 on page 4–50. • Deleted Note 2 from Table 4–85 on page 4–51 through Table 4–96 on page 4–56. • Added Note 4 to Table 4–101 on page 4–62. • Table 4–102 on page 4–64: updated table and added Note 4. • Updated description of “External I/O Delay Parameters” on page 4–66. • Added Note 1 to Table 4–109 on page 4–73 and Table 4–110 on page 4–74. • Updated Table 4–103 on page 4–66 through Table 4–110 on page 4–74. • Deleted Note 2 from Table 4–103 on page 4–66 through Table 4–106 on page 4–69. • Added new paragraph about output adder delays on page 4–68. • Updated Table 4–110 on page 4–74. • Added Note 1 to Table 4–111 through Table 4–113 on page 4–75.

Figure 2–2. Stratix LAB Structure



LAB Interconnects

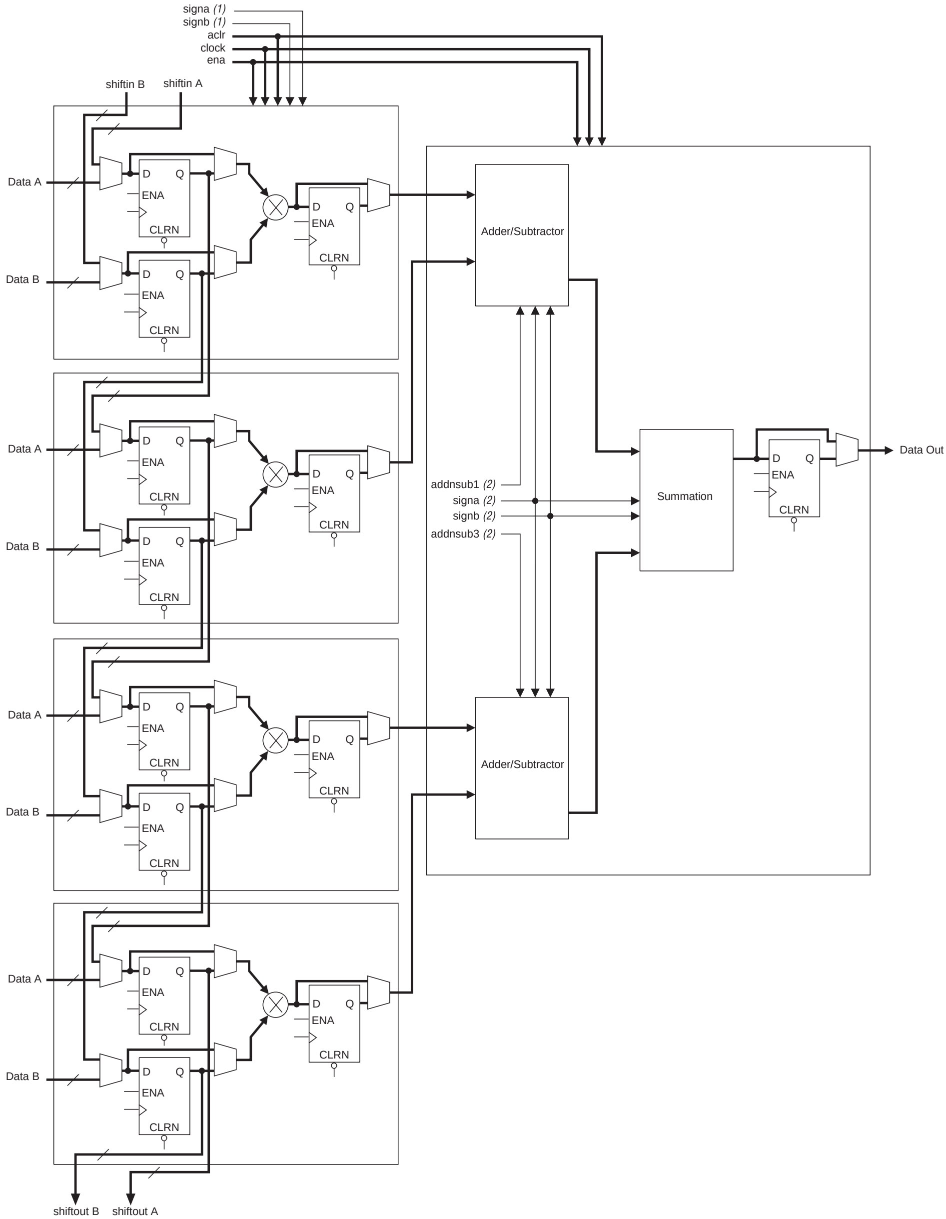
The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

C8 interconnects span eight LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C8 interconnects to drive either up or down. C8 interconnect connections between the LABs in a column are similar to the C4 connections shown in Figure 2–11 with the exception that they connect to eight LABs above and below. The C8 interconnects can drive and be driven by all types of architecture blocks similar to C4 interconnects. C8 interconnects can drive each other to extend their range as well as R8 interconnects for column-to-column connections. C8 interconnects are faster than two C4 interconnects.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[7..0]`.

Figure 2–39. Four-Multipliers Adder Mode

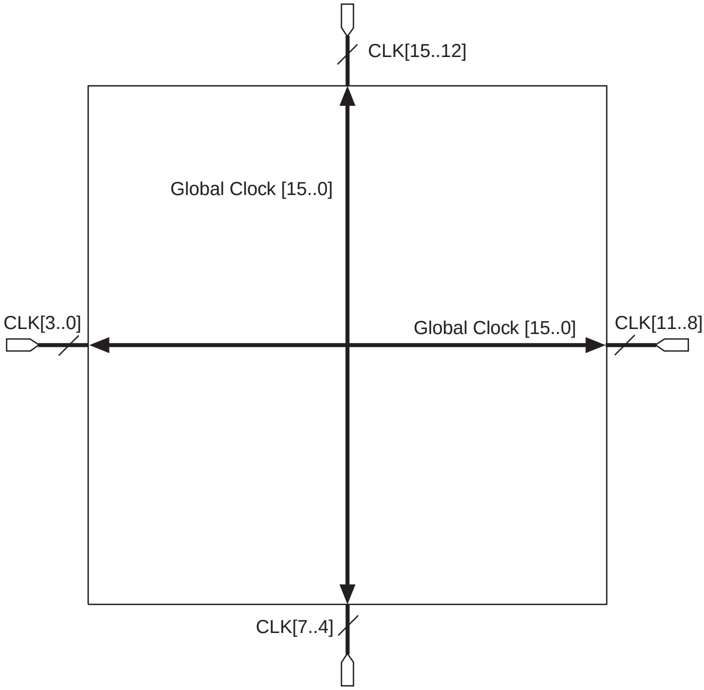


Notes to Figure 2–39:

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

Figure 2–42. Global Clocking *Note (1)*



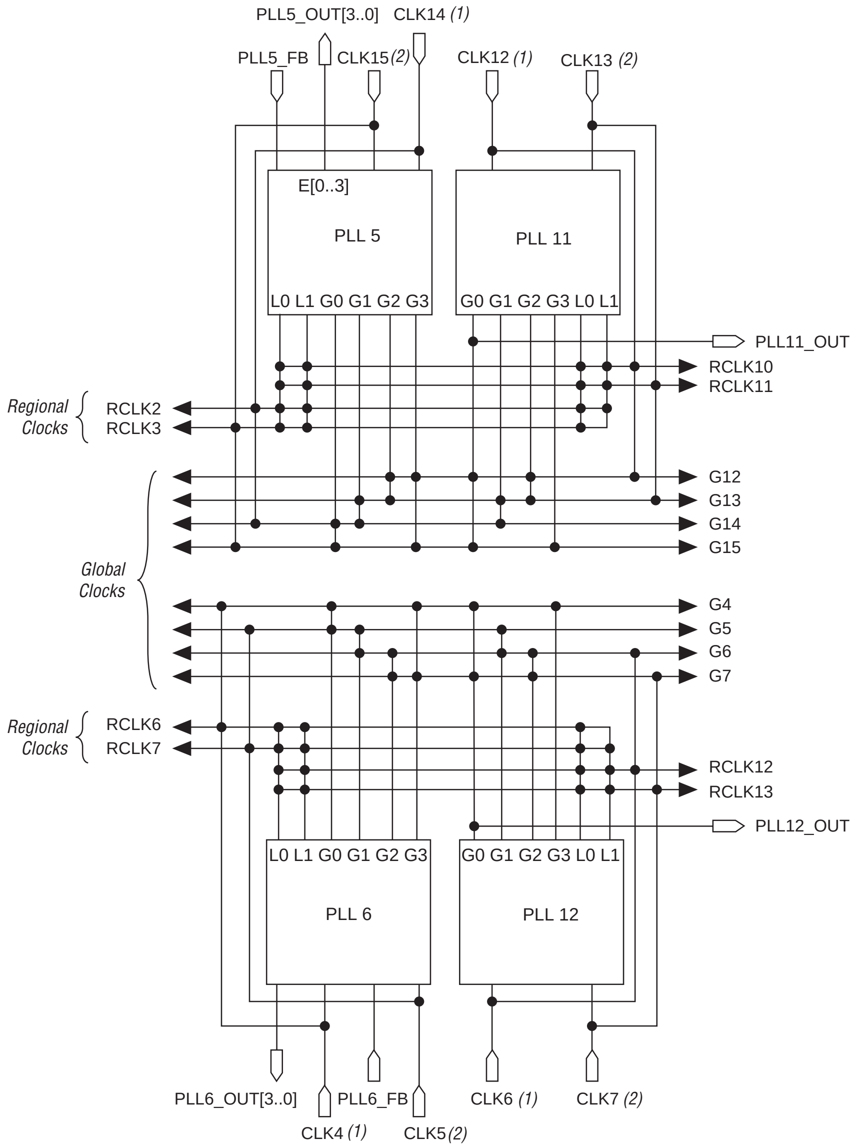
Note to Figure 2–42:

(1) The corner fast PLLs can also be driven through the global or regional clock networks. The global or regional clock input to the fast PLL can be driven by an output from another PLL, a pin-driven global or regional clock, or internally-generated global signals.

Regional Clock Network

There are four regional clock networks within each quadrant of the Stratix device that are driven by the same dedicated `CLK[15..0]` input pins or from PLL outputs. From a top view of the silicon, `RCLK[0..3]` are in the top left quadrant, `RCLK[8..11]` are in the top-right quadrant, `RCLK[4..7]` are in the bottom-left quadrant, and `RCLK[12..15]` are in the bottom-right quadrant. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. `RCLK` cannot be driven by internal logic. The `CLK` clock pins symmetrically drive the `RCLK` networks within a particular quadrant, as shown in Figure 2–43. See Figures 2–50 and 2–51 for `RCLK` connections from PLLs and `CLK` pins.

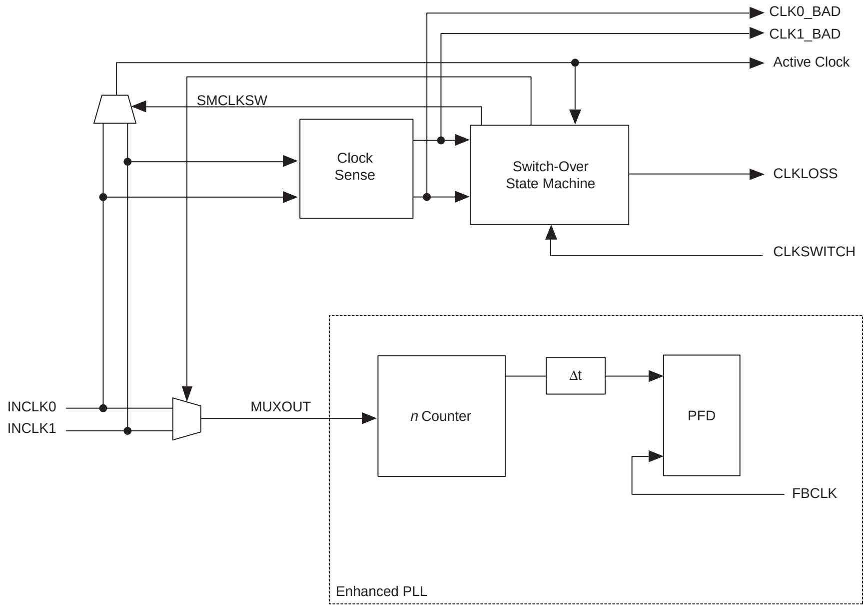
Figure 2–51. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs Note (1)



Notes to Figure 2–51:

(1) PLLs 1 to 4 and 7 to 10 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs.
(2) `CLK4`, `CLK6`, `CLK12`, and `CLK14` feed the corresponding PLL's `inclk0` port.
(3) `CLK5`, `CLK7`, `CLK13`, and `CLK15` feed the corresponding PLL's `inclk1` port.
(4) The EP1S40 device in the 780-pin FineLine BGA package does not support PLLs 11 and 12.

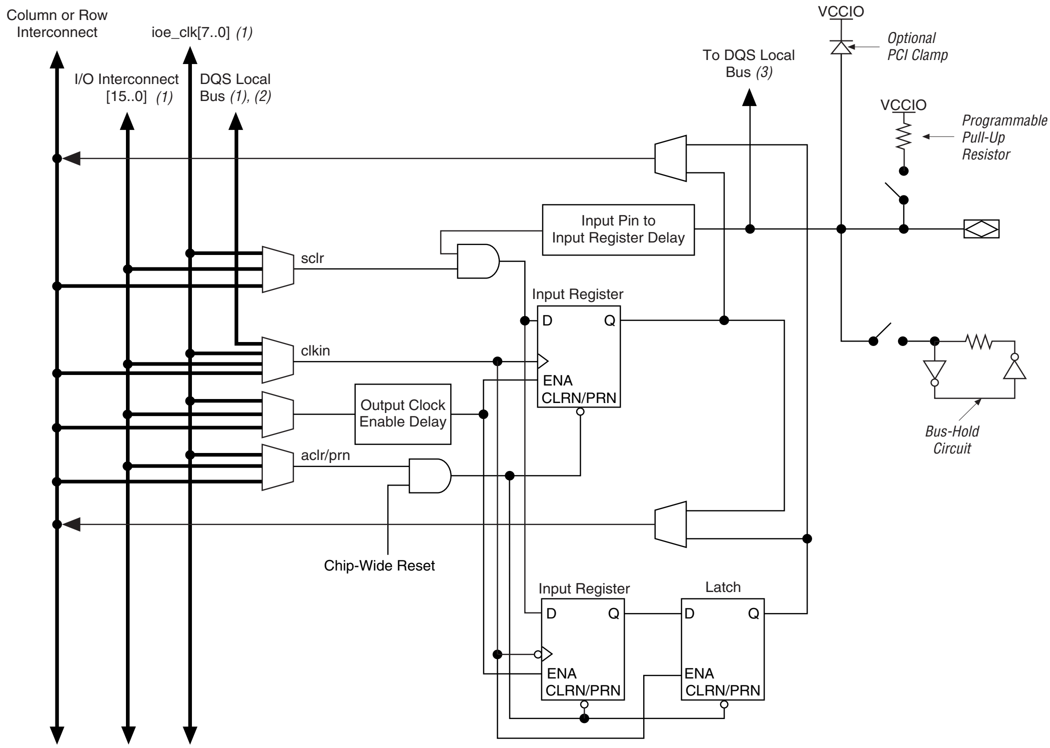
Figure 2–53. Clock Switchover Circuitry



There are two possible ways to use the clock switchover feature.

- Use automatic switchover circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 2–53. In this case, the secondary clock becomes the reference clock for the PLL.
- Use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. You can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

Figure 2–65. Stratix IOE in DDR Input I/O Configuration *Note (1)*



Notes to Figure 2–65:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.

For more information on I/O standards supported by Stratix devices, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook, Volume 2*.

Stratix devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in Figure 2–70. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in Table 2–31 except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. Table 2–32 shows I/O standard support for each I/O bank.

Table 2–32. I/O Support by Bank (Part 2 of 2)			
I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
SSTL-3 Class II	✓	✓	✓
AGP (1× and 2×)	✓		✓
CTT	✓	✓	✓

Each I/O bank has its own `VCCIO` pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different standard independently. Each bank also has dedicated `VREF` pins to support any one of the voltage-referenced standards (such as SSTL-3) independently.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

Differential On-Chip Termination

Stratix devices provide differential on-chip termination (LVDS I/O standard) to reduce reflections and maintain signal integrity. Differential on-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections. The internal termination is designed using transistors in the linear region of operation.

Stratix devices support internal differential termination with a nominal resistance value of 137.5 Ω for LVDS input receiver buffers. LVPECL signals require an external termination resistor. Figure 2–71 shows the device with differential termination.

The Stratix device instruction register length is 10 bits and the `USERCODE` register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix devices.

Table 3–2. Stratix Boundary-Scan Register Length	
Device	**Boundary-Scan Register Length**
EP1S10	1,317
EP1S20	1,797
EP1S25	2,157
EP1S30	2,253
EP1S40	2,529
EP1S60	3,129
EP1S80	3,777

Table 3–3. 32-Bit Stratix Device IDCODE

Device	**IDCODE (32 Bits)** *(1)*			
	Version (4 Bits)	**Part Number (16 Bits)**	**Manufacturer Identity (11 Bits)**	**LSB (1 Bit)** *(2)*
EP1S10	0000	0010 0000 0000 0001	000 0110 1110	1
EP1S20	0000	0010 0000 0000 0010	000 0110 1110	1
EP1S25	0000	0010 0000 0000 0011	000 0110 1110	1
EP1S30	0000	0010 0000 0000 0100	000 0110 1110	1
EP1S40	0000	0010 0000 0000 0101	000 0110 1110	1
EP1S60	0000	0010 0000 0000 0110	000 0110 1110	1
EP1S80	0000	0010 0000 0000 0111	000 0110 1110	1

Notes to Tables 3–2 and 3–3:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	2.25	V
V_{IL}	Low-level input voltage		–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 4–8. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Notes to Tables 4–1 through 4–8:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns, or overshoot to the voltage shown in Table 4–9, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.

(5) V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(7) Typical values are for T_A = 25°C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

(10) Drive strength is programmable according to the values shown in the *Stratix Architecture* chapter of the *Stratix Device Handbook, Volume 1*.

Table 4–9. Overshoot Input Voltage with Respect to Duty Cycle (Part 1 of 2)

Vin (V)	Maximum Duty Cycle (%)
4.0	100
4.1	90
4.2	50

Table 4–50. M-RAM Block Internal Timing Microparameters (Part 2 of 2)									
Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MRAMBESU}$	25		25		28		33		ps
$t_{MRAMBEH}$	18		20		23		27		ps
$t_{MRAMDATAASU}$	25		25		28		33		ps
$t_{MRAMDATAAH}$	18		20		23		27		ps
$t_{MRAMADDRASU}$	25		25		28		33		ps
$t_{MRAMADDRAH}$	18		20		23		27		ps
$t_{MRAMDATABSU}$	25		25		28		33		ps
$t_{MRAMDATABH}$	18		20		23		27		ps
$t_{MRAMADDRBSU}$	25		25		28		33		ps
$t_{MRAMADDRBH}$	18		20		23		27		ps
$t_{MRAMDATACO1}$		1,038		1,053		1,210		1,424	ps
$t_{MRAMDATACO2}$		4,362		4,939		5,678		6,681	ps
$t_{MRAMCLKHL}$	1,000		1,111		1,190		1,400		ps
$t_{MRAMCLR}$	135		150		172		202		ps

Table 4–51. Routing Delay Internal Timing Parameters									
Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{R4}		268		295		339		390	ps
t_{R8}		371		349		401		461	ps
t_{R24}		465		512		588		676	ps
t_{C4}		440		484		557		641	ps
t_{C8}		577		634		730		840	ps
t_{C16}		445		489		563		647	ps
t_{LOCAL}		313		345		396		455	ps

Routing delays vary depending on the load on that specific routing line. The Quartus II software reports the routing delay information when running the timing analysis for a design.

Table 4–93. EP1S80 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	0.884		0.976		1.118		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.267	6.274	3.267	6.721	3.267	7.415	NA	NA	ns
t_{XZ}	3.207	6.148	3.207	6.589	3.207	7.291	NA	NA	ns
t_{ZX}	3.207	6.148	3.207	6.589	3.207	7.291	NA	NA	ns
$t_{INSUPLL}$	0.506		0.656		0.838		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.635	2.805	1.635	2.809	1.635	2.828	NA	NA	ns
t_{XZPLL}	1.575	2.679	1.575	2.677	1.575	2.704	NA	NA	ns
t_{ZXPLL}	1.575	2.679	1.575	2.677	1.575	2.704	NA	NA	ns

Table 4–94. EP1S80 External I/O Timing on Row Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.792		2.993		3.386		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.619	5.235	2.619	5.609	2.619	6.086	NA	NA	ns
t_{XZ}	2.646	5.289	2.646	5.665	2.646	6.154	NA	NA	ns
t_{ZX}	2.646	5.289	2.646	5.665	2.646	6.154	NA	NA	ns

Definition of I/O Skew

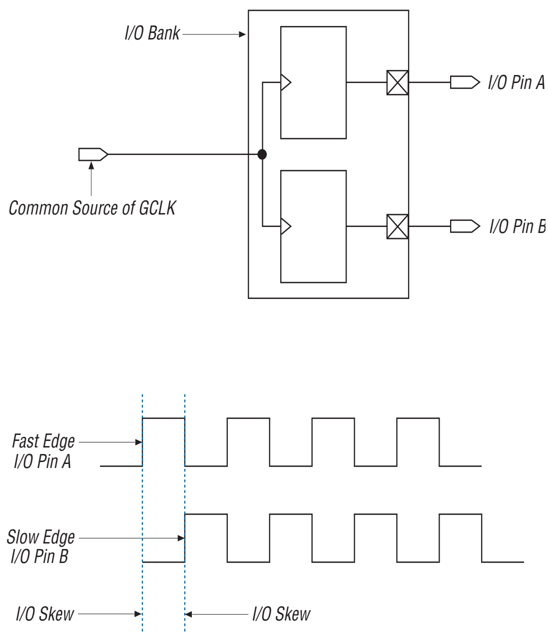
I/O skew is defined as the absolute value of the worst-case difference in clock-to-out times (t_{CO}) between any two output registers fed by a common clock source.

I/O bank skew is made up of the following components:

- Clock network skews: This is the difference between the arrival times of the clock at the clock input port of the two IOE registers.
- Package skews: This is the package trace length differences between (I/O pad A to I/O pin A) and (I/O pad B to I/O pin B).

Figure 4–5 shows an example of two IOE registers located in the same bank, being fed by a common clock source. The clock can come from an input pin or from a PLL output.

Figure 4–5. I/O Skew within an I/O Bank



External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density. All of the timing parameters in this section apply to both flip-chip and wire-bond packages.

Tables 4–103 and 4–104 show the input adder delays associated with column and row I/O pins. If an I/O standard is selected other than 3.3-V LVTTL or LVCMOS, add the selected delay to the external t_{INSU} and $t_{INSUPLL}$ I/O parameters shown in Tables 4–54 through 4–96.

Table 4–103. Stratix I/O Standard Column Pin Input Delay Adders

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0		0	ps
3.3-V LVTTL		0		0		0		0	ps
2.5-V LVTTL		19		19		22		26	ps
1.8-V LVTTL		221		232		266		313	ps
1.5-V LVTTL		352		369		425		500	ps
GTL		–45		–48		–55		–64	ps
GTL+		–75		–79		–91		–107	ps
3.3-V PCI		0		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0		0	ps
Compact PCI		0		0		0		0	ps
AGP 1×		0		0		0		0	ps
AGP 2×		0		0		0		0	ps
CTT		120		126		144		170	ps
SSTL-3 Class I		–162		–171		–196		–231	ps
SSTL-3 Class II		–162		–171		–196		–231	ps
SSTL-2 Class I		–202		–213		–244		–287	ps
SSTL-2 Class II		–202		–213		–244		–287	ps
SSTL-18 Class I		78		81		94		110	ps
SSTL-18 Class II		78		81		94		110	ps
1.5-V HSTL Class I		–76		–80		–92		–108	ps
1.5-V HSTL Class II		–76		–80		–92		–108	ps
1.8-V HSTL Class I		–52		–55		–63		–74	ps
1.8-V HSTL Class II		–52		–55		–63		–74	ps

Table 4–107. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2)

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	4 mA		1,822		1,913		1,913		1,913	ps
	8 mA		1,586		1,665		1,665		1,665	ps
	12 mA		686		720		720		720	ps
	16 mA		630		662		662		662	ps
	24 mA		0		0		0		0	ps
2.5-V LVTTL	2 mA		2,925		3,071		3,071		3,071	ps
	8 mA		1,496		1,571		1,571		1,571	ps
	12 mA		937		984		984		984	ps
	16 mA		1,003		1,053		1,053		1,053	ps
1.8-V LVTTL	2 mA		7,101		7,456		7,456		7,456	ps
	8 mA		3,620		3,801		3,801		3,801	ps
	12 mA		3,109		3,265		3,265		3,265	ps
1.5-V LVTTL	2 mA		10,941		11,488		11,488		11,488	ps
	4 mA		7,431		7,803		7,803		7,803	ps
	8 mA		5,990		6,290		6,290		6,290	ps
GTL			–959		–1,007		–1,007		–1,007	ps
GTL+			–438		–460		–460		–460	ps
3.3-V PCI			660		693		693		693	ps
3.3-V PCI-X 1.0			660		693		693		693	ps
Compact PCI			660		693		693		693	ps
AGP 1×			660		693		693		693	ps
AGP 2×			288		303		303		303	ps
CTT			631		663		663		663	ps
SSTL-3 Class I			301		316		316		316	ps
SSTL-3 Class II			–359		–377		–377		–377	ps
SSTL-2 Class I			523		549		549		549	ps
SSTL-2 Class II			–49		–51		–51		–51	ps
SSTL-18 Class I			2,315		2,431		2,431		2,431	ps
SSTL-18 Class II			723		759		759		759	ps
1.5-V HSTL Class I			1,687		1,771		1,771		1,771	ps
1.5-V HSTL Class II			1,095		1,150		1,150		1,150	ps
1.8-V HSTL Class I			599		629		678		744	ps
1.8-V HSTL Class II			87		102		102		102	ps

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 3 of 4) Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SW	PCML ($J = 4, 7, 8, 10$)	750			750			800			800			ps
	PCML ($J = 2$)	900			900			1,200			1,200			ps
	PCML ($J = 1$)	1,500			1,500			1,700			1,700			ps
	LVDS and LVPECL ($J = 1$)	500			500			550			550			ps
	LVDS, LVPECL, HyperTransport technology ($J = 2$ through 10)	440			440			500			500			ps
Input jitter tolerance (peak-to-peak)	All			250			250			250			250	ps
Output jitter (peak-to-peak)	All			160			160			200			200	ps
Output t_{RISE}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	120	170	200	120	170	200	ps
	LVPECL	90	130	150	90	130	150	100	135	150	100	135	150	ps
	PCML	80	110	135	80	110	135	80	110	135	80	110	135	ps
Output t_{FALL}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	110	170	200	110	170	200	ps
	LVPECL	90	130	160	90	130	160	100	135	160	100	135	160	ps
	PCML	105	140	175	105	140	175	110	145	175	110	145	175	ps