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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4125
Number of Logic Elements/Cells	41250
Total RAM Bits	3423744
Number of I/O	615
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s40f780c5



Chapter Revision Dates

The chapters in this book, *Stratix Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

- Chapter 1. Introduction
Revised: *July 2005*
Part number: *S51001-3.2*
- Chapter 2. Stratix Architecture
Revised: *July 2005*
Part number: *S51002-3.2*
- Chapter 3. Configuration & Testing
Revised: *July 2005*
Part number: *S51003-1.3*
- Chapter 4. DC & Switching Characteristics
Revised: *January 2006*
Part number: *S51004-3.4*
- Chapter 5. Reference & Ordering Information
Revised: *September 2004*
Part number: *S51005-2.1*

Chapter	Date/Version	Changes Made
4	January 2005, 3.2	<ul style="list-style-type: none"> Updated rise and fall input values.
	September 2004, v3.1	<ul style="list-style-type: none"> Updated Note 3 in Table 4–8 on page 4–4. Updated Table 4–10 on page 4–6. Updated Table 4–20 on page 4–12 through Table 4–23 on page 4–13. Added rows $V_{IL(AC)}$ and $V_{IH(AC)}$ to each table. Updated Table 4–26 on page 4–14 through Table 4–29 on page 4–15. Updated Table 4–31 on page 4–16. Updated description of “External Timing Parameters” on page 4–33. Updated Table 4–36 on page 4–20. Added signals t_{OUTCO}, T_{XZ}, and T_{ZX} to Figure 4–4 on page 4–33. Added rows $t_{M512CLKENSU}$ and $t_{M512CLKENH}$ to Table 4–40 on page 4–24. Added rows $t_{M4CLKENSU}$ and $t_{M4CLKENH}$ to Table 4–41 on page 4–24. Updated Note 2 in Table 4–54 on page 4–35. Added rows $t_{MRAMCLKENSU}$ and $t_{MRAMCLKENH}$ to Table 4–42 on page 4–25. Updated Table 4–46 on page 4–29. Updated Table 4–47 on page 4–29.

Chapter	Date/Version	Changes Made
4		<ul style="list-style-type: none"> Updated Table 4–123 on page 4–85 through Table 4–126 on page 4–92. Updated Note 3 in Table 4–123 on page 4–85. Table 4–125 on page 4–88: moved to correct order in chapter, and updated table. Updated Table 4–126 on page 4–92. Updated Table 4–127 on page 4–94. Updated Table 4–128 on page 4–95.
	April 2004, v3.0	<ul style="list-style-type: none"> Table 4–129 on page 4–96: updated table and added Note 10. Updated Table 4–131 and Table 4–132 on page 4–100. Updated Table 4–110 on page 4–74. Updated Table 4–123 on page 4–85. Updated Table 4–124 on page 4–87. through Table 4–126 on page 4–92. Added Note 10 to Table 4–129 on page 4–96. Moved Table 4–127 on page 4–94 to correct order in the chapter. Updated Table 4–131 on page 4–100 through Table 4–132 on page 4–100. Deleted t_{XZ} and t_{ZX} from Figure 4–4. Waveform was added to Figure 4–6. The minimum and maximum duty cycle values in Note 3 of Table 4–8 were moved to a new Table 4–9. Changes were made to values in SSTL-3 Class I and II rows in Table 4–17. Note 1 was added to Table 4–34. Added t_{SU_R} and t_{SU_C} rows in Table 4–38. Changed Table 4–55 title from “EP1S10 Column Pin Fast Regional Clock External I/O Timing Parameters” to “EP1S10 External I/O Timing on Column Pins Using Fast Regional Clock Networks.” Changed values in Tables 4–46, 4–48 to 4–51, 4–128, and 4–131. Added t_{ARESET} row in Tables 4–127 to 4–132. Deleted -5 Speed Grade column in Tables 4–117 to 4–119 and 4–122 to 4–123. Fixed differential waveform in Figure 4–1. Added “Definition of I/O Skew” section. Added t_{SU} and t_{CO_C} rows and made changes to values in t_{PRE} and t_{CLKHL} rows in Table 4–46. Values changed in the t_{SU} and t_H rows in Table 4–47. Values changed in the $t_{M4KCLKHL}$ row in Table 4–49. Values changed in the $t_{MRAMCLKHL}$ row in Table 4–50. Added Table 4–51 to “Internal Timing Parameters” section. The timing information is preliminary in Tables 4–55 through 4–96. Table 4–111 was separated into 3 tables: Tables 4–111 to 4–113.
	November 2003, v2.2	<ul style="list-style-type: none"> Updated Tables 4–127 through 4–129.

M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO RAM

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed. The memory address and output width can be configured as $64\text{K} \times 8$ (or $64\text{K} \times 9$ bits), $32\text{K} \times 16$ (or $32\text{K} \times 18$ bits), $16\text{K} \times 32$ (or $16\text{K} \times 36$ bits), $8\text{K} \times 64$ (or $8\text{K} \times 72$ bits), and $4\text{K} \times 128$ (or $4\text{K} \times 144$ bits). The $4\text{K} \times 128$ configuration is unavailable in true dual-port mode because there are a total of 144 data output drivers in the block. Mixed-width configurations are also possible, allowing different read and write widths. [Tables 2-8](#) and [2-9](#) summarize the possible M-RAM block configurations:

Table 2-8. M-RAM Block Configurations (Simple Dual-Port)					
Read Port	Write Port				
	$64\text{K} \times 9$	$32\text{K} \times 18$	$16\text{K} \times 36$	$8\text{K} \times 72$	$4\text{K} \times 144$
$64\text{K} \times 9$	✓	✓	✓	✓	
$32\text{K} \times 18$	✓	✓	✓	✓	
$16\text{K} \times 36$	✓	✓	✓	✓	
$8\text{K} \times 72$	✓	✓	✓	✓	
$4\text{K} \times 144$					✓

Table 2–9. M-RAM Block Configurations (True Dual-Port)

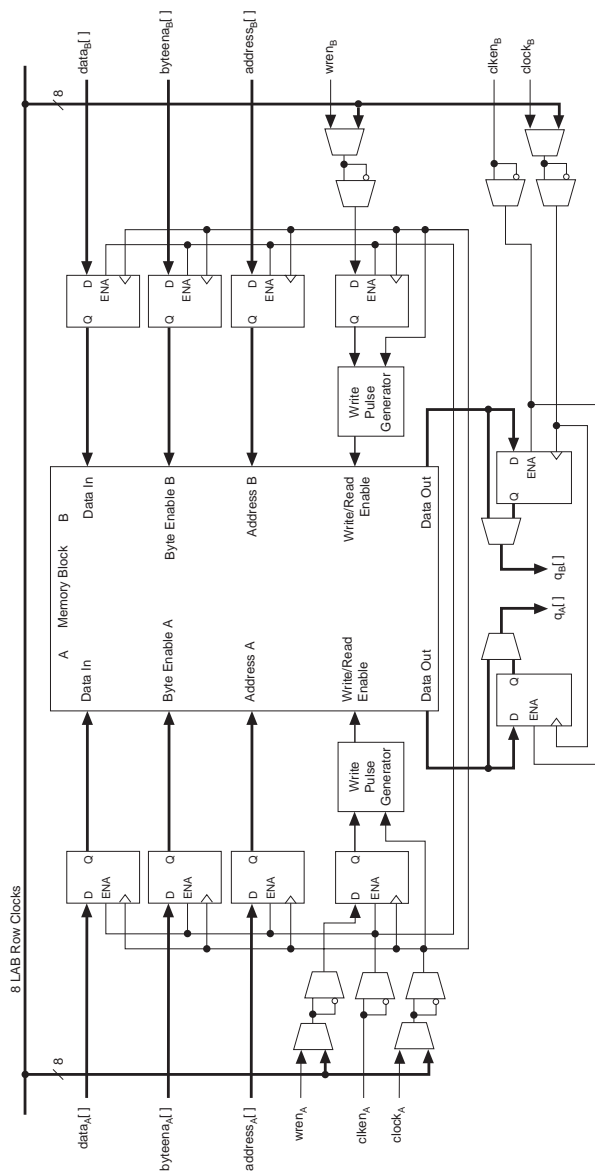
Port A	Port B			
	64K × 9	32K × 18	16K × 36	8K × 72
64K × 9	✓	✓	✓	✓
32K × 18	✓	✓	✓	✓
16K × 36	✓	✓	✓	✓
8K × 72	✓	✓	✓	✓

The read and write operation of the memory is controlled by the `WREN` signal, which sets the ports into either read or write modes. There is no separate read enable (`RE`) signal.

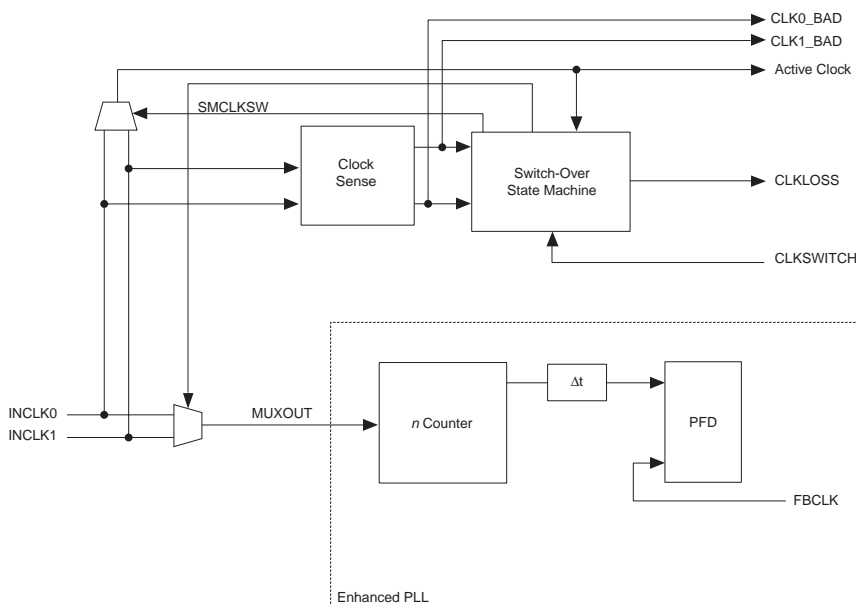
Writing into RAM is controlled by both the `WREN` and byte enable (`byteena`) signals for each port. The default value for the `byteena` signal is high, in which case writing is controlled only by the `WREN` signal. The byte enables are available for the $\times 18$, $\times 36$, and $\times 72$ modes. In the $\times 144$ simple dual-port mode, the two sets of `byteena` signals (`byteena_a` and `byteena_b`) are combined to form the necessary 16 byte enables. Tables 2–10 and 2–11 summarize the byte selection.

Table 2–10. Byte Enable for M-RAM Blocks *Notes (1), (2)*

<code>byteena[3..0]</code>	<code>datain $\times 18$</code>	<code>datain $\times 36$</code>	<code>datain $\times 72$</code>
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

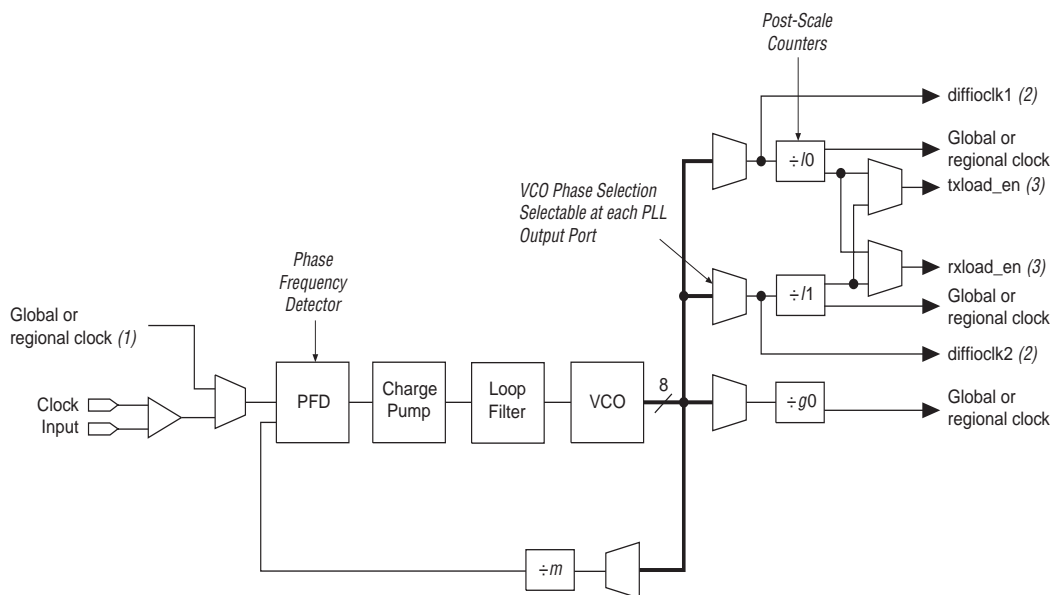
Figure 2–25. Input/Output Clock Mode in True Dual-Port Mode *Notes (1), (2)***Notes to Figure 2–25:**

- (1) All registers shown have asynchronous clear ports.
- (2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Figure 2–53. Clock Switchover Circuitry

There are two possible ways to use the clock switchover feature.

- Use automatic switchover circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of [Figure 2–53](#). In this case, the secondary clock becomes the reference clock for the PLL.
- Use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than $\pm 20\%$. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. You can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

Figure 2–58. Stratix Device Fast PLL**Notes to Figure 2–58:**

- (1) The global or regional clock input can be driven by an output from another PLL or any dedicated CLK or FCLK pin. It cannot be driven by internally-generated global signals.
- (2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.
- (3) This signal is a high-speed differential I/O support SERDES control signal.

Clock Multiplication & Division

Stratix device fast PLLs provide clock synthesis for PLL output ports using m /(post scaler) scaling factors. The input clock is multiplied by the m feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, m , per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and $g0$ counter for global clock output port; all range from 1 to 32.

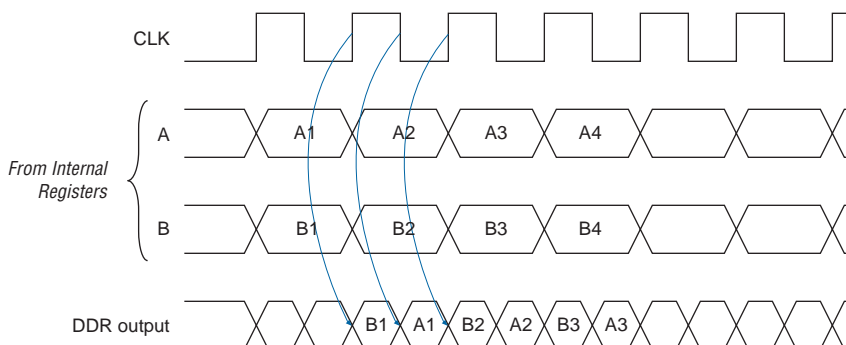
In the case of a high-speed differential interface, set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES. When used for clocking the SERDES, the m counter can range from 1 to 30. The VCO frequency is equal to $f_{IN} \times m$, where VCO frequency must be between 300 and 1000 MHz.

External Clock Inputs

Each fast PLL supports single-ended or differential inputs for source synchronous transmitters or for general-purpose use. Source-synchronous receivers support differential clock inputs. The fast PLL inputs are fed by CLK [0 . . 3], CLK [8 . . 11], and FPLL [7 . . 10] CLK pins, as shown in [Figure 2–50 on page 2–85](#).

[Table 2–22](#) shows the I/O standards supported by fast PLL input pins.

Table 2–22. Fast PLL Port I/O Standards (Part 1 of 2)		
I/O Standard	Input	
	INCLK	PLENABLE
LVTTTL	✓	✓
LVC MOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X 1.0		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	
Differential SSTL		
3.3-V GTL		
3.3-V GTL+	✓	
1.5-V HSTL Class I	✓	
1.5-V HSTL Class II		
1.8-V HSTL Class I	✓	
1.8-V HSTL Class II		
SSTL-18 Class I	✓	
SSTL-18 Class II		
SSTL-2 Class I	✓	

Figure 2–68. Output Timing Diagram in DDR Mode

The Stratix IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

Stratix devices support DDR SDRAM at up to 200 MHz (400-Mbps data rate) through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces up to 200 MHz. Stratix devices also provide preliminary support for reduced latency DRAM II (RLDRAM II) at rates up to 200 MHz through the dedicated phase-shift circuitry.



In addition to the required signals for external memory interfacing, Stratix devices offer the optional clock enable signal. By default the Quartus II software sets the clock enable signal high, which tells the output register to update with new values. The output registers hold their own values if the design sets the clock enable signal low. See [Figure 2–64](#).



To find out more about the DDR SDRAM specification, see the JEDEC web site (www.jedec.org). For information on memory controller megafunctions for Stratix devices, see the Altera web site (www.altera.com). See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices* for more information on DDR SDRAM interface in Stratix. Also see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices* and *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

The Stratix device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix devices.

Table 3–2. Stratix Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1S10	1,317
EP1S20	1,797
EP1S25	2,157
EP1S30	2,253
EP1S40	2,529
EP1S60	3,129
EP1S80	3,777

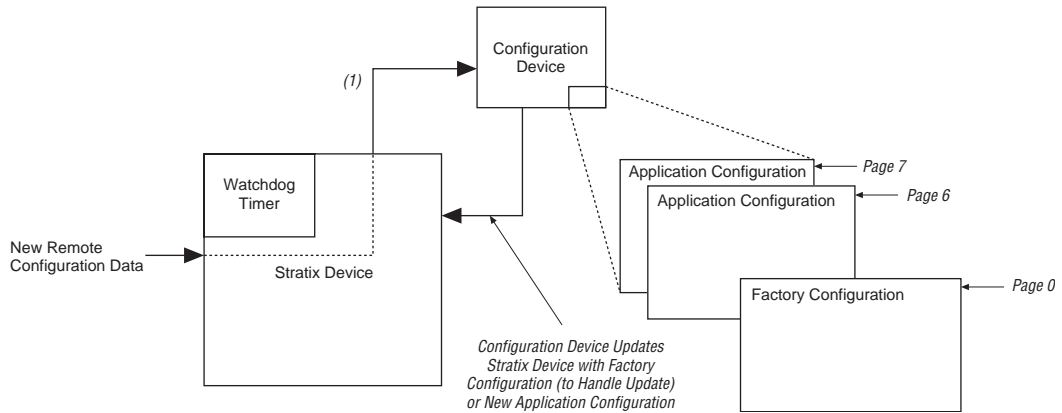
Table 3–3. 32-Bit Stratix Device IDCODE

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)
EP1S10	0000	0010 0000 0000 0001	000 0110 1110	1
EP1S20	0000	0010 0000 0000 0010	000 0110 1110	1
EP1S25	0000	0010 0000 0000 0011	000 0110 1110	1
EP1S30	0000	0010 0000 0000 0100	000 0110 1110	1
EP1S40	0000	0010 0000 0000 0101	000 0110 1110	1
EP1S60	0000	0010 0000 0000 0110	000 0110 1110	1
EP1S80	0000	0010 0000 0000 0111	000 0110 1110	1

Notes to Tables 3–2 and 3–3:

- (1) The most significant bit (MSB) is on the left.
- (2) The IDCODE's least significant bit (LSB) is always 1.

Figure 3–2. Stratix Device Remote Update



Note to Figure 3–2:

- (1) When the Stratix device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

Table 4–28. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8 \text{ mA}$ (3)	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8 \text{ mA}$ (3)			0.4	V

Table 4–29. 1.8-V HSTL Class II Specifications

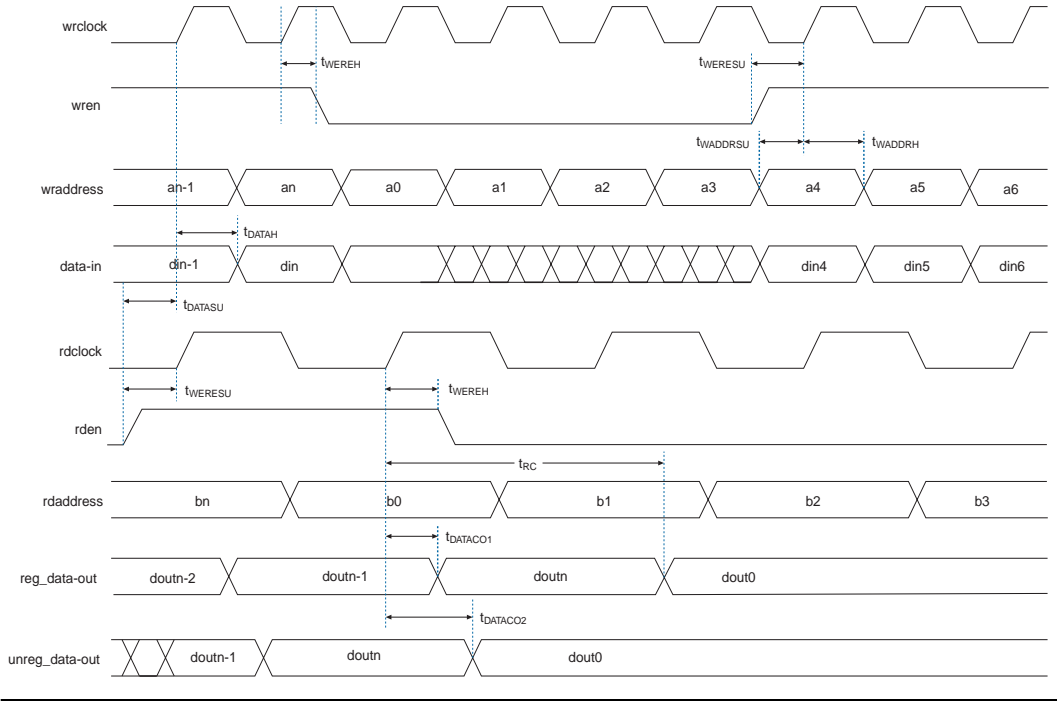
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -16 \text{ mA}$ (3)	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16 \text{ mA}$ (3)			0.4	V

Table 4–30. 1.5-V Differential HSTL Class I & Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Figure 4–3 shows the TriMatrix memory waveforms for the M512, M4K, and M-RAM timing parameters shown in Tables 4–40 through 4–42.

Figure 4–3. Dual-Port RAM Timing Microparameter Waveform



Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–44 through 4–50 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–43. Routing Delay Internal Timing Microparameter Descriptions (Part 1 of 2)	
Symbol	Parameter
t_{R4}	Delay for an R4 line with average loading; covers a distance of four LAB columns.
t_{R8}	Delay for an R8 line with average loading; covers a distance of eight LAB columns.
t_{R24}	Delay for an R24 line with average loading; covers a distance of 24 LAB columns.

Table 4–50. M-RAM Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{MRAMBESU}	25		25		28		33		ps
t_{MRAMBEH}	18		20		23		27		ps
$t_{\text{MRAMDATAASU}}$	25		25		28		33		ps
$t_{\text{MRAMDATAAH}}$	18		20		23		27		ps
$t_{\text{MRAMADDRASU}}$	25		25		28		33		ps
$t_{\text{MRAMADDRAH}}$	18		20		23		27		ps
$t_{\text{MRAMDATABSU}}$	25		25		28		33		ps
$t_{\text{MRAMDATABH}}$	18		20		23		27		ps
$t_{\text{MRAMADDRBSU}}$	25		25		28		33		ps
$t_{\text{MRAMADDRBH}}$	18		20		23		27		ps
$t_{\text{MRAMDATA CO1}}$		1,038		1,053		1,210		1,424	ps
$t_{\text{MRAMDATA CO2}}$		4,362		4,939		5,678		6,681	ps
$t_{\text{MRAMCLKHL}}$	1,000		1,111		1,190		1,400		ps
t_{MRAMCLR}	135		150		172		202		ps

Table 4–51. Routing Delay Internal Timing Parameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{R4}		268		295		339		390	ps
t_{R8}		371		349		401		461	ps
t_{R24}		465		512		588		676	ps
t_{C4}		440		484		557		641	ps
t_{C8}		577		634		730		840	ps
t_{C16}		445		489		563		647	ps
t_{LOCAL}		313		345		396		455	ps

Routing delays vary depending on the load on that specific routing line. The Quartus II software reports the routing delay information when running the timing analysis for a design.

Table 4–87. EP1S60 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.000		2.152		2.441		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.051	5.900	3.051	6.340	3.051	6.977	NA	NA	ns
t_{XZ}	2.991	5.774	2.991	6.208	2.991	6.853	NA	NA	ns
t_{ZX}	2.991	5.774	2.991	6.208	2.991	6.853	NA	NA	ns
t_{INSUPLL}	1.315		1.362		1.543		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
t_{OUTCOPLL}	1.029	2.196	1.029	2.303	1.029	2.323	NA	NA	ns
t_{XZPLL}	0.969	2.070	0.969	2.171	0.969	2.199	NA	NA	ns
t_{ZXPLL}	0.969	2.070	0.969	2.171	0.969	2.199	NA	NA	ns

Table 4–88. EP1S60 External I/O Timing on Row Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.144		3.393		3.867		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.643	5.275	2.643	5.654	2.643	6.140	NA	NA	ns
t_{XZ}	2.670	5.329	2.670	5.710	2.670	6.208	NA	NA	ns
t_{ZX}	2.670	5.329	2.670	5.710	2.670	6.208	NA	NA	ns

Table 4–108. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,571		1,650		1,650		1,650	ps
	4 mA		594		624		624		624	ps
	8 mA		208		218		218		218	ps
	12 mA		0		0		0		0	ps
3.3-V LVTTTL	4 mA		1,571		1,650		1,650		1,650	ps
	8 mA		1,393		1,463		1,463		1,463	ps
	12 mA		596		626		626		626	ps
	16 mA		562		590		590		590	ps
2.5-V LVTTTL	2 mA		2,562		2,690		2,690		2,690	ps
	8 mA		1,343		1,410		1,410		1,410	ps
	12 mA		864		907		907		907	ps
	16 mA		945		992		992		992	ps
1.8-V LVTTTL	2 mA		6,306		6,621		6,621		6,621	ps
	8 mA		3,369		3,538		3,538		3,538	ps
	12 mA		2,932		3,079		3,079		3,079	ps
1.5-V LVTTTL	2 mA		9,759		10,247		10,247		10,247	ps
	4 mA		6,830		7,172		7,172		7,172	ps
	8 mA		5,699		5,984		5,984		5,984	ps
GTL+			–333		–350		–350		–350	ps
CTT			591		621		621		621	ps
SSTL-3 Class I			267		280		280		280	ps
SSTL-3 Class II			–346		–363		–363		–363	ps
SSTL-2 Class I			481		505		505		505	ps
SSTL-2 Class II			–58		–61		–61		–61	ps
SSTL-18 Class I			2,207		2,317		2,317		2,317	ps
1.5-V HSTL Class I			1,966		2,064		2,064'		2,064	ps
1.8-V HSTL Class I			1,208		1,268		1,460		1,720	ps

Tables 4–109 and 4–110 show the adder delays for the column and row IOE programmable delays. These delays are controlled with the Quartus II software logic options listed in the Parameter column.

Table 4–109. Stratix IOE Programmable Delays on Column Pins *Note (1)*

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off		3,970		4,367		5,022		5,908	ps
	Small		3,390		3,729		4,288		5,045	ps
	Medium		2,810		3,091		3,554		4,181	ps
	Large		224		235		270		318	ps
	On		224		235		270		318	ps
Decrease input delay to input register	Off		3,900		4,290		4,933		5,804	ps
	On		0		0		0		0	ps
Decrease input delay to output register	Off		1,240		1,364		1,568		1,845	ps
	On		0		0		0		0	ps
Increase delay to output pin	Off		0		0		0		0	ps
	On		397		417		417		417	ps
Increase delay to output enable pin	Off		0		0		0		0	ps
	On		338		372		427		503	ps
Increase output clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase input clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase output enable clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase t_{ZX} delay to output pin	Off		0		0		0		0	ps
	On		2,199		2,309		2,309		2,309	ps

process and operating conditions. Run the timing analyzer in the Quartus II software at the fast and slow operating conditions to see the phase shift range that is achieved below these frequencies.

Table 4–135. Stratix DLL Low Frequency Limit for Full Phase Shift

Phase Shift	Minimum Frequency for Full Phase Shift	Unit
72°	119	MHz
90°	149	MHz

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