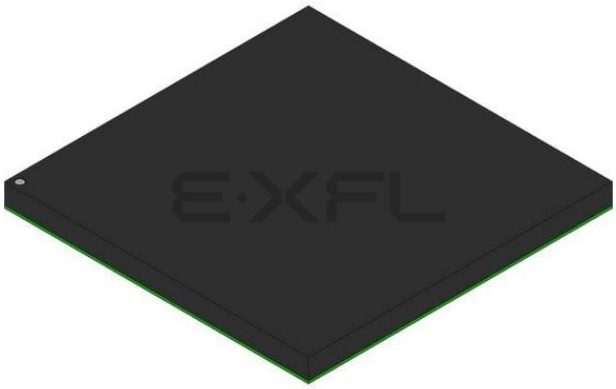

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	683
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	956-BBGA
Supplier Device Package	956-BGA (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1s60b956c6n

Chapter 3. Configuration & Testing

Chapter 4. DC & Switching Characteristics

Chapter	Date/Version	Changes Made
4		• Table 4–48 on page 4–30: added rows $t_{M512CLKSENSU}$ and $t_{M512CLKENH}$, and updated symbol names. • Updated power-up current (ICCINT) required to power a Stratix device on page 4–17. • Updated Table 4–37 on page 4–22 through Table 4–43 on page 4–27. • Table 4–49 on page 4–31: added rows $t_{M4KCLKENSU}$, $t_{M4KCLKENH}$, $t_{M4KBESU}$, and $t_{M4KBEH,}$ deleted rows $t_{M4KRADDRASU}$ and $t_{M4KRADDRH}$, and updated symbol names. • Table 4–50 on page 4–31: added rows $t_{MRAMCLKENSU}$, $t_{MRAMCLKENH}$, $t_{MRAMBESU}$, and $t_{MRAMBEH}$, deleted rows $t_{MRAMADDRASU}$ and $t_{MRAMRADDRH}$, and updated symbol names. • Table 4–52 on page 4–34: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. • Table 4–52 on page 4–34: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. • Table 4–53 on page 4–34: updated table and added rows t_{XZPLL} and t_{ZXPLL}. • Updated Note 2 in Table 4–53 on page 4–34. • Table 4–54 on page 4–35: updated table, deleted “Conditions” column, and added rows t_{XZPLL} and t_{ZXPLL}. • Updated Note 2 in Table 4–54 on page 4–35. • Deleted Note 2 from Table 4–55 on page 4–36 through Table 4–66 on page 4–41. • Updated Table 4–55 on page 4–36 through Table 4–96 on page 4–56. Added rows T_{XZ}, T_{ZX}, T_{XZPLL}, and $T_{ZXPLL.}$ • Added Note 4 to Table 4–101 on page 4–62. • Deleted Note 1 from Table 4–67 on page 4–42 through Table 4–84 on page 4–50. • Added new section “I/O Timing Measurement Methodology” on page 4–60. • Deleted Note 1 from Table 4–67 on page 4–42 through Table 4–84 on page 4–50. • Deleted Note 2 from Table 4–85 on page 4–51 through Table 4–96 on page 4–56. • Added Note 4 to Table 4–101 on page 4–62. • Table 4–102 on page 4–64: updated table and added Note 4. • Updated description of “External I/O Delay Parameters” on page 4–66. • Added Note 1 to Table 4–109 on page 4–73 and Table 4–110 on page 4–74. • Updated Table 4–103 on page 4–66 through Table 4–110 on page 4–74. • Deleted Note 2 from Table 4–103 on page 4–66 through Table 4–106 on page 4–69. • Added new paragraph about output adder delays on page 4–68. • Updated Table 4–110 on page 4–74. • Added Note 1 to Table 4–111 through Table 4–113 on page 4–75.

Table 1–1. Stratix Device Features — EP1S10, EP1S20, EP1S25, EP1S30

Feature	EP1S10	EP1S20	EP1S25	EP1S30
LEs	10,570	18,460	25,660	32,470
M512 RAM blocks (32 × 18 bits)	94	194	224	295
M4K RAM blocks (128 × 36 bits)	60	82	138	171
M-RAM blocks (4K × 144 bits)	1	2	2	4
Total RAM bits	920,448	1,669,248	1,944,576	3,317,184
DSP blocks	6	10	10	12
Embedded multipliers *(1)*	48	80	80	96
PLLs	6	6	6	10
Maximum user I/O pins	426	586	706	726

Table 1–2. Stratix Device Features — EP1S40, EP1S60, EP1S80

Feature	EP1S40	EP1S60	EP1S80
LEs	41,250	57,120	79,040
M512 RAM blocks (32 × 18 bits)	384	574	767
M4K RAM blocks (128 × 36 bits)	183	292	364
M-RAM blocks (4K × 144 bits)	4	6	9
Total RAM bits	3,423,744	5,215,104	7,427,520
DSP blocks	14	18	22
Embedded multipliers *(1)*	112	144	176
PLLs	12	12	12
Maximum user I/O pins	822	1,022	1,238

Note to Tables 1–1 and 1–2:

(1) This parameter lists the total number of 9 × 9-bit multipliers for each device. For the total number of 18 × 18-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 2. For the total number of 36 × 36-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 8.

2. Stratix Architecture

S51002-3.2

Functional Description

Stratix® devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

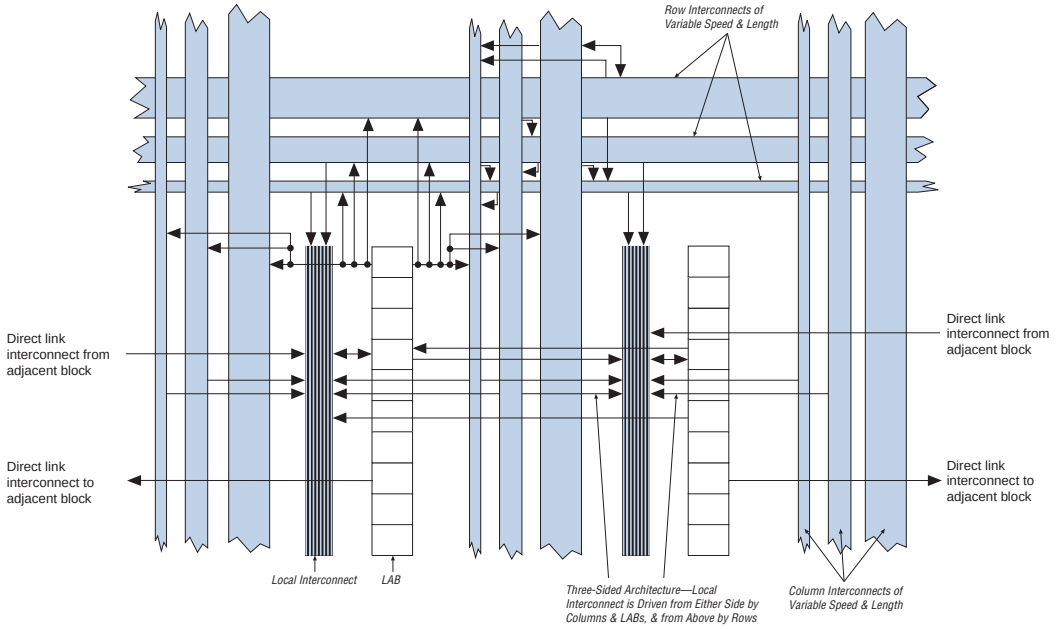
M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device's logic array.

Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with

Figure 2–2. Stratix LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

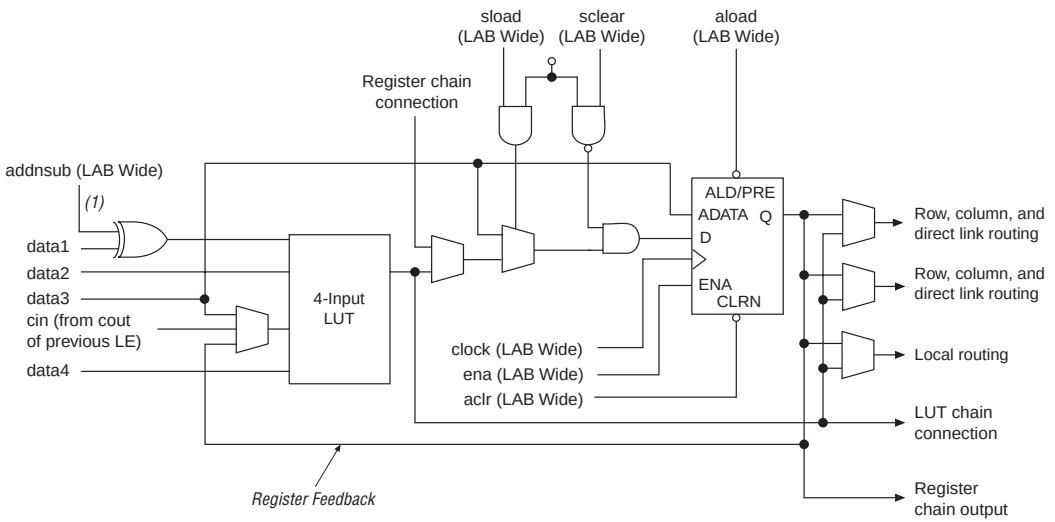
asynchronous preset load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The addnsub control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

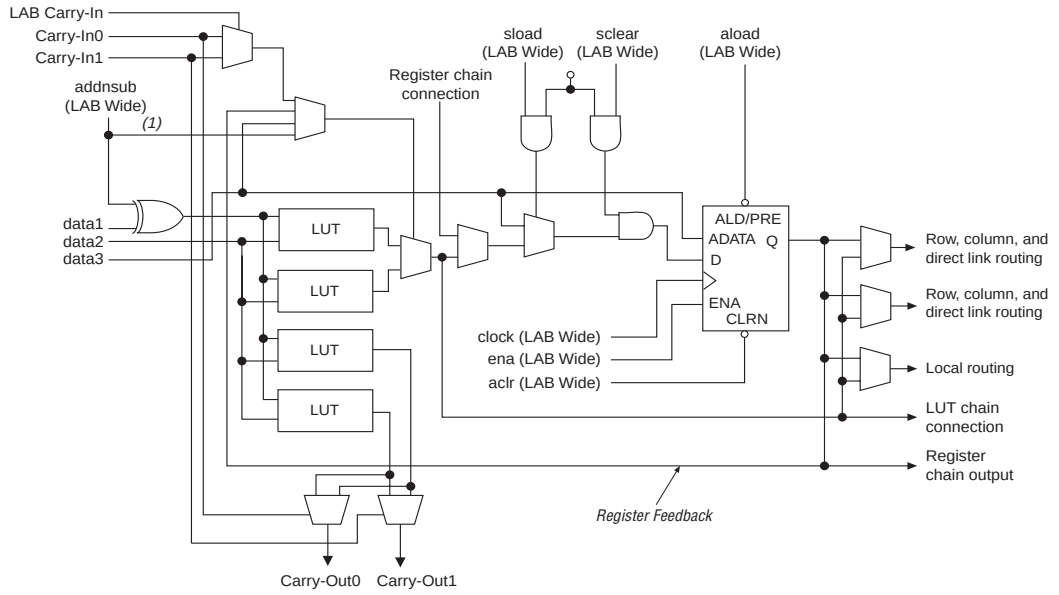
The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–6). The Quartus II Compiler automatically selects the carry-in or the data3 signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the data3 input of the LE. LEs in normal mode support packed registers.

Figure 2–6. LE in Normal Mode



Note to Figure 2–6:
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Figure 2–7. LE in Dynamic Arithmetic Mode



Note to Figure 2–7:
(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

can drive other R8 interconnects to extend their range as well as C8 interconnects for row-to-row connections. One R8 interconnect is faster than two R4 interconnects connected together.

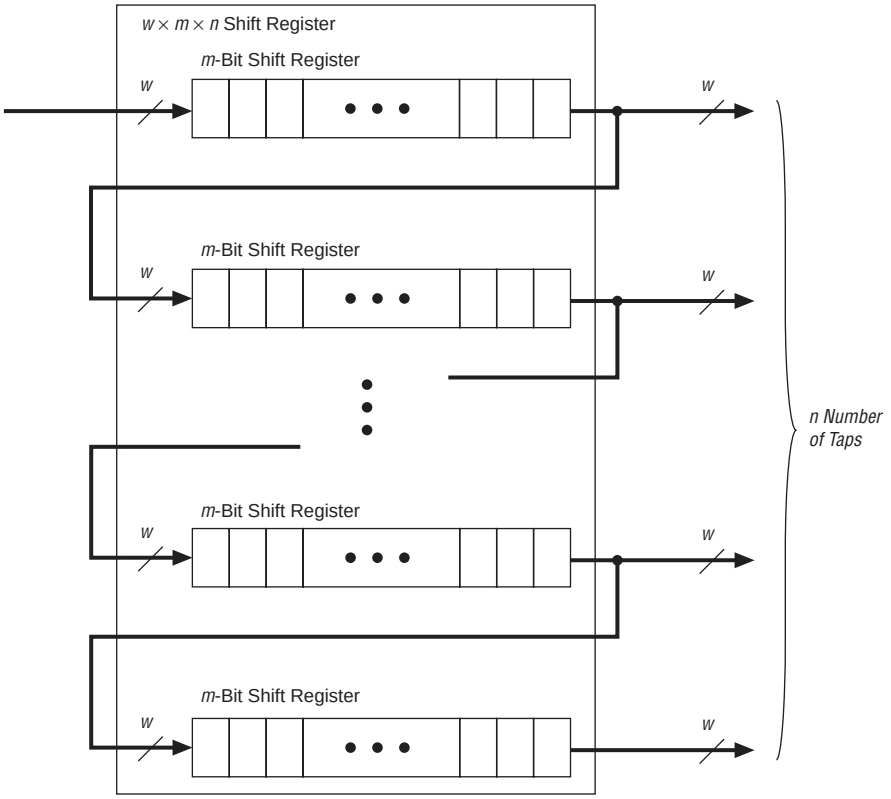
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, TriMatrix memory and DSP blocks, and horizontal IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C8 interconnects traversing a distance of eight blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–10 shows the LUT chain and register chain interconnects.

Figure 2–14. Shift Register Memory Configuration

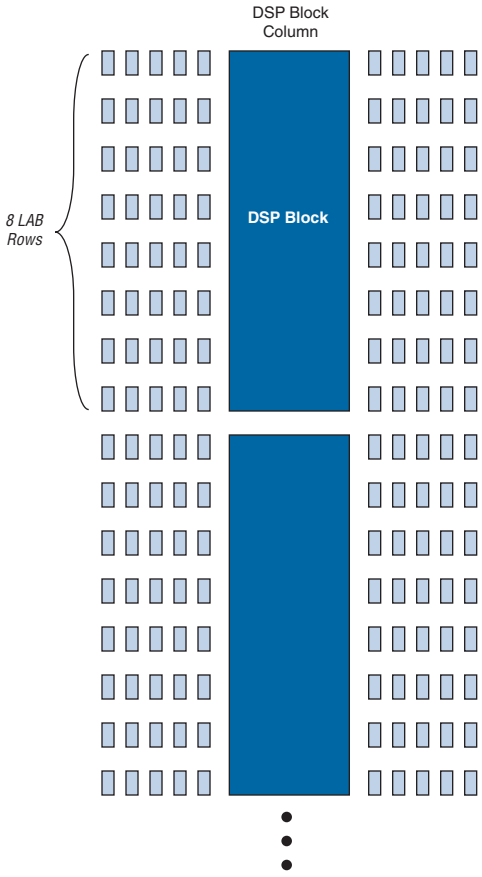


Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The large number of M512 blocks are ideal for designs with many shallow first-in first-out (FIFO) buffers. M4K blocks provide additional resources for channelized functions that do not require large amounts of storage. The M-RAM blocks provide a large single block of RAM ideal for data packet storage. The different-sized blocks allow Stratix devices to efficiently support variable-sized memory in designs.

The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

Figure 2–29. DSP Blocks Arranged in Columns



and/or output enable registers. A programmable delay exists to increase the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 2–24 shows the programmable delays for Stratix devices.

Table 2–24. Stratix Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output pin delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register
Output enable clock enable delay	Increase output enable clock enable delay

The IOE registers in Stratix devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available for the IOE registers.

Double-Data Rate I/O Pins

Stratix devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–65 shows an IOE configured for DDR input. Figure 2–66 shows the DDR input timing diagram.

Table 2–28 shows the possible settings for the I/O standards with drive strength control.

Table 2–28. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2
GTL/GTL+ 1.5-V HSTL Class I and II 1.8-V HSTL Class I and II SSTL-3 Class I and II SSTL-2 Class I and II SSTL-18 Class I and II	Support max and min strength

Notes to Table 2–28:
(1) This is the Quartus II software default current setting.
(2) I/O banks 1, 2, 5, and 6 do not support this setting.

Quartus II software version 4.2 and later will report current strength as "PCI Compliant" for 3.3-V PCI, 3.3-V PCI-X 1.0, and Compact PCI I/O standards.

Stratix devices support series on-chip termination (OCT) using programmable drive strength. For more information, contact your Altera Support Representative.

Open-Drain Output

Stratix devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Slew-Rate Control

The output buffer for each Stratix device I/O pin has a programmable output slew-rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each

Table 2–37 shows the number of channels that each fast PLL can clock in EP1S10, EP1S20, and EP1S25 devices. Tables 2–38 through Table 2–41 show this information for EP1S30, EP1S40, EP1S60, and EP1S80 devices.

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 1 of 2) Note (1)

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S10	484-pin FineLine BGA	Transmitter (2)	20	840 (4)	5	5	5	5
				840 (3)	10	10	10	10
		Receiver	20	840 (4)	5	5	5	5
				840 (3)	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter (2)	36	624 (4)	9	9	9	9
				624 (3)	18	18	18	18
		Receiver	36	624 (4)	9	9	9	9
				624 (3)	18	18	18	18
	780-pin FineLine BGA	Transmitter (2)	44	840 (4)	11	11	11	11
				840 (3)	22	22	22	22
		Receiver	44	840 (4)	11	11	11	11
				840 (3)	22	22	22	22
EP1S20	484-pin FineLine BGA	Transmitter (2)	24	840 (4)	6	6	6	6
				840 (3)	12	12	12	12
		Receiver	20	840 (4)	5	5	5	5
				840 (3)	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter (2)	48	624 (4)	12	12	12	12
				624 (3)	24	24	24	24
		Receiver	50	624 (4)	13	12	12	13
				624 (3)	25	25	25	25
	780-pin FineLine BGA	Transmitter (2)	66	840 (4)	17	16	16	17
				840 (3)	33	33	33	33
		Receiver	66	840 (4)	17	16	16	17
				840 (3)	33	33	33	33

Table 2–40. EP1S60 Differential Channels (Part 2 of 2) Note (1)

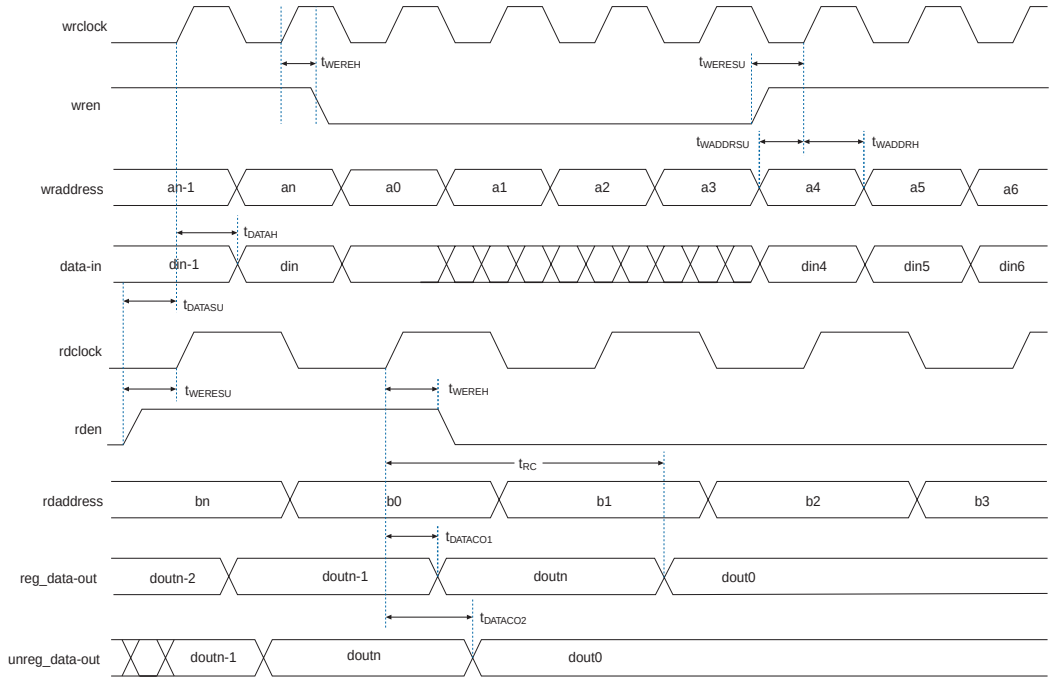
Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
1,020-pin FineLine BGA	Transmitter (4)	80 (12) (7)	840	12 (2)	10 (4)	10 (4)	12 (2)	20	20	20	20
			840 (5), (8)	22 (6)	22 (6)	22 (6)	22 (6)	20	20	20	20
	Receiver	80 (10) (7)	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5), (8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)
1,508-pin FineLine BGA	Transmitter (4)	80 (36) (7)	840	12 (8)	10 (10)	10 (10)	12 (8)	20	20	20	20
			840 (5),(8)	22 (18)	22 (18)	22 (18)	22 (18)	20	20	20	20
	Receiver	80 (36) (7)	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 (5),(8)	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)

Table 2–41. EP1S80 Differential Channels (Part 1 of 2) Note (1)

Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
956-pin BGA	Transmitter (4)	80 (40) (7)	840	10	10	10	10	20	20	20	20
			840 (5),(8)	20	20	20	20	20	20	20	20
	Receiver	80	840	20	20	20	20	10	10	10	10
			840 (5),(8)	40	40	40	40	10	10	10	10
1,020-pin FineLine BGA	Transmitter (4)	92 (12) (7)	840	10 (2)	10 (4)	10 (4)	10 (2)	20	20	20	20
			840 (5),(8)	20 (6)	20 (6)	20 (6)	20 (6)	20	20	20	20
	Receiver	90 (10) (7)	840	20	20	20	20	10 (2)	10 (3)	10 (3)	10 (2)
			840 (5),(8)	40	40	40	40	10 (2)	10 (3)	10 (3)	10 (2)

Figure 4–3 shows the TriMatrix memory waveforms for the M512, M4K, and M-RAM timing parameters shown in Tables 4–40 through 4–42.

Figure 4–3. Dual-Port RAM Timing Microparameter Waveform



Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–44 through 4–50 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–43. Routing Delay Internal Timing Microparameter Descriptions (Part 1 of 2)

Symbol	Parameter
t_{R4}	Delay for an R4 line with average loading; covers a distance of four LAB columns.
t_{R8}	Delay for an R8 line with average loading; covers a distance of eight LAB columns.
t_{R24}	Delay for an R24 line with average loading; covers a distance of 24 LAB columns.

Table 4–63. EP1S20 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.351		1.479		1.699		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.732	5.380	2.732	5.728	2.732	6.240	NA	NA	ns
t_{XZ}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
t_{ZX}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
$t_{INSUPLL}$	0.923		0.971		1.098		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.210	2.544	1.210	2.648	1.210	2.715	NA	NA	ns
t_{XZPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns
t_{ZXPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns

Table 4–64. EP1S20 External I/O Timing on Row Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.032		2.207		2.535		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.492	5.018	2.492	5.355	2.492	5.793	NA	NA	ns
t_{XZ}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns
t_{ZX}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns

Table 4–123. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVDS *(2)*	400	311	311	MHz
HyperTransport technology *(2)*	420	400	400	MHz

Notes to Tables 4–120 through 4–123:

(1) Differential SSTL-2 outputs are only available on column clock pins.
(2) These parameters are only available on row I/O pins.
(3) SSTL-2 in maximum drive strength condition. See Table 4–101 on page 4–62 for more information on exact loading conditions for each I/O standard.
(4) SSTL-2 in minimum drive strength with ≤10pF output load condition.
(5) SSTL-2 in minimum drive strength with > 10pF output load condition.
(6) Differential SSTL-2 outputs are only supported on column clock pins.

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 4 of 4) Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{DUTY}	LVDS (J = 2 through 10)	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (J =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100			100	µs

Notes to Table 4–125:

(1) When J = 4, 7, 8, and 10, the SERDES block is used.

(2) When J = 2 or J = 1, the SERDES is bypassed.

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