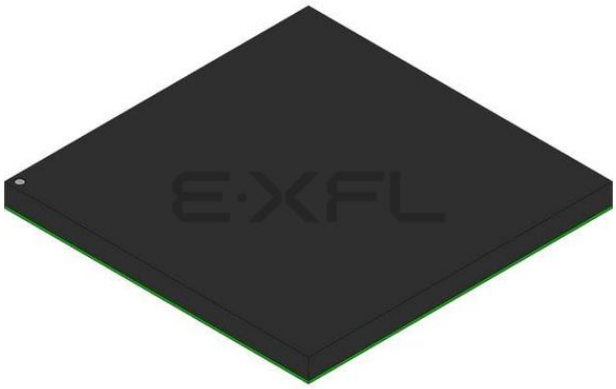

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 683 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 956-BBGA |
| Supplier Device Package | 956-BGA (40x40) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1s60b956c7 |

| Chapter | Date/Version | Changes Made |
|---|---|---|
| 2 | July 2003, v2.0 | • Added reference on page 2-73 to Figures 2-50 and 2-51 for RCLK connections.<br>• Updated ranges for EPLL post-scale and pre-scale dividers on page 2-85.<br>• Updated PLL Reconfiguration frequency from 25 to 22 MHz on page 2-87.<br>• New requirement to assert are set signal each PLL when it has to re-acquire lock on either a new clock after loss of lock (page 2-96).<br>• Updated max input frequency for CLK[1,3,8,10] from 462 to 500, Table 2-24.<br>• Renamed impedance matching to series termination throughout.<br>• Updated naming convention for DQS pins on page 2-112 to match pin tables.<br>• Added DDR SDRAM Performance Specification on page 2-117.<br>• Added external reference resistor values for terminator technology (page 2-136).<br>• Added Terminator Technology Specification on pages 2-137 and 2-138.<br>• Updated Tables 2-45 to 2-49 to reflect PLL cross-bank support for high speed differential channels at full speed.<br>• Wire bond package performance specification for "high" speed channels was increased to 624 Mbps from 462 Mbps throughout chapter. |
| 3 | July 2005, v1.3 | • Updated "Operating Modes" section.<br>• Updated "Temperature Sensing Diode" section.<br>• Updated "IEEE Std. 1149.1 (JTAG) Boundary-Scan Support" section.<br>• Updated "Configuration" section. |
| | January 2005, v1.2 | • Updated limits for JTAG chain of devices. |
| | September 2004, v1.1 | • Added new section, "Stratix Automated Single Event Upset (SEU) Detection" on page 3–12.<br>• Updated description of "Custom-Built Circuitry" on page 3–13. |
| | April 2003, v1.0 | • No new changes in *Stratix Device Handbook* v2.0. |
| 4 | January 2006, v3.4 | • Added Table 4–135. |
| | July 2005, v3.3 | • Updated Tables 4–6 and 4–30.<br>• Updated Tables 4–103 through 4–108.<br>• Updated Tables 4–114 through 4–124.<br>• Updated Table 4–129.<br>• Added Table 4–130. |

Stratix devices are available in space-saving FineLine BGA® and ball-grid array (BGA) packages (see Tables 1–3 through 1–5). All Stratix devices support vertical migration within the same package (for example, you can migrate between the EP1S10, EP1S20, and EP1S25 devices in the 672-pin BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migrational. The Quartus® II software can automatically cross reference and place all pins except differential pins for migration when given a device migration list. You must use the pin-outs for each device to verify the differential placement migration. A future version of the Quartus II software will support differential pin migration.

*Table 1–3. Stratix Package Options & I/O Pin Counts*

| Device | 672-Pin BGA | 956-Pin BGA | 484-Pin FineLine BGA | 672-Pin FineLine BGA | 780-Pin FineLine BGA | 1,020-Pin FineLine BGA | 1,508-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|
| EP1S10 | 345 | | 335 | 345 | 426 | | |
| EP1S20 | 426 | | 361 | 426 | 586 | | |
| EP1S25 | 473 | | | 473 | 597 | 706 | |
| EP1S30 | | 683 | | | 597 | 726 | |
| EP1S40 | | 683 | | | 615 | 773 | 822 |
| EP1S60 | | 683 | | | | 773 | 1,022 |
| EP1S80 | | 683 | | | | 773 | 1,203 |

*Note to Table 1–3:*

(1) All I/O pin counts include 20 dedicated clock input pins (`clk[15..0]p`, `clk0n`, `clk2n`, `clk9n`, and `clk11n`) that can be used for data inputs.

*Table 1–4. Stratix BGA Package Sizes*

| Dimension | 672 Pin | 956 Pin |
|---|---|---|
| Pitch (mm) | 1.27 | 1.27 |
| Area (mm²) | 1,225 | 1,600 |
| Length × width (mm × mm) | 35 × 35 | 40 × 40 |

functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

## LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 2–14 for more information on LUT chain and register chain connections.

## addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition, and subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

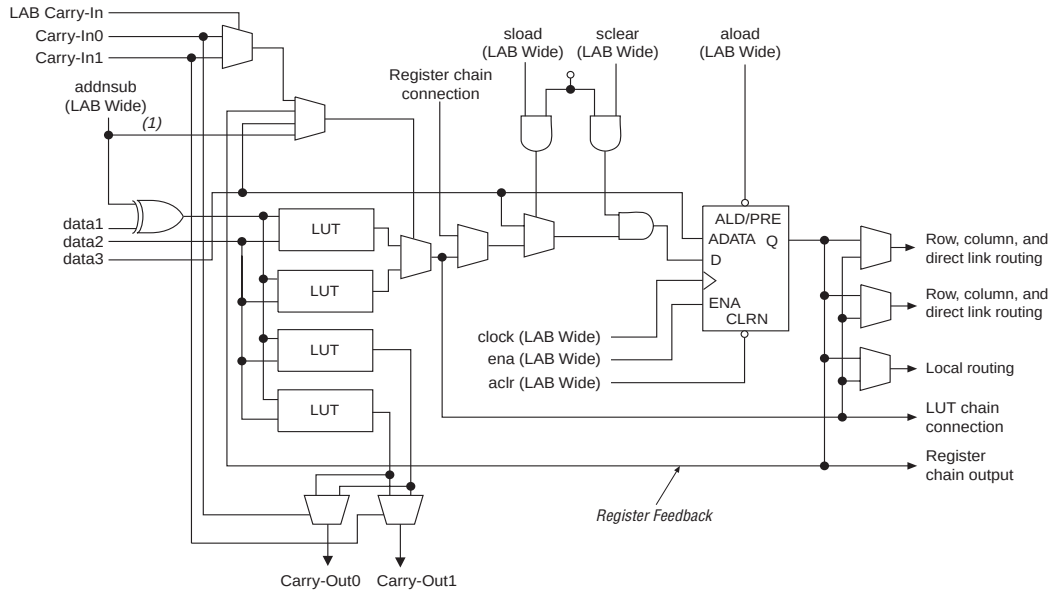
## LE Operating Modes

The Stratix LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0` and `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear,

*Figure 2–7. LE in Dynamic Arithmetic Mode*



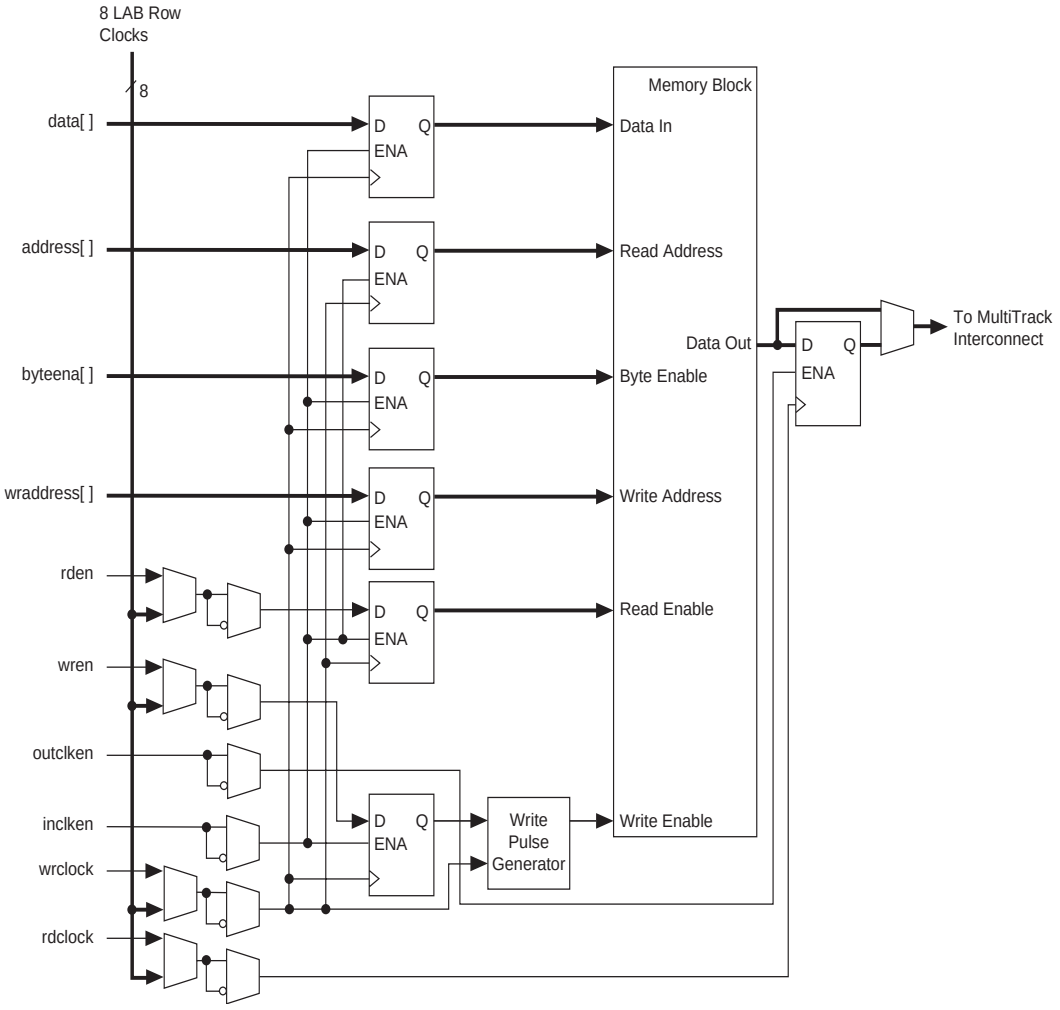

*Note to Figure 2–7:*
(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

### *Carry-Select Chain*

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

*Figure 2–26. Input/Output Clock Mode in Simple Dual-Port Mode* Notes (1), (2)

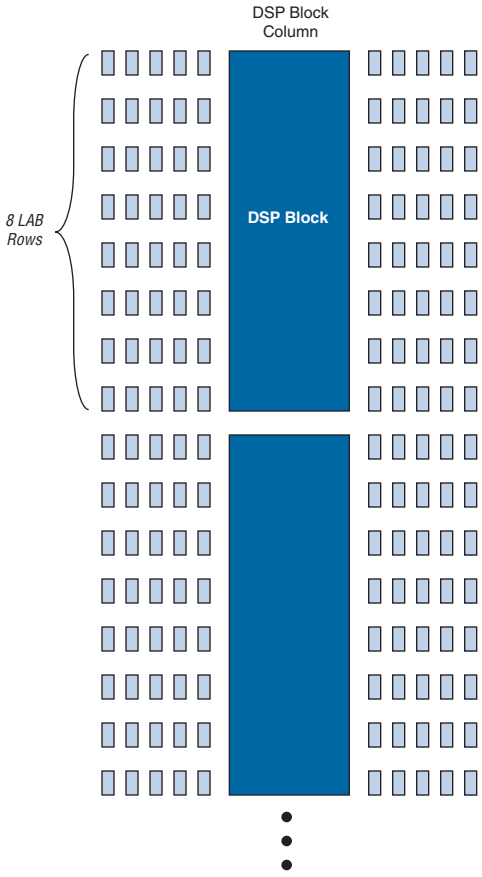



*Notes to Figure 2–26:*

(1) All registers shown except the `rden` register have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

*Figure 2–29. DSP Blocks Arranged in Columns*



The variation due to process, voltage, and temperature is about ±15% on the delay settings. PLL reconfiguration can control the clock delay shift elements, but not the VCO phase shift multiplexers, during system operation.

### *Spread-Spectrum Clocking*

Stratix device enhanced PLLs use spread-spectrum technology to reduce electromagnetic interference generation from a system by distributing the energy over a broader frequency range. The enhanced PLL typically provides 0.5% down spread modulation using a triangular profile. The modulation frequency is programmable. Enabling spread-spectrum for a PLL affects all of its outputs.

### *Lock Detect*

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. You may need to gate the lock signal for use as a system control. The lock signal from the locked port can drive the logic array or an output pin.

Whenever the PLL loses lock (for example, `inclk` jitter, clock switchover, PLL reconfiguration, power supply noise, and so on), the PLL must be reset with the `areset` signal to guarantee correct phase relationship between the PLL output clocks. If the phase relationship between the input clock versus output clock, and between different output clocks from the PLL is not important in the design, then the PLL need not be reset.

See the *Stratix FPGA Errata Sheet* for more information on implementing the gated lock signal in a design.

### *Programmable Duty Cycle*

The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

### *Advanced Clear & Enable Control*

There are several control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

Tables 2–25 and 2–26 show the performance specification for DDR SDRAM, RLDRAM II, QDR SRAM, QDRII SRAM, and ZBT SRAM interfaces in EP1S10 through EP1S40 devices and in EP1S60 and EP1S80 devices. The DDR SDRAM and QDR SRAM numbers in Table 2–25 have been verified with hardware characterization with third-party DDR SDRAM and QDR SRAM devices over temperature and voltage extremes.

*Table 2–25. External RAM Support in EP1S10 through EP1S40 Devices*

| DDR Memory Type | I/O Standard | Maximum Clock Rate (MHz) | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | -5 Speed Grade | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | |
| | | Flip-Chip | Flip-Chip | Wire-Bond | Flip-Chip | Wire-Bond | Flip-Chip | Wire-Bond |
| DDR SDRAM *(1)*, *(2)* | SSTL-2 | 200 | 167 | 133 | 133 | 100 | 100 | 100 |
| DDR SDRAM - side banks *(2)*, *(3)*, *(4)* | SSTL-2 | 150 | 133 | 110 | 133 | 100 | 100 | 100 |
| RLDRAM II *(4)* | 1.8-V HSTL | 200 | *(5)* | *(5)* | *(5)* | *(5)* | *(5)* | *(5)* |
| QDR SRAM *(6)* | 1.5-V HSTL | 167 | 167 | 133 | 133 | 100 | 100 | 100 |
| QDRII SRAM *(6)* | 1.5-V HSTL | 200 | 167 | 133 | 133 | 100 | 100 | 100 |
| ZBT SRAM *(7)* | LVTTL | 200 | 200 | 200 | 167 | 167 | 133 | 133 |

***Notes to Table 2–25:***

(1) These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).

(2) For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*

(3) DDR SDRAM is supported on the Stratix device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.

(4) These performance specifications are preliminary.

(5) This device does not support RLDRAM II.

(6) For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

(7) For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

*Table 2–27. DQS & DQ Bus Mode Support (Part 2 of 2)* Note (1)

| Device | Package | Number of ×8 Groups | Number of ×16 Groups | Number of ×32 Groups |
|---|---|---|---|---|
| EP1S25 | 672-pin BGA<br>672-pin FineLine BGA | 16 (3) | 8 | 4 |
| | 780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S30 | 956-pin BGA<br>780-pin FineLine BGA<br>1,020-pin FineLine BGA | 20 | 8 | 4 |
| EP1S40 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S60 | 956-pin BGA<br>1,020-pin FineLine BGA<br>1,508-pin FineLine BGA | 20 | 8 | 4 |
| EP1S80 | 956-pin BGA<br>1,508-pin FineLine BGA<br>1,923-pin FineLine BGA | 20 | 8 | 4 |

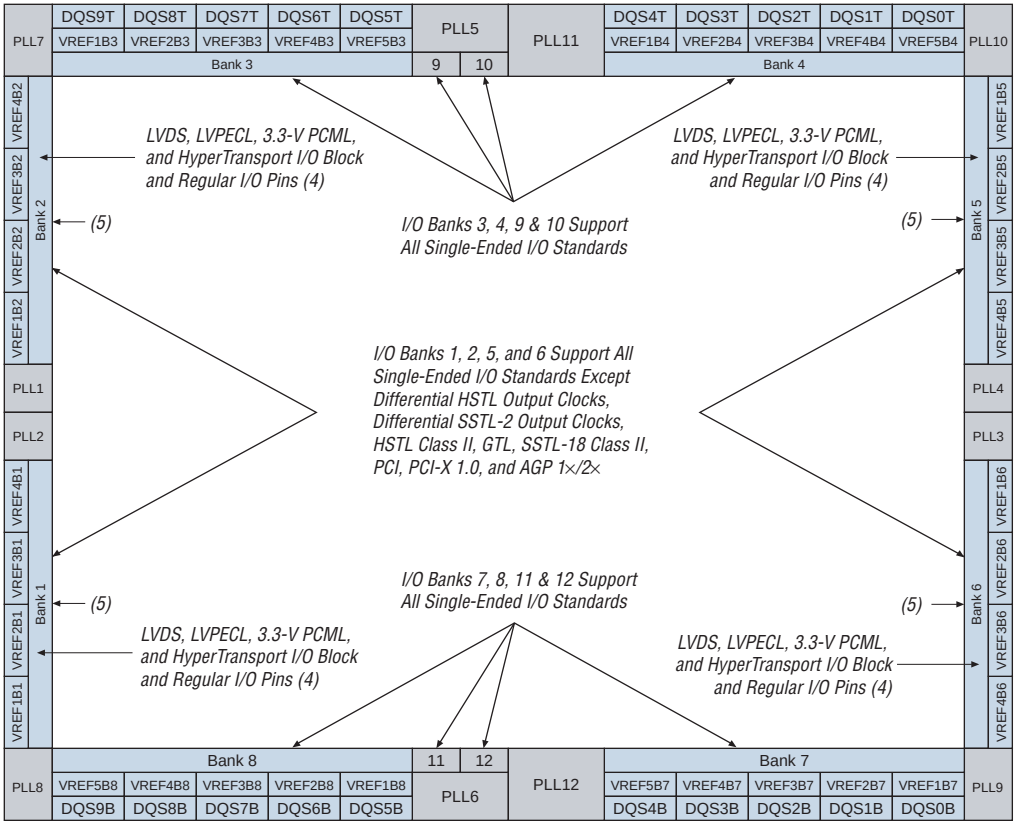
*Notes to Table 2–27:*

(1) See the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2* for $V_{REF}$ guidelines.
(2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.
(3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.
(4) This package has nine groups in I/O banks 3 and 4 and nine groups in I/O banks 7 and 8.
(5) These packages have three groups in I/O banks 3 and 4 and four groups in I/O banks 7 and 8.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Two separate single phase-shifting reference circuits are located on the top and bottom of the Stratix device. Each circuit is driven by a system reference clock through the `CLK` pins that is the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase-shift circuitry on the bottom of the device. The phase-shifting reference circuit on the top of the device controls the compensated delay elements for all 10 DQS pins located at the top of the device. The phase-shifting reference circuit on the bottom of the device controls the compensated delay elements for all 10 DQS pins located on the bottom of the device. All 10 delay elements (DQS signals) on either the top or bottom of the device

***Figure 2–70. Stratix I/O Banks*** *Notes (1), (2), (3)*




*Notes to Figure 2–70:*

(1) Figure 2–70 is a top view of the silicon die. This will correspond to a top-down view for non-flip-chip packages, but will be a reverse view for flip-chip packages.

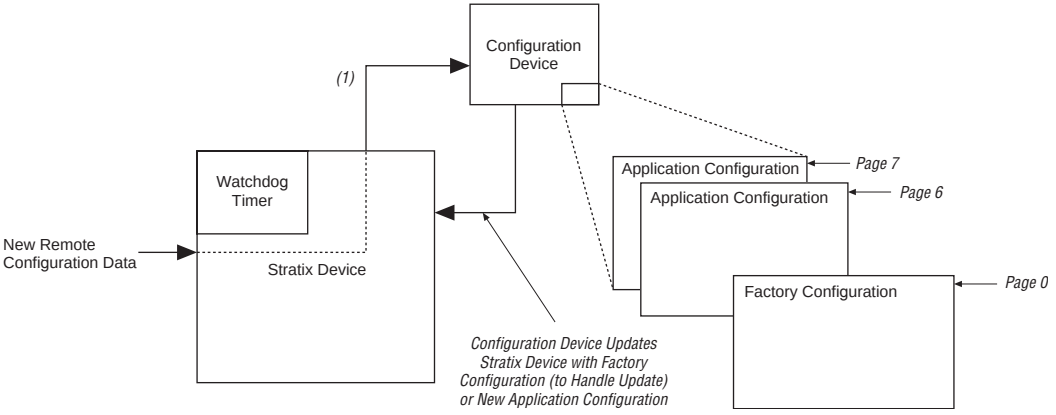
(2) Figure 2–70 is a graphic representation only. See the device pin-outs on the web (**www.altera.com**) and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL Class I and II, GTL, SSTL-18 Class II, PCI, PCI-X 1.0, and AGP 1× /2×.

(5) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix and Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2*.

*Figure 3–2. Stratix Device Remote Update*




*Note to Figure 3–2:*

(1) When the Stratix device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

For Stratix, the CRC is computed by the Quartus II software and downloaded into the device as a part of the configuration bit stream. The CRC_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

### Custom-Built Circuitry

Dedicated circuitry is built in the Stratix devices to perform error detection automatically. You can use the built-in dedicated circuitry for error detection using CRC feature in Stratix devices, eliminating the need for external logic. This circuitry will perform error detection automatically when enabled. This error detection circuitry in Stratix devices constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a re-configuration cycle. Select the desired time between checks by adjusting a built-in clock divider.

### Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 100 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, see *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

## Temperature Sensing Diode

Stratix devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the junction temperature of the Stratix device and can be used for intelligent power management.

The diode requires two pins (tempdiodep and tempdioden) on the Stratix device to connect to the external temperature-sensing device, as shown in Figure 3–5. The temperature sensing diode is a passive element and therefore can be used before the Stratix device is powered.

*Table 4–47. DSP Block Internal Timing Microparameters (Part 2 of 2)*

| Symbol | -5 | | -6 | | -7 | | -8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PIPE2OUTREG2ADD}$ | | 2,002 | | 2,203 | | 2,533 | | 2,980 | ps |
| $t_{PIPE2OUTREG4ADD}$ | | 2,899 | | 3,189 | | 3,667 | | 4,314 | ps |
| $t_{PD9}$ | | 3,709 | | 4,081 | | 4,692 | | 5,520 | ps |
| $t_{PD18}$ | | 4,795 | | 5,275 | | 6,065 | | 7,135 | ps |
| $t_{PD36}$ | | 7,495 | | 8,245 | | 9,481 | | 11,154 | ps |
| $t_{CLR}$ | 450 | | 500 | | 575 | | 676 | | ps |
| $t_{CLKHL}$ | 1,350 | | 1,500 | | 1,724 | | 2,029 | | ps |

*Table 4–48. M512 Block Internal Timing Microparameters*

| Symbol | -5 | | -6 | | -7 | | -8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{M512RC}$ | | 3,340 | | 3,816 | | 4,387 | | 5,162 | ps |
| $t_{M512WC}$ | | 3,138 | | 3,590 | | 4,128 | | 4,860 | ps |
| $t_{M512WERESU}$ | 110 | | 123 | | 141 | | 166 | | ps |
| $t_{M512WEREH}$ | 34 | | 38 | | 43 | | 51 | | ps |
| $t_{M512CLKENSU}$ | 215 | | 215 | | 247 | | 290 | | ps |
| $t_{M512CLKENH}$ | –70 | | –70 | | –81 | | –95 | | ps |
| $t_{M512DATASU}$ | 110 | | 123 | | 141 | | 166 | | ps |
| $t_{M512DATAH}$ | 34 | | 38 | | 43 | | 51 | | ps |
| $t_{M512WADDRSU}$ | 110 | | 123 | | 141 | | 166 | | ps |
| $t_{M512WADDRH}$ | 34 | | 38 | | 43 | | 51 | | ps |
| $t_{M512RADDRSU}$ | 110 | | 123 | | 141 | | 166 | | ps |
| $t_{M512RADDRH}$ | 34 | | 38 | | 43 | | 51 | | ps |
| $t_{M512DATACO1}$ | | 424 | | 472 | | 541 | | 637 | ps |
| $t_{M512DATACO2}$ | | 3,366 | | 3,846 | | 4,421 | | 5,203 | ps |
| $t_{M512CLKHL}$ | 1,000 | | 1,111 | | 1,190 | | 1,400 | | ps |
| $t_{M512CLR}$ | 170 | | 189 | | 217 | | 255 | | ps |

| *Table 4–53. Stratix Regional Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{XZPLL}$ | Synchronous IOE output enable register to output pin disable delay using regional clock fed by Enhanced PLL with default phase setting |
| $t_{ZXPLL}$ | Synchronous IOE output enable register to output pin enable delay using regional clock fed by Enhanced PLL with default phase setting |

*Notes to Table 4–53:*
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column and row IOE pins. You should use the Quartus II software to verify the external timing for any pin.

Table 4–54 shows the external I/O timing parameters when using global clock networks.

| *Table 4–54. Stratix Global Clock External I/O Timing Parameters Notes (1), (2)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{INSU}$ | Setup time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin |
| $t_{INH}$ | Hold time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin |
| $t_{OUTCO}$ | Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by `CLK` pin |
| $t_{INSUPLL}$ | Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting |
| $t_{INHPLL}$ | Hold time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting |
| $t_{OUTCOPLL}$ | Clock-to-output delay output or bidirectional pin using IOE output register with global clock Enhanced PLL with default phase setting |
| $t_{XZPLL}$ | Synchronous IOE output enable register to output pin disable delay using global clock fed by Enhanced PLL with default phase setting |
| $t_{ZXPLL}$ | Synchronous IOE output enable register to output pin enable delay using global clock fed by Enhanced PLL with default phase setting |

*Notes to Table 4–54:*
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column and row IOE pins. You should use the Quartus II software to verify the external timing for any pin.

*Table 4–71. EP1S25 External I/O Timing on Row Pins Using Regional Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.793 | | 1.927 | | 2.182 | | 2.542 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.759 | 5.457 | 2.759 | 5.835 | 2.759 | 6.346 | 2.759 | 7.024 | ns |
| $t_{XZ}$ | 2.786 | 5.511 | 2.786 | 5.891 | 2.786 | 6.414 | 2.786 | 7.106 | ns |
| $t_{ZX}$ | 2.786 | 5.511 | 2.786 | 5.891 | 2.786 | 6.414 | 2.786 | 7.106 | ns |
| $t_{INSUPLL}$ | 1.169 | | 1.221 | | 1.373 | | 1.600 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.375 | 2.861 | 1.375 | 2.999 | 1.375 | 3.082 | 1.375 | 3.174 | ns |
| $t_{XZPLL}$ | 1.402 | 2.915 | 1.402 | 3.055 | 1.402 | 3.150 | 1.402 | 3.256 | ns |
| $t_{ZXPLL}$ | 1.402 | 2.915 | 1.402 | 3.055 | 1.402 | 3.150 | 1.402 | 3.256 | ns |

*Table 4–72. EP1S25 External I/O Timing on Row Pins Using Global Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 1.665 | | 1.779 | | 2.012 | | 2.372 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.834 | 5.585 | 2.834 | 5.983 | 2.834 | 6.516 | 2.834 | 7.194 | ns |
| $t_{XZ}$ | 2.861 | 5.639 | 2.861 | 6.039 | 2.861 | 6.584 | 2.861 | 7.276 | ns |
| $t_{ZX}$ | 2.861 | 5.639 | 2.861 | 6.039 | 2.861 | 6.584 | 2.861 | 7.276 | ns |
| $t_{INSUPLL}$ | 1.538 | | 1.606 | | 1.816 | | 2.121 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.164 | 2.492 | 1.164 | 2.614 | 1.164 | 2.639 | 1.164 | 2.653 | ns |
| $t_{XZPLL}$ | 1.191 | 2.546 | 1.191 | 2.670 | 1.191 | 2.707 | 1.191 | 2.735 | ns |
| $t_{ZXPLL}$ | 1.191 | 2.546 | 1.191 | 2.670 | 1.191 | 2.707 | 1.191 | 2.735 | ns |

*Table 4–83. EP1S40 External I/O Timing on Row Pins Using Regional Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.349 | | 2.526 | | 2.898 | | 2.952 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.725 | 5.381 | 2.725 | 5.784 | 2.725 | 6.290 | 2.725 | 7.426 | ns |
| $t_{XZ}$ | 2.752 | 5.435 | 2.752 | 5.840 | 2.752 | 6.358 | 2.936 | 7.508 | ns |
| $t_{ZX}$ | 2.752 | 5.435 | 2.752 | 5.840 | 2.752 | 6.358 | 2.936 | 7.508 | ns |
| $t_{INSUPLL}$ | 1.328 | | 1.322 | | 1.605 | | 1.883 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.169 | 2.502 | 1.169 | 2.698 | 1.169 | 2.650 | 1.169 | 2.691 | ns |
| $t_{XZPLL}$ | 1.196 | 2.556 | 1.196 | 2.754 | 1.196 | 2.718 | 1.196 | 2.773 | ns |
| $t_{ZXPLL}$ | 1.196 | 2.556 | 1.196 | 2.754 | 1.196 | 2.718 | 1.196 | 2.773 | ns |

*Table 4–84. EP1S40 External I/O Timing on Row Pins Using Global Clock Networks*

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.020 | | 2.171 | | 2.491 | | 2.898 | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCO}$ | 2.912 | 5.710 | 2.912 | 6.139 | 2.912 | 6.697 | 2.931 | 7.480 | ns |
| $t_{XZ}$ | 2.939 | 5.764 | 2.939 | 6.195 | 2.939 | 6.765 | 2.958 | 7.562 | ns |
| $t_{ZX}$ | 2.939 | 5.764 | 2.939 | 6.195 | 2.939 | 6.765 | 2.958 | 7.562 | ns |
| $t_{INSUPLL}$ | 1.370 | | 1.368 | | 1.654 | | 1.881 | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.144 | 2.460 | 1.144 | 2.652 | 1.144 | 2.601 | 1.170 | 2.693 | ns |
| $t_{XZPLL}$ | 1.171 | 2.514 | 1.171 | 2.708 | 1.171 | 2.669 | 1.197 | 2.775 | ns |
| $t_{ZXPLL}$ | 1.171 | 2.514 | 1.171 | 2.708 | 1.171 | 2.669 | 1.197 | 2.775 | ns |

*Table 4–87. EP1S60 External I/O Timing on Column Pins Using Global Clock Networks* Note (1)

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.000 | | 2.152 | | 2.441 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 3.051 | 5.900 | 3.051 | 6.340 | 3.051 | 6.977 | NA | NA | ns |
| $t_{XZ}$ | 2.991 | 5.774 | 2.991 | 6.208 | 2.991 | 6.853 | NA | NA | ns |
| $t_{ZX}$ | 2.991 | 5.774 | 2.991 | 6.208 | 2.991 | 6.853 | NA | NA | ns |
| $t_{INSUPLL}$ | 1.315 | | 1.362 | | 1.543 | | NA | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCOPLL}$ | 1.029 | 2.196 | 1.029 | 2.303 | 1.029 | 2.323 | NA | NA | ns |
| $t_{XZPLL}$ | 0.969 | 2.070 | 0.969 | 2.171 | 0.969 | 2.199 | NA | NA | ns |
| $t_{ZXPLL}$ | 0.969 | 2.070 | 0.969 | 2.171 | 0.969 | 2.199 | NA | NA | ns |

*Table 4–88. EP1S60 External I/O Timing on Row Pins Using Fast Regional Clock Networks* Note (1)

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.144 | | 3.393 | | 3.867 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 2.643 | 5.275 | 2.643 | 5.654 | 2.643 | 6.140 | NA | NA | ns |
| $t_{XZ}$ | 2.670 | 5.329 | 2.670 | 5.710 | 2.670 | 6.208 | NA | NA | ns |
| $t_{ZX}$ | 2.670 | 5.329 | 2.670 | 5.710 | 2.670 | 6.208 | NA | NA | ns |

*Table 4–93. EP1S80 External I/O Timing on Column Pins Using Global Clock Networks* Note (1)

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 0.884 | | 0.976 | | 1.118 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 3.267 | 6.274 | 3.267 | 6.721 | 3.267 | 7.415 | NA | NA | ns |
| $t_{XZ}$ | 3.207 | 6.148 | 3.207 | 6.589 | 3.207 | 7.291 | NA | NA | ns |
| $t_{ZX}$ | 3.207 | 6.148 | 3.207 | 6.589 | 3.207 | 7.291 | NA | NA | ns |
| $t_{INSUPLL}$ | 0.506 | | 0.656 | | 0.838 | | NA | | ns |
| $t_{INHPLL}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCOPLL}$ | 1.635 | 2.805 | 1.635 | 2.809 | 1.635 | 2.828 | NA | NA | ns |
| $t_{XZPLL}$ | 1.575 | 2.679 | 1.575 | 2.677 | 1.575 | 2.704 | NA | NA | ns |
| $t_{ZXPLL}$ | 1.575 | 2.679 | 1.575 | 2.677 | 1.575 | 2.704 | NA | NA | ns |

*Table 4–94. EP1S80 External I/O Timing on Row Pins Using Fast Regional Clock Networks* Note (1)

| Parameter | -5 Speed Grade | | -6 Speed Grade | | -7 Speed Grade | | -8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.792 | | 2.993 | | 3.386 | | NA | | ns |
| $t_{INH}$ | 0.000 | | 0.000 | | 0.000 | | NA | | ns |
| $t_{OUTCO}$ | 2.619 | 5.235 | 2.619 | 5.609 | 2.619 | 6.086 | NA | NA | ns |
| $t_{XZ}$ | 2.646 | 5.289 | 2.646 | 5.665 | 2.646 | 6.154 | NA | NA | ns |
| $t_{ZX}$ | 2.646 | 5.289 | 2.646 | 5.665 | 2.646 | 6.154 | NA | NA | ns |

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