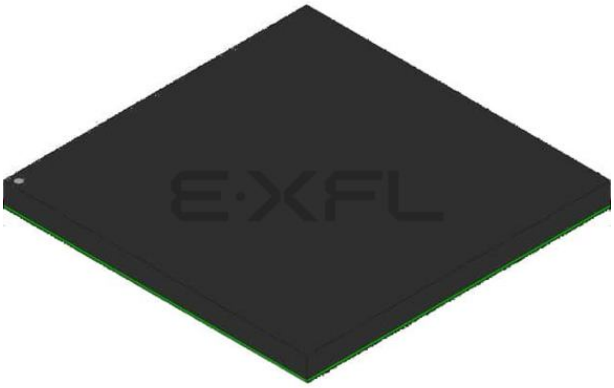

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Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	683
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	956-BBGA, FCBGA
Supplier Device Package	956-BGA (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1s80b956c6

Table 2–11. M-RAM Combined Byte Selection for ×144 Mode Notes (1), (2)

byteena[15..0]	datain ×144
[0] = 1	[8..0]
[1] = 1	[17..9]
[2] = 1	[26..18]
[3] = 1	[35..27]
[4] = 1	[44..36]
[5] = 1	[53..45]
[6] = 1	[62..54]
[7] = 1	[71..63]
[8] = 1	[80..72]
[9] = 1	[89..81]
[10] = 1	[98..90]
[11] = 1	[107..99]
[12] = 1	[116..108]
[13] = 1	[125..117]
[14] = 1	[134..126]
[15] = 1	[143..135]

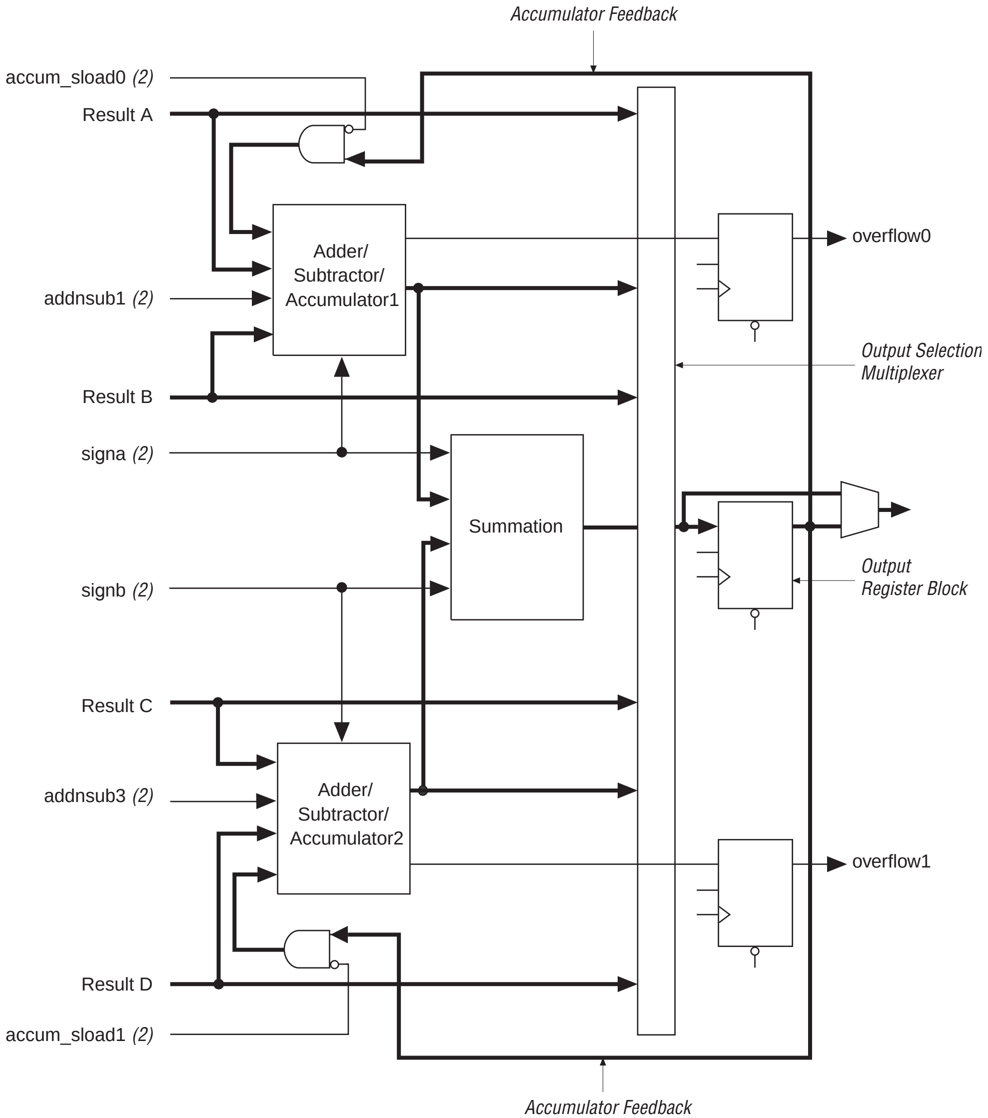
Notes to Tables 2–10 and 2–11:

(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16, ×32, ×64, and ×128 modes.

Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. All input registers—`renwe`, `datain`, address, and byte enable registers—are clocked together from either of the two clocks feeding the block. The output register can be bypassed. The eight `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, clr_b, `clocken_a`, and `clocken_b` signals as shown in Figure 2–19.

Figure 2–34. Adder/Output Blocks Note (1)



Notes to Figure 2–34:

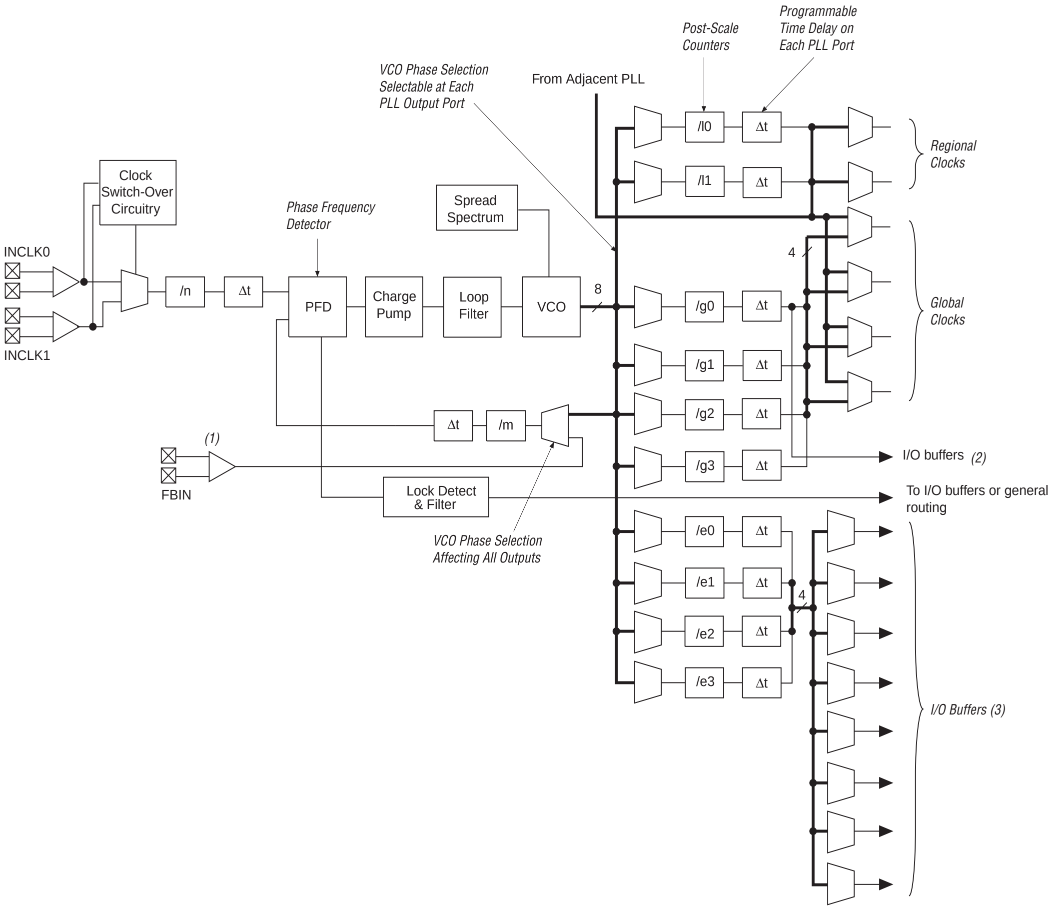
(1) Adder/output block shown in Figure 2–34 is in 18 × 18-bit mode. In 9 × 9-bit mode, there are four adder/subtractor blocks and two summation blocks.

(2) These signals are either not registered, registered once, or registered twice to match the data path pipeline.

Enhanced PLLs

Stratix devices contain up to four enhanced PLLs with advanced clock management features. Figure 2–52 shows a diagram of the enhanced PLL.

Figure 2–52. Stratix Enhanced PLL



Notes to Figure 2–52:

(1) External feedback is available in PLLs 5 and 6.
(2) This single-ended external output is available from the *g*0 counter for PLLs 11 and 12.
(3) These four counters and external outputs are available in PLLs 5 and 6.
(4) This connection is only available on EP1S40 and larger Stratix devices. For example, PLLs 5 and 11 are adjacent and PLLs 6 and 12 are adjacent. The EP1S40 device in the 780-pin FineLine BGA package does not support PLLs 11 and 12.

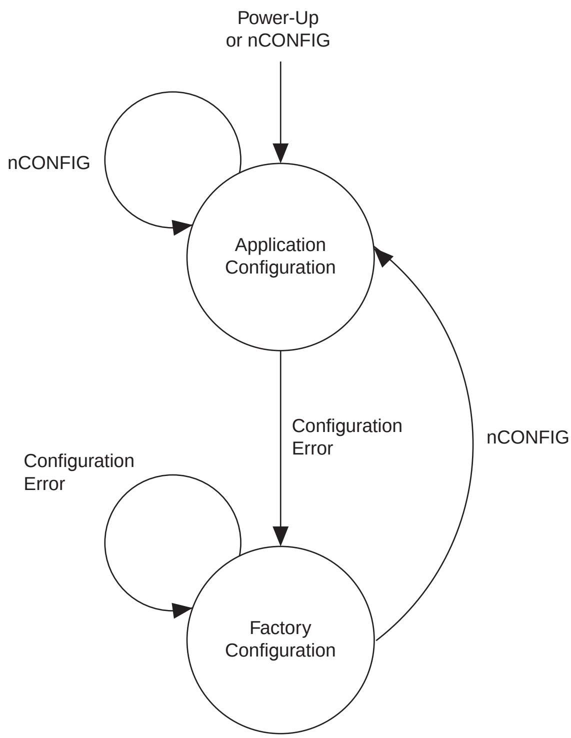
For more information on I/O standards supported by Stratix devices, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook, Volume 2*.

Stratix devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in Figure 2–70. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in Table 2–31 except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. Table 2–32 shows I/O standard support for each I/O bank.

Local Update Mode

Local update mode is a simplified version of the remote update. This feature is intended for simple systems that need to load a single application configuration immediately upon power up without loading the factory configuration first. Local update designs have only one application configuration to load, so it does not require a factory configuration to determine which application configuration to use. Figure 3–4 shows the transition diagram for local update mode.

Figure 3–4. Local Update Transition Diagram



Stratix Automated Single Event Upset (SEU) Detection

Stratix devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. FPGA devices that operate at high elevations or in close proximity to earth's North or South Pole require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

Table 4–22. SSTL-3 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.4$	V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA *(3)*	$V_{TT} + 0.6$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA *(3)*			$V_{TT} - 0.6$	V

Table 4–23. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
$V_{IH(DC)}$	High-level DC input voltage		$V_{REF} + 0.2$		$V_{CCIO} + 0.3$	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		$V_{REF} - 0.2$	V
$V_{IH(AC)}$	High-level AC input voltage		$V_{REF} + 0.4$			V
$V_{IL(AC)}$	Low-level AC input voltage				$V_{REF} - 0.4$	V
V_{OH}	High-level output voltage	$I_{OH} = -16$ mA *(3)*	$V_{TT} + 0.8$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16$ mA *(3)*			$V_{TT} - 0.8$	V

Table 4–24. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage *(4)*		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage *(4)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = -0.5$ mA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	$I_{OUT} = 1.5$ mA			$0.1 \times V_{CCIO}$	V

Table 4–25. 3.3-V AGP 1× Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(4)*		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage *(4)*				$0.3 \times V_{CCIO}$	V

Table 4–28. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA *(3)*			0.4	V

Table 4–29. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -16$ mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16$ mA *(3)*			0.4	V

Table 4–30. 1.5-V Differential HSTL Class I & Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 4–40. M512 Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{M512RC}	Synchronous read cycle time
t_{M512WC}	Synchronous write cycle time
$t_{M512WERESU}$	Write or read enable setup time before clock
$t_{M512WEREH}$	Write or read enable hold time after clock
$t_{M512CLKENSU}$	Clock enable setup time before clock
$t_{M512CLKENH}$	Clock enable hold time after clock
$t_{M512DATASU}$	Data setup time before clock
$t_{M512DATAH}$	Data hold time after clock
$t_{M512WADDRSU}$	Write address setup time before clock
$t_{M512WADDRH}$	Write address hold time after clock
$t_{M512RADDRSU}$	Read address setup time before clock
$t_{M512RADDRH}$	Read address hold time after clock
$t_{M512DATACO1}$	Clock-to-output delay when using output registers
$t_{M512DATACO2}$	Clock-to-output delay without output registers
$t_{M512CLKHL}$	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown in Table 4–36 on page 4–20 and as reported by the timing analyzer in the Quartus II software.
$t_{M512CLR}$	Minimum clear pulse width

Table 4–41. M4K Block Internal Timing Microparameter Descriptions (Part 1 of 2)

Symbol	Parameter
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KCLKENSU}$	Clock enable setup time before clock
$t_{M4KCLKENH}$	Clock enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock

Table 4–42. M-RAM Block Internal Timing Microparameter Descriptions (Part 2 of 2)	
Symbol	**Parameter**
$t_{MRAMDATABH}$	B port hold time after clock
$t_{MRAMADDRBSU}$	B port address setup time before clock
$t_{MRAMADDRBH}$	B port address hold time after clock
$t_{MRAMDATACO1}$	Clock-to-output delay when using output registers
$t_{MRAMDATACO2}$	Clock-to-output delay without output registers
$t_{MRAMCLKHL}$	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown in Table 4–36 on page 4–20 and as reported by the timing analyzer in the Quartus II software.
$t_{MRAMCLR}$	Minimum clear pulse width.

Table 4–77. EP1S30 External I/O Timing on Row Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.322		2.467		2.828		3.342		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.731	5.408	2.731	5.843	2.731	6.360	2.731	7.036	ns
t_{XZ}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
t_{ZX}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
$t_{INSUPLL}$	1.291		1.283		1.469		1.832		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.192	2.539	1.192	2.737	1.192	2.786	1.192	2.742	ns
t_{XZPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns
t_{ZXPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns

Table 4–78. EP1S30 External I/O Timing on Row Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.995		2.089		2.398		2.830		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.917	5.735	2.917	6.221	2.917	6.790	2.917	7.548	ns
t_{XZ}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
t_{ZX}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
$t_{INSUPLL}$	1.337		1.312		1.508		1.902		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.164	2.493	1.164	2.708	1.164	2.747	1.164	2.672	ns
t_{XZPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns
t_{ZXPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns

Tables 4–79 through 4–84 show the external timing parameters on column and row pins for EP1S40 devices.

Table 4–79. EP1S40 External I/O Timing on Column Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.696		2.907		3.290		2.899		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.506	5.015	2.506	5.348	2.506	5.809	2.698	7.286	ns
t_{XZ}	2.446	4.889	2.446	5.216	2.446	5.685	2.638	7.171	ns
t_{ZX}	2.446	4.889	2.446	5.216	2.446	5.685	2.638	7.171	ns

Table 4–80. EP1S40 External I/O Timing on Column Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.413		2.581		2.914		2.938		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.668	5.254	2.668	5.628	2.668	6.132	2.869	7.307	ns
t_{XZ}	2.608	5.128	2.608	5.496	2.608	6.008	2.809	7.192	ns
t_{ZX}	2.608	5.128	2.608	5.496	2.608	6.008	2.809	7.192	ns
$t_{INSUPLL}$	1.385		1.376		1.609		1.837		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.117	2.382	1.117	2.552	1.117	2.504	1.117	2.542	ns
t_{XZPLL}	1.057	2.256	1,057	2.420	1.057	2.380	1.057	2.427	ns
t_{ZXPLL}	1.057	2.256	1,057	2.420	1.057	2.380	1.057	2.427	ns

Table 4–89. EP1S60 External I/O Timing on Row Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.775		2.990		3.407		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.867	5.644	2.867	6.057	2.867	6.600	NA	NA	ns
t_{XZ}	2.894	5.698	2.894	6.113	2.894	6.668	NA	NA	ns
t_{ZX}	2.894	5.698	2.894	6.113	2.894	6.668	NA	NA	ns
$t_{INSUPLL}$	1.523		1.577		1.791		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.174	2.507	1.174	2.643	1.174	2.664	NA	NA	ns
t_{XZPLL}	1.201	2.561	1.201	2.699	1.201	2.732	NA	NA	ns
t_{ZXPLL}	1.201	2.561	1.201	2.699	1.201	2.732	NA	NA	ns

Table 4–90. EP1S60 External I/O Timing on Row Pins Using Global Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.232		2.393		2.721		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.182	6.187	3.182	6.654	3.182	7.286	NA	NA	ns
t_{XZ}	3.209	6.241	3.209	6.710	3.209	7.354	NA	NA	ns
t_{ZX}	3.209	6.241	3.209	6.710	3.209	7.354	NA	NA	ns
$t_{INSUPLL}$	1.651		1.612		1.833		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.154	2.469	1.154	2.608	1.154	2.622	NA	NA	ns
t_{XZPLL}	1.181	2.523	1.181	2.664	1.181	2.690	NA	NA	ns
t_{ZXPLL}	1.181	2.523	1.181	2.664	1.181	2.690	NA	NA	ns

Note to Tables 4–85 to 4–90:

(1) Only EP1S25, EP1S30, and EP1S40 devices have the -8 speed grade.

Table 4–104. Stratix I/O Standard Row Pin Input Delay Adders									
Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0		0	ps
3.3-V LVTTL		0		0		0		0	ps
2.5-V LVTTL		21		22		25		29	ps
1.8-V LVTTL		181		190		218		257	ps
1.5-V LVTTL		300		315		362		426	ps
GTL+		–152		–160		–184		–216	ps
CTT		–168		–177		–203		–239	ps
SSTL-3 Class I		–193		–203		–234		–275	ps
SSTL-3 Class II		–193		–203		–234		–275	ps
SSTL-2 Class I		–262		–276		–317		–373	ps
SSTL-2 Class II		–262		–276		–317		–373	ps
SSTL-18 Class I		–105		–111		–127		–150	ps
SSTL-18 Class II		0		0		0		0	ps
1.5-V HSTL Class I		–151		–159		–183		–215	ps
1.8-V HSTL Class I		–126		–133		–153		–179	ps
LVDS		–149		–157		–180		–212	ps
LVPECL		–149		–157		–180		–212	ps
3.3-V PCML		–65		–69		–79		–93	ps
HyperTransport		77		–81		–93		–110	ps

Table 4–106. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2)										
Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
1.5-V LVTTL	2 mA		5,460		5,733		5,733		5,733	ps
	4 mA		2,690		2,824		2,824		2,824	ps
	8 mA		1,398		1,468		1,468		1,468	ps
GTL+			6		6		6		6	ps
CTT			845		887		887		887	ps
SSTL-3 Class I			638		670		670		670	ps
SSTL-3 Class II			144		151		151		151	ps
SSTL-2 Class I			604		634		634		634	ps
SSTL-2 Class II			211		221		221		221	ps
SSTL-18 Class I			955		1,002		1,002		1,002	ps
1.5-V HSTL Class I			733		769		769		769	ps
1.8-V HSTL Class I			372		390		390		390	ps
LVDS			–196		–206		–206		–206	ps
LVPECL			–148		–156		–156		–156	ps
PCML			–147		–155		–155		–155	ps
HyperTransport technology			–93		–98		–98		–98	ps

Note to Table 4–103 through 4–106:
(1) These parameters are only available on row I/O pins.

Table 4–107. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2)										
Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,822		1,913		1,913		1,913	ps
	4 mA		684		718		718		718	ps
	8 mA		233		245		245		245	ps
	12 mA		1		1		1		1	ps
	24 mA		–608		–638		–638		–638	ps

Table 4–121. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	400	350	300	300	MHz
2.5 V	400	350	300	300	MHz
1.8 V	400	350	300	300	MHz
1.5 V	350	300	300	300	MHz
LVCMOS	400	350	300	300	MHz
GTL	200	167	125	125	MHz
GTL+	200	167	125	125	MHz
SSTL-3 Class I	167	150	133	133	MHz
SSTL-3 Class II	167	150	133	133	MHz
SSTL-2 Class I	150	133	133	133	MHz
SSTL-2 Class II	150	133	133	133	MHz
SSTL-18 Class I	150	133	133	133	MHz
SSTL-18 Class II	150	133	133	133	MHz
1.5-V HSTL Class I	250	225	200	200	MHz
1.5-V HSTL Class II	225	225	200	200	MHz
1.8-V HSTL Class I	250	225	200	200	MHz
1.8-V HSTL Class II	225	225	200	200	MHz
3.3-V PCI	250	225	200	200	MHz
3.3-V PCI-X 1.0	225	225	200	200	MHz
Compact PCI	400	350	300	300	MHz
AGP 1×	400	350	300	300	MHz
AGP 2×	400	350	300	300	MHz
CTT	300	250	200	200	MHz
LVPECL *(2)*	717	717	500	500	MHz
PCML *(2)*	420	420	420	420	MHz
LVDS *(2)*	717	717	500	500	MHz
HyperTransport technology *(2)*	420	420	420	420	MHz

Tables 4–125 and 4–126 show the high-speed I/O timing for Stratix devices.

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 1 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (Clock frequency) (LVDS, LVPECL, HyperTransport technology) $f_{HSCLK} = f_{HSDR}$ / W	*W* = 4 to 30 (Serdes used)	10		210	10		210	10		156	10		115.5	MHz
	W = 2 (Serdes bypass)	50		231	50		231	50		231	50		231	MHz
	W = 2 (Serdes used)	150		420	150		420	150		312	150		231	MHz
	W = 1 (Serdes bypass)	100		462	100		462	100		462	100		462	MHz
	W = 1 (Serdes used)	300		717	300		717	300		624	300		462	MHz
f_{HSDR} Device operation (LVDS, LVPECL, HyperTransport technology)	*J* = 10	300		840	300		840	300		640	300		462	Mbps
	J = 8	300		840	300		840	300		640	300		462	Mbps
	J = 7	300		840	300		840	300		640	300		462	Mbps
	J = 4	300		840	300		840	300		640	300		462	Mbps
	J = 2	100		462	100		462	100		640	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		462	100		462	100		640	100		462	Mbps

Table 4–126. High-Speed I/O Specifications for Wire-Bond Packages (Part 1 of 2)

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (Clock frequency) (LVDS,LVPECL, HyperTransport technology) $f_{HSCLK} = f_{HSDR} / W$	*W* = 4 to 30 (Serdes used)	10		156	10		115.5	10		115.5	MHz
	W = 2 (Serdes bypass)	50		231	50		231	50		231	MHz
	W = 2 (Serdes used)	150		312	150		231	150		231	MHz
	W = 1 (Serdes bypass)	100		311	100		270	100		270	MHz
	W = 1 (Serdes used)	300		624	300		462	300		462	MHz
f_{HSDR} Device operation, (LVDS,LVPECL, HyperTransport technology)	J = 10	300		624	300		462	300		462	Mbps
	J = 8	300		624	300		462	300		462	Mbps
	J = 7	300		624	300		462	300		462	Mbps
	J = 4	300		624	300		462	300		462	Mbps
	J = 2	100		462	100		462	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		311	100		270	100		270	Mbps
f_{HSCLK} (Clock frequency) (PCML) $f_{HSCLK} = f_{HSDR} / W$	*W* = 4 to 30 (Serdes used)	10		77.75							MHz
	W = 2 (Serdes bypass)	50		150	50		77.5	50		77.5	MHz
	W = 2 (Serdes used)	150		155.5							MHz
	W = 1 (Serdes bypass)	100		200	100		155	100		155	MHz
	W = 1 (Serdes used)	300		311							MHz
Device operation, f_{HSDR} (PCML)	J = 10	300		311							Mbps
	J = 8	300		311							Mbps
	J = 7	300		311							Mbps
	J = 4	300		311							Mbps
	J = 2	100		300	100		155	100		155	Mbps
	J = 1	100		200	100		155	100		155	Mbps
TCCS	All			400			400			400	ps

Table 4–127. Enhanced PLL Specifications for -5 Speed Grades (Part 2 of 2)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	30		150	kHz
% spread	Percentage spread for spread spectrum frequency *(10)*	0.4	0.5	0.6	%
t_{ARESET}	Minimum pulse width on `areset` signal	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandataout` goes high.	500			ns

Table 4–128. Enhanced PLL Specifications for -6 Speed Grades (Part 1 of 2)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_{IN}	Input clock frequency	3 *(1)*, *(2)*		650	MHz
f_{INPFD}	Input frequency to PFD	3		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			±200 *(3)*	ps
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(3)*	ps
t_{FCOMP}	External feedback clock compensation time *(4)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		450	MHz
f_{OUT_EXT}	Output frequency for external clock *(3)*	0.3		500	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(6)*			±100 ps for >200-MHz `outclk` ±20 mUI for <200-MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	

Table 4–130. Enhanced PLL Specifications for -8 Speed Grade (Part 2 of 3)					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(3)*	ps
t_{FCOMP}	External feedback clock compensation time *(4)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		357	MHz
f_{OUT_EXT}	Output frequency for external clock *(3)*	0.3		369	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(6)*			±100 ps for >200-MHz `outclk` ±20 mUI for <200-MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			289/$f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			193/$f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(5)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(7) (11)*	*(9)*		100	µs
t_{LOCK}	Time required to lock from end of device configuration *(11)*	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		600 *(8)*	MHz

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