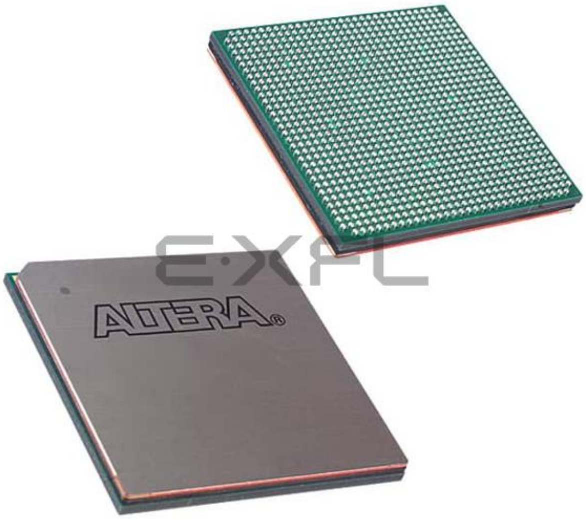

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	7904
Number of Logic Elements/Cells	79040
Total RAM Bits	7427520
Number of I/O	773
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1s80f1020i7n

Chapter 3. Configuration & Testing

Chapter 4. DC & Switching Characteristics

Chapter	Date/Version	Changes Made
4	October 2003, v2.1	● Added -8 speed grade information. ● Updated performance information in Table 4–36. ● Updated timing information in Tables 4–55 through 4–96. ● Updated delay information in Tables 4–103 through 4–108. ● Updated programmable delay information in Tables 4–100 and 4–103.
	July 2003, v2.0	● Updated clock rates in Tables 4–114 through 4–123. ● Updated speed grade information in the introduction on page 4-1. ● Corrected figures 4-1 & 4-2 and Table 4-9 to reflect how VID and VOD are specified. ● Added note 6 to Table 4-32. ● Updated Stratix Performance Table 4-35. ● Updated EP1S60 and EP1S80 timing parameters in Tables 4-82 to 4-93. The Stratix timing models are final for all devices. ● Updated Stratix IOE programmable delay chains in Tables 4-100 to 4-101. ● Added single-ended I/O standard output pin delay adders for loading in Table 4-102. ● Added spec for FPLL[10..7]CLK pins in Tables 4-104 and 4-107. ● Updated high-speed I/O specification for J=2 in Tables 4-114 and 4-115. ● Updated EPLL specification and fast PLL specification in Tables 4-116 to 4-120.
5	September 2004, v2.1	● Updated reference to device pin-outs on page 5–1 to indicate that device pin-outs are no longer included in this manual and are now available on the Altera web site.
	April 2003, v1.0	● No new changes in Stratix Device Handbook v2.0.

1. Introduction

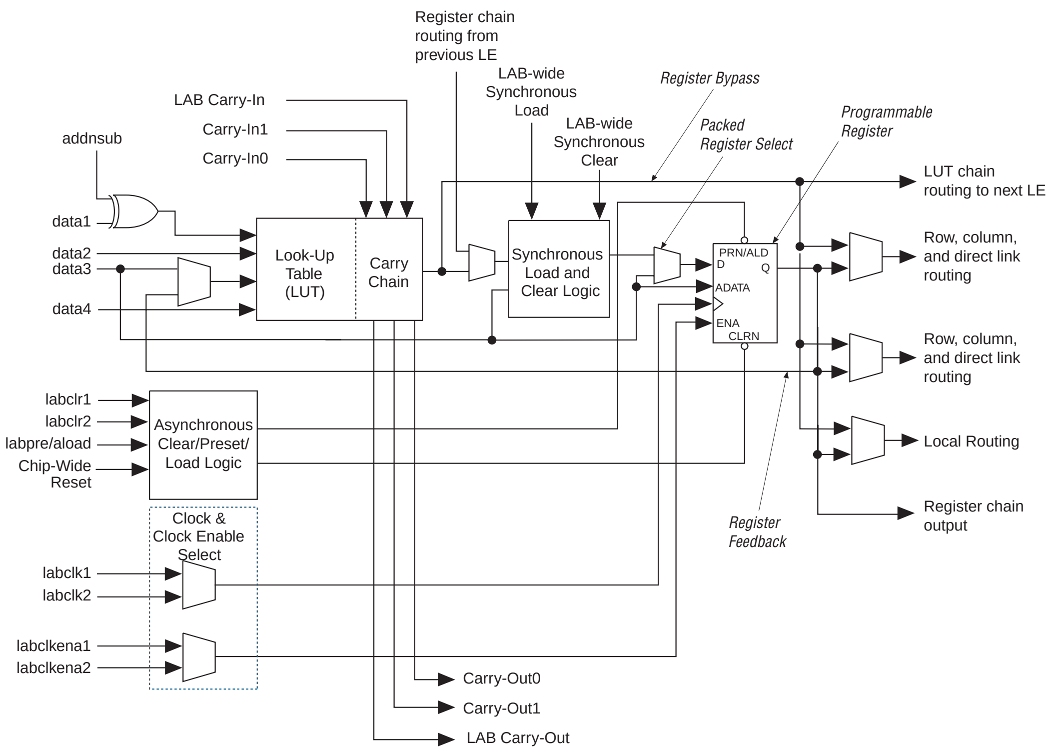
S51001-3.2

Introduction

The Stratix® family of FPGAs is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities of up to 79,040 logic elements (LEs) and up to 7.5 Mbits of RAM. Stratix devices offer up to 22 digital signal processing (DSP) blocks with up to 176 (9-bit × 9-bit) embedded multipliers, optimized for DSP applications that enable efficient implementation of high-performance filters and multipliers. Stratix devices support various I/O standards and also offer a complete clock management solution with its hierarchical clock structure with up to 420-MHz performance and up to 12 phase-locked loops (PLLs).

The following shows the main sections in the Stratix Device Family Data Sheet:

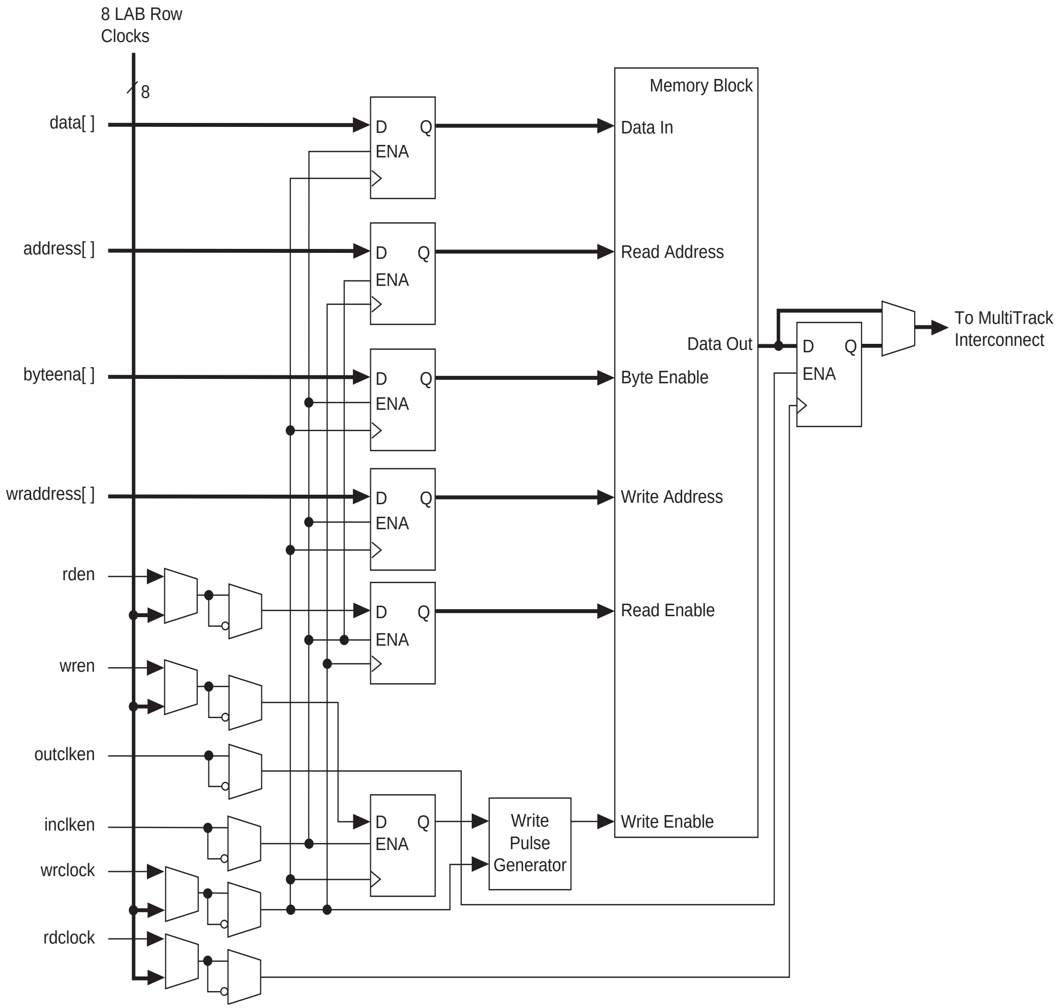
Figure 2–5. Stratix LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinatorial functions, the register is bypassed and the output of the LUT drives directly to the outputs of the LE.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated

Figure 2–26. Input/Output Clock Mode in Simple Dual-Port Mode Notes (1), (2)



Notes to Figure 2–26:

(1) All registers shown except the `rden` register have asynchronous clear ports.

(2) Violating the setup or hold time on the address registers could corrupt the memory contents. This applies to both read and write operations.

Table 2–13 shows the number of DSP blocks in each Stratix device.

Table 2–13. DSP Blocks in Stratix Devices *Notes (1), (2)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1S10	6	48	24	6
EP1S20	10	80	40	10
EP1S25	10	80	40	10
EP1S30	12	96	48	12
EP1S40	14	112	56	14
EP1S60	18	144	72	18
EP1S80	22	176	88	22

Notes to Table 2–13:

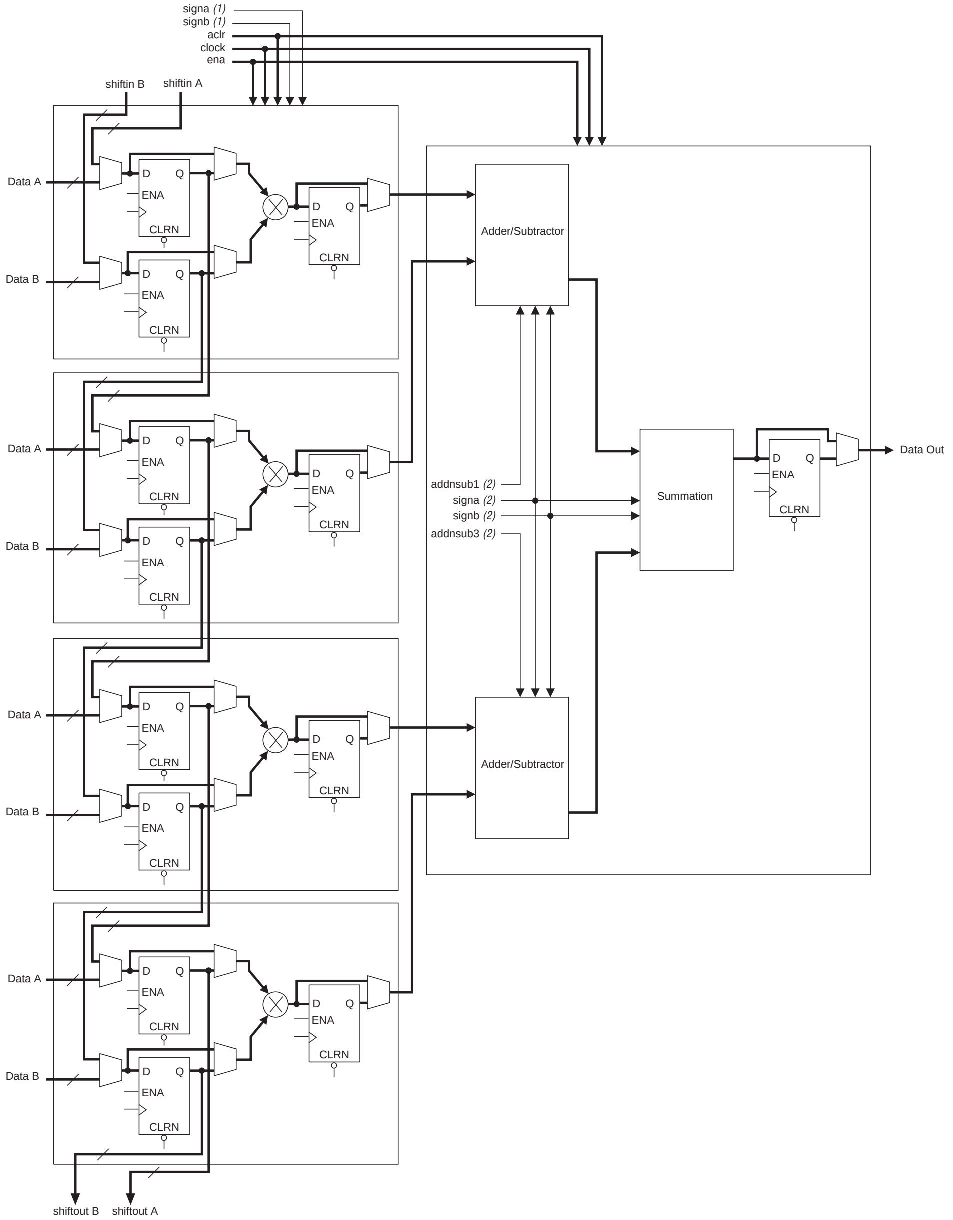
(1) Each device has either the number of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

(2) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP block multipliers can optionally feed an adder/subtractor or accumulator within the block depending on the configuration. This makes routing to LEs easier, saves LE routing resources, and increases performance, because all connections and blocks are within the DSP block. Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications.

Figure 2–30 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode. Figure 2–31 shows the 9 × 9-bit multiplier configuration of the DSP block.

Figure 2–39. Four-Multipliers Adder Mode



Notes to Figure 2–39:

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

Table 2–28 shows the possible settings for the I/O standards with drive strength control.

Table 2–28. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2
GTL/GTL+ 1.5-V HSTL Class I and II 1.8-V HSTL Class I and II SSTL-3 Class I and II SSTL-2 Class I and II SSTL-18 Class I and II	Support max and min strength

Notes to Table 2–28:
(1) This is the Quartus II software default current setting.
(2) I/O banks 1, 2, 5, and 6 do not support this setting.

Quartus II software version 4.2 and later will report current strength as "PCI Compliant" for 3.3-V PCI, 3.3-V PCI-X 1.0, and Compact PCI I/O standards.

Stratix devices support series on-chip termination (OCT) using programmable drive strength. For more information, contact your Altera Support Representative.

Open-Drain Output

Stratix devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Slew-Rate Control

The output buffer for each Stratix device I/O pin has a programmable output slew-rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each

Table 2–32 shows I/O standard support for each I/O bank.

Table 2–32. I/O Support by Bank (Part 1 of 2)

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
LVTTL	✓	✓	✓
LVCMOS	✓	✓	✓
2.5 V	✓	✓	✓
1.8 V	✓	✓	✓
1.5 V	✓	✓	✓
3.3-V PCI	✓		✓
3.3-V PCI-X 1.0	✓		✓
LVPECL		✓	✓
3.3-V PCML		✓	✓
LVDS		✓	✓
HyperTransport technology		✓	✓
Differential HSTL (clock inputs)	✓	✓	
Differential HSTL (clock outputs)			✓
Differential SSTL (clock outputs)			✓
3.3-V GTL	✓		✓
3.3-V GTL+	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓
1.5-V HSTL Class II	✓		✓
1.8-V HSTL Class I	✓	✓	✓
1.8-V HSTL Class II	✓		✓
SSTL-18 Class I	✓	✓	✓
SSTL-18 Class II	✓		✓
SSTL-2 Class I	✓	✓	✓
SSTL-2 Class II	✓	✓	✓
SSTL-3 Class I	✓	✓	✓

Table 2–32. I/O Support by Bank (Part 2 of 2)			
I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
SSTL-3 Class II	✓	✓	✓
AGP (1× and 2×)	✓		✓
CTT	✓	✓	✓

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different standard independently. Each bank also has dedicated VREF pins to support any one of the voltage-referenced standards (such as SSTL-3) independently.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

Differential On-Chip Termination

Stratix devices provide differential on-chip termination (LVDS I/O standard) to reduce reflections and maintain signal integrity. Differential on-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections. The internal termination is designed using transistors in the linear region of operation.

Stratix devices support internal differential termination with a nominal resistance value of 137.5 Ω for LVDS input receiver buffers. LVPECL signals require an external termination resistor. Figure 2–71 shows the device with differential termination.

Table 4–28. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(3)*			0.4	V

Table 4–29. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			$V_{CCIO} \times 0.5$		V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.5		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(3)*			0.4	V

Table 4–30. 1.5-V Differential HSTL Class I & Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 4–31. CTT I/O Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		2.05	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ≤V_{OUT} ≤ V_{CCIO}	–10		10	µA

Table 4–32. Bus Hold Parameters										
Parameter	**Conditions**	**V_{CCIO} Level**								**Unit**
		1.5 V		**1.8 V**		**2.5 V**		**3.3 V**		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Low sustaining current	V_{IN} > V_{IL} (maximum)	25		30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)	-25		–30		–50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}		160		200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}		-160		–200		–300		–500	µA
Bus-hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

Table 4–49. M4K Block Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{M4KRC}		3,807		4,320		4,967		5,844	ps
t_{M4KWC}		2,556		2,840		3,265		3,842	ps
$t_{M4KWERESU}$	131		149		171		202		ps
$t_{M4KWEREH}$	34		38		43		51		ps
$t_{M4KCLKENSU}$	193		215		247		290		ps
$t_{M4KCLKENH}$	–63		–70		–81		–95		ps
$t_{M4KBESU}$	131		149		171		202		ps
t_{M4KBEH}	34		38		43		51		ps
$t_{M4KDATAASU}$	131		149		171		202		ps
$t_{M4KDATAAH}$	34		38		43		51		ps
$t_{M4KADDRASU}$	131		149		171		202		ps
$t_{M4KADDRAH}$	34		38		43		51		ps
$t_{M4KDATABSU}$	131		149		171		202		ps
$t_{M4KDATABH}$	34		38		43		51		ps
$t_{M4KADDRBSU}$	131		149		171		202		ps
$t_{M4KADDRBH}$	34		38		43		51		ps
$t_{M4KDATACO1}$		571		635		729		858	ps
$t_{M4KDATACO2}$		3,984		4,507		5,182		6,097	ps
$t_{M4KCLKHL}$	1,000		1,111		1,190		1,400		ps
t_{M4KCLR}	170		189		217		255		ps

Table 4–50. M-RAM Block Internal Timing Microparameters (Part 1 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{MRAMRC}		4,364		4,838		5,562		6,544	ps
t_{MRAMWC}		3,654		4,127		4,746		5,583	ps
$t_{MRAMWERESU}$	25		25		28		33		ps
$t_{MRAMWEREH}$	18		20		23		27		ps
$t_{MRAMCLKENSU}$	99		111		127		150		ps
$t_{MRAMCLKENH}$	–48		–53		–61		–72		ps

Table 4–63. EP1S20 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*									
Parameter	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**-8 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	1.351		1.479		1.699		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.732	5.380	2.732	5.728	2.732	6.240	NA	NA	ns
t_{XZ}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
t_{ZX}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
$t_{INSUPLL}$	0.923		0.971		1.098		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.210	2.544	1.210	2.648	1.210	2.715	NA	NA	ns
t_{XZPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns
t_{ZXPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns

Table 4–64. EP1S20 External I/O Timing on Row Pins Using Fast Regional Clock Networks *Note (1)*									
Parameter	**-5 Speed Grade**		**-6 Speed Grade**		**-7 Speed Grade**		**-8 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.032		2.207		2.535		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.492	5.018	2.492	5.355	2.492	5.793	NA	NA	ns
t_{XZ}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns
t_{ZX}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns

Table 4–77. EP1S30 External I/O Timing on Row Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.322		2.467		2.828		3.342		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.731	5.408	2.731	5.843	2.731	6.360	2.731	7.036	ns
t_{XZ}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
t_{ZX}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
$t_{INSUPLL}$	1.291		1.283		1.469		1.832		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.192	2.539	1.192	2.737	1.192	2.786	1.192	2.742	ns
t_{XZPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns
t_{ZXPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns

Table 4–78. EP1S30 External I/O Timing on Row Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.995		2.089		2.398		2.830		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.917	5.735	2.917	6.221	2.917	6.790	2.917	7.548	ns
t_{XZ}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
t_{ZX}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
$t_{INSUPLL}$	1.337		1.312		1.508		1.902		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.164	2.493	1.164	2.708	1.164	2.747	1.164	2.672	ns
t_{XZPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns
t_{ZXPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns

Figure 4–6 shows the case where four IOE registers are located in two different I/O banks.

Figure 4–6. I/O Skew Across Two I/O Banks

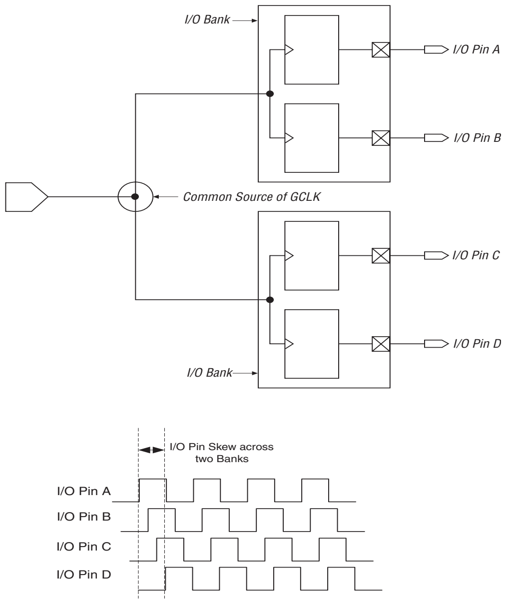


Table 4–97 defines the timing parameters used to define the timing for horizontal I/O pins (side banks 1, 2, 5, 6) and vertical I/O pins (top and bottom banks 3, 4, 7, 8). The timing parameters define the skew within an I/O bank, across two neighboring I/O banks on the same side of the device, across all horizontal I/O banks, across all vertical I/O banks, and the skew for the overall device.

Table 4–97. Output Pin Timing Skew Definitions (Part 1 of 2)

Symbol	Definition
t_{SB_HIO}	Row I/O (HIO) within one I/O bank *(1)*
t_{SB_VIO}	Column I/O (VIO) within one I/O bank *(1)*
t_{SS_HIO}	Row I/O (HIO) same side of the device, across two banks *(2)*
t_{SS_VIO}	Column I/O (VIO) same side of the device, across two banks *(2)*

External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density. All of the timing parameters in this section apply to both flip-chip and wire-bond packages.

Tables 4–103 and 4–104 show the input adder delays associated with column and row I/O pins. If an I/O standard is selected other than 3.3-V LVTTL or LVCMOS, add the selected delay to the external t_{INSU} and $t_{INSUPLL}$ I/O parameters shown in Tables 4–54 through 4–96.

Table 4–103. Stratix I/O Standard Column Pin Input Delay Adders

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0		0	ps
3.3-V LVTTL		0		0		0		0	ps
2.5-V LVTTL		19		19		22		26	ps
1.8-V LVTTL		221		232		266		313	ps
1.5-V LVTTL		352		369		425		500	ps
GTL		–45		–48		–55		–64	ps
GTL+		–75		–79		–91		–107	ps
3.3-V PCI		0		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0		0	ps
Compact PCI		0		0		0		0	ps
AGP 1×		0		0		0		0	ps
AGP 2×		0		0		0		0	ps
CTT		120		126		144		170	ps
SSTL-3 Class I		–162		–171		–196		–231	ps
SSTL-3 Class II		–162		–171		–196		–231	ps
SSTL-2 Class I		–202		–213		–244		–287	ps
SSTL-2 Class II		–202		–213		–244		–287	ps
SSTL-18 Class I		78		81		94		110	ps
SSTL-18 Class II		78		81		94		110	ps
1.5-V HSTL Class I		–76		–80		–92		–108	ps
1.5-V HSTL Class II		–76		–80		–92		–108	ps
1.8-V HSTL Class I		–52		–55		–63		–74	ps
1.8-V HSTL Class II		–52		–55		–63		–74	ps

Table 4–121. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	400	350	300	300	MHz
2.5 V	400	350	300	300	MHz
1.8 V	400	350	300	300	MHz
1.5 V	350	300	300	300	MHz
LVCMOS	400	350	300	300	MHz
GTL	200	167	125	125	MHz
GTL+	200	167	125	125	MHz
SSTL-3 Class I	167	150	133	133	MHz
SSTL-3 Class II	167	150	133	133	MHz
SSTL-2 Class I	150	133	133	133	MHz
SSTL-2 Class II	150	133	133	133	MHz
SSTL-18 Class I	150	133	133	133	MHz
SSTL-18 Class II	150	133	133	133	MHz
1.5-V HSTL Class I	250	225	200	200	MHz
1.5-V HSTL Class II	225	225	200	200	MHz
1.8-V HSTL Class I	250	225	200	200	MHz
1.8-V HSTL Class II	225	225	200	200	MHz
3.3-V PCI	250	225	200	200	MHz
3.3-V PCI-X 1.0	225	225	200	200	MHz
Compact PCI	400	350	300	300	MHz
AGP 1×	400	350	300	300	MHz
AGP 2×	400	350	300	300	MHz
CTT	300	250	200	200	MHz
LVPECL *(2)*	717	717	500	500	MHz
PCML *(2)*	420	420	420	420	MHz
LVDS *(2)*	717	717	500	500	MHz
HyperTransport technology *(2)*	420	420	420	420	MHz

Tables 4–125 and 4–126 show the high-speed I/O timing for Stratix devices.

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 1 of 4) Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (Clock frequency) (LVDS, LVPECL, HyperTransport technology) $f_{HSCLK} = f_{HSDR}$ / W	*W* = 4 to 30 (Serdes used)	10		210	10		210	10		156	10		115.5	MHz
	W = 2 (Serdes bypass)	50		231	50		231	50		231	50		231	MHz
	W = 2 (Serdes used)	150		420	150		420	150		312	150		231	MHz
	W = 1 (Serdes bypass)	100		462	100		462	100		462	100		462	MHz
	W = 1 (Serdes used)	300		717	300		717	300		624	300		462	MHz
f_{HSDR} Device operation (LVDS, LVPECL, HyperTransport technology)	*J* = 10	300		840	300		840	300		640	300		462	Mbps
	J = 8	300		840	300		840	300		640	300		462	Mbps
	J = 7	300		840	300		840	300		640	300		462	Mbps
	J = 4	300		840	300		840	300		640	300		462	Mbps
	J = 2	100		462	100		462	100		640	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		462	100		462	100		640	100		462	Mbps

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 4 of 4) Notes (1), (2)														
Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{DUTY}	LVDS (*J* = 2 through 10)	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (*J* =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100			100	µs

Notes to Table 4–125:

(1) When J = 4, 7, 8, and 10, the SERDES block is used.

(2) When J = 2 or J = 1, the SERDES is bypassed.