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Applications of "Embedded - Microcontrollers"

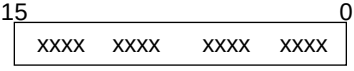
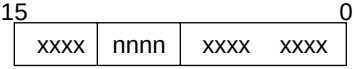
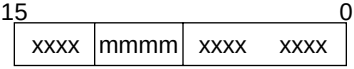
Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, SCI, SmartCard
Peripherals	POR, WDT
Number of I/O	8
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	3.15V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417708rf100av

2.3.3 Instruction Formats

Table 2.3 explains the meaning of instruction formats and source and destination operands. The meaning of the operands depends on the operation code. The following symbols are used.

xxxx: Operation code
mmmm: Source register
nnnn: Destination register
iiii: Immediate data
dddd: Displacement

Table 2.3 Instruction Formats

Instruction Format	Source Operand	Destination Operand	Instruction Example
0 format 	—	—	NOP
n format 	—	nnnn: register direct	MOVT Rn
	Control register or system register	nnnn: register direct	STS MACH,Rn
	Control register or system register	nnnn: register indirect with pre-decrement	STC.L SR,@–Rn
m format 	mmmm: register direct	Control register or system register	LDC Rm,SR
	mmmm: register indirect with post-increment	Control register or system register	LDC.L @Rm+,SR
	mmmm: register indirect	—	JMP @Rm
	mmmm: PC-relative using Rm	—	BRAF Rm

3.6.2 Data Array

The data array is assigned to H'F3000000 to H'F3FFFFFF. To access a data array, the 32-bit address field (for read/write operations), and 32-bit data field (for write operations) must be specified. These are specified in the general register. The address section specifies information for selecting the entry to be accessed; the data section specifies the longword data to be written to the data array (figure 3.14 (2)).

In the address section, specify the entry address for selecting the entry (bits 16–12), W for selecting the way (bits 9–8: 00 is way 0, 01 is way 1, 10 is way 2, 11 is way 3), and H'F3 to indicate data array access (bits 31–24). The IX bit in MMUCR indicates whether an EX-OR is taken of the entry address and ASID.

Both reading and writing use the longword of the data array specified by the entry address and way number. The access size of the data array is fixed at longword.

Section 7 User Break Controller (UBC)

7.1 Overview

The user break controller (UBC) provides functions that simplify program debugging. These functions make it easy to design an effective self-monitoring debugger, enabling programs to be debugged in the chip alone, without using an in-circuit emulator. Break conditions that can be set in the UBC are instruction fetch or data read/write, data size, data content, address value, and stop timing during instruction fetches.

7.1.1 Features

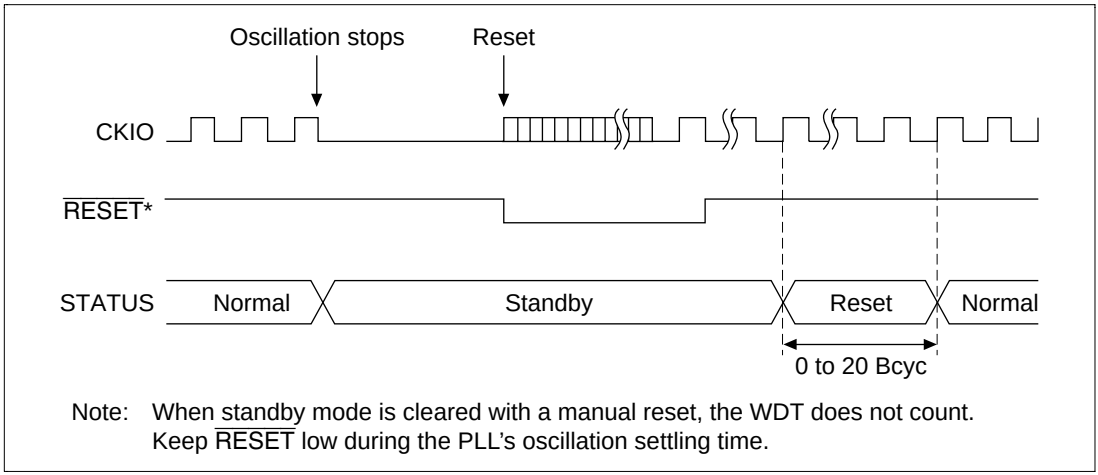
The features of the user break controller are listed below.

- Two break channels (channel A and channel B). User break interrupts can be requested using either independent or sequential condition for the two channels (sequential breaks are channel A, then channel B).
- Selection and setting of the following as break compare conditions:
  - Address
    Selection of 32-bit logical address and ASID to be compared
    Address: Compare all bits, mask bottom 10 bits, mask bottom 12 bits. mask all bits
    ASID: Compare all bits/mask all bits
  - Data (channel B only, 32-bit maskable)
  - Bus cycle: Instruction fetch/data access
  - Read/write
  - Operand size: byte/word/longword
- The instruction fetch cycle break can be performed before or after the instruction is executed.
- User break trap generated when break conditions are satisfied. A user-designed user break trap routine can be run.

7.1.2 Block Diagram

Figure 7.1 shows the logical block diagram of the user break controller.

Standby to Manual Reset:



Note: When standby mode is cleared with a manual reset, the WDT does not count. Keep RESET low during the PLL's oscillation settling time.

Figure 8.6 Standby to Manual Reset STATUS Output

8.6.3 Timing for Canceling Sleep Mode

Sleep to Interrupt:

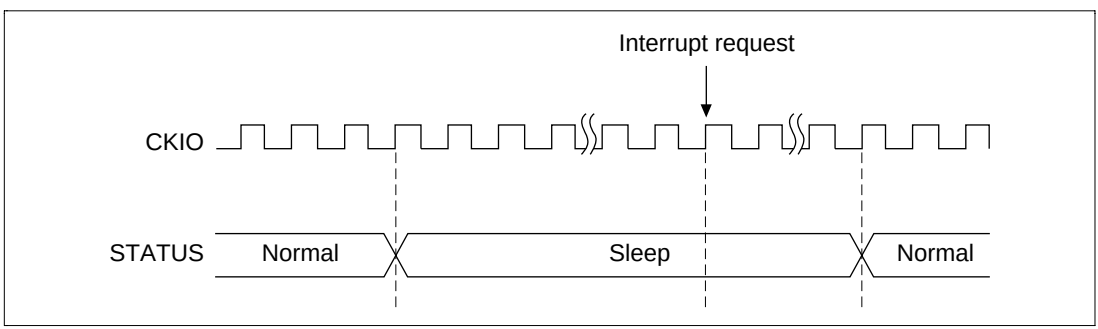


Figure 8.7 Sleep to Interrupt STATUS Output

9.2 Overview of the CPG

9.2.1 CPG Block Diagram

A block diagram of the on-chip clock pulse generator is shown in figure 9.1(SH7708, SH7708S) and figure 9.2(SH7708R).

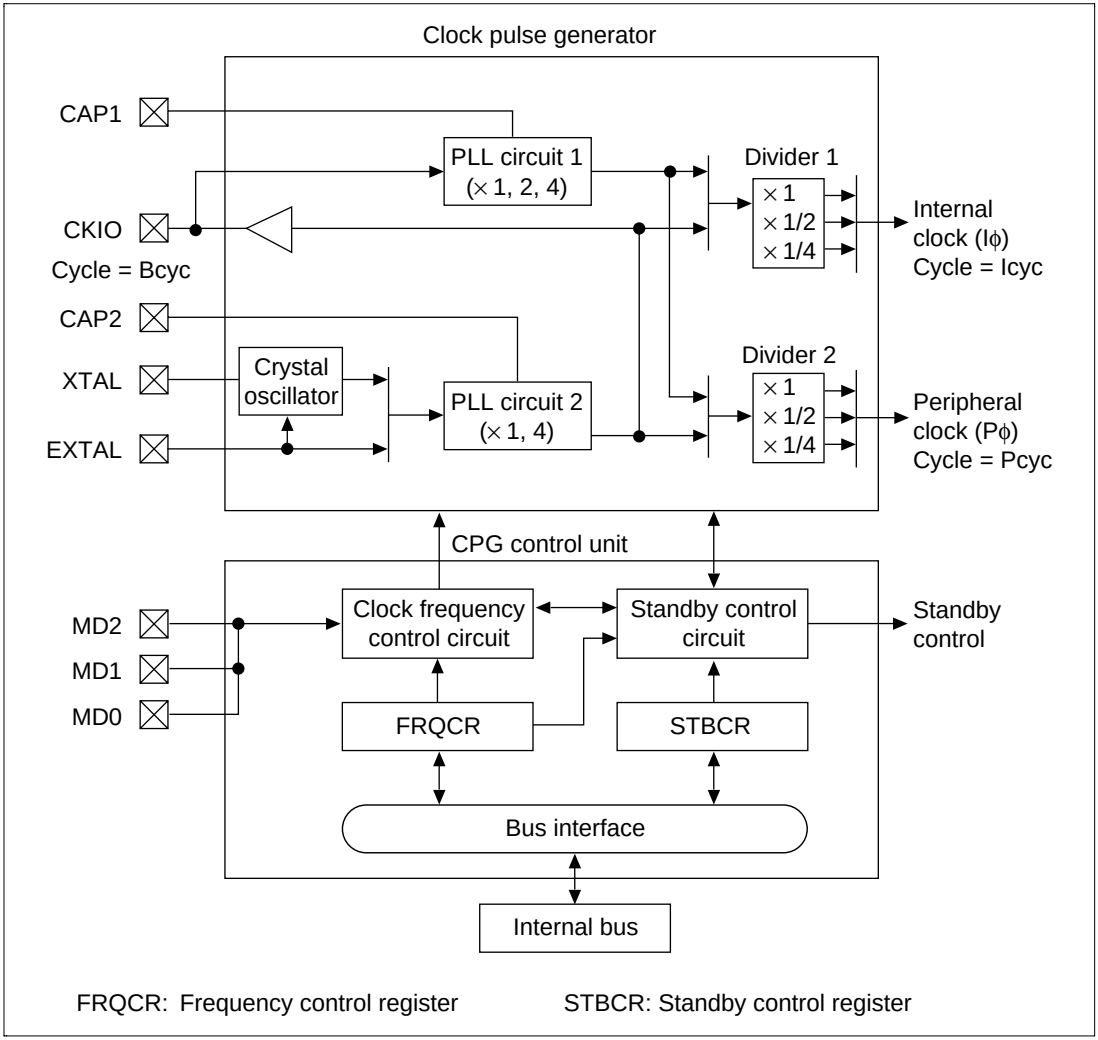


Figure 9.1 Block Diagram of Clock Pulse Generator(SH7708, SH7708S)

10.2 BSC Registers

10.2.1 Bus Control Register 1 (BCR1)

The bus control register 1 (BCR1) is a 16-bit read/write register that sets the functions and bus cycle status for each area. It is initialized to H'0000 by a power-on reset, but is not initialized by a manual reset or in standby mode. Do not access external memory outside area 0 until BCR1 register initialization is complete.

Bit:	15	14	13	12	11	10	9	8
Bit name:	—	—	HIZMEM*2	HIZCNT	ENDIAN	A0BST1	A0BST0	A5BST1
Initial value:	0	0	0	0	0/1*1	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
Bit name:	A5BST0	A6BST1	A6BST0	DRAM TP2	DRAM TP1	DRAM TP0	A5PCM	A6PCM
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Notes: 1. Samples the value of the external pin designating endian upon a power-on reset.
2. Reserved bit in the SH7708.

Bits 15 and 14—Reserved: These bits always read 0. The write value should always be 0.

Bits 13 (SH7708)—Reserved: These bits always read 0. The write value should always be 0. This bit is not supported in emulator.

Bit 13 (SH7708S, SH7708R) —High-Z Memory Control (HIZMEM): Specifies the state of A25 to A0, BS, CS, RD/WR, WE/DQM, RD, MD3/CE2A, and MD4/CE2B in standby mode.

Bit 13: HIZMEM	Description	
0	High-impedance (high-Z) in standby mode	(Initial value)
1	Drive state in standby mode	

Bit 12—High-Z Control (HIZCNT): Specifies the state of the RAS and CAS signals in the standby and bus-released states.

Bits 9 and 8—CAS-Before-RAS Refresh RAS Assert Time (TRAS1, TRAS0): These bits set the RAS assert period for CAS-before-RAS refreshing of the DRAM connected to area 2.

In the SH7708, set the same values in the TRAS bits in MCR and DCR.

Bit 9: TRAS1	Bit 8: TRAS0	Description	
0	0	2 cycles	(Initial value)
	1	3 cycles	
1	0	4 cycles	
	1	5 cycles	

Bit 6—Burst Enable (BE): Specifies whether to conduct a burst access of the DRAM connected to area 2.

Bit 6: BE	Description	
0	Burst disabled	(Initial value)
1	High-speed page mode access	

Bits 4 and 3—Address Multiplex (AMX1, AMX0): These bits specify address multiplexing for the DRAM connected to area 2.

Bit 4: AMX1	Bit 3: AMX0	Description	
0	0	8-bit column address product	(Initial value)
	1	9-bit column address product	
1	0	10-bit column address product	
	1	11-bit column address product	

Bit 2—Refresh Control (RFSH): Determines whether or not refreshing of the DRAM connected to area 2 is performed.

Bit 2: RFSH	Description	
0	No refresh	(Initial value)
1	Refresh	

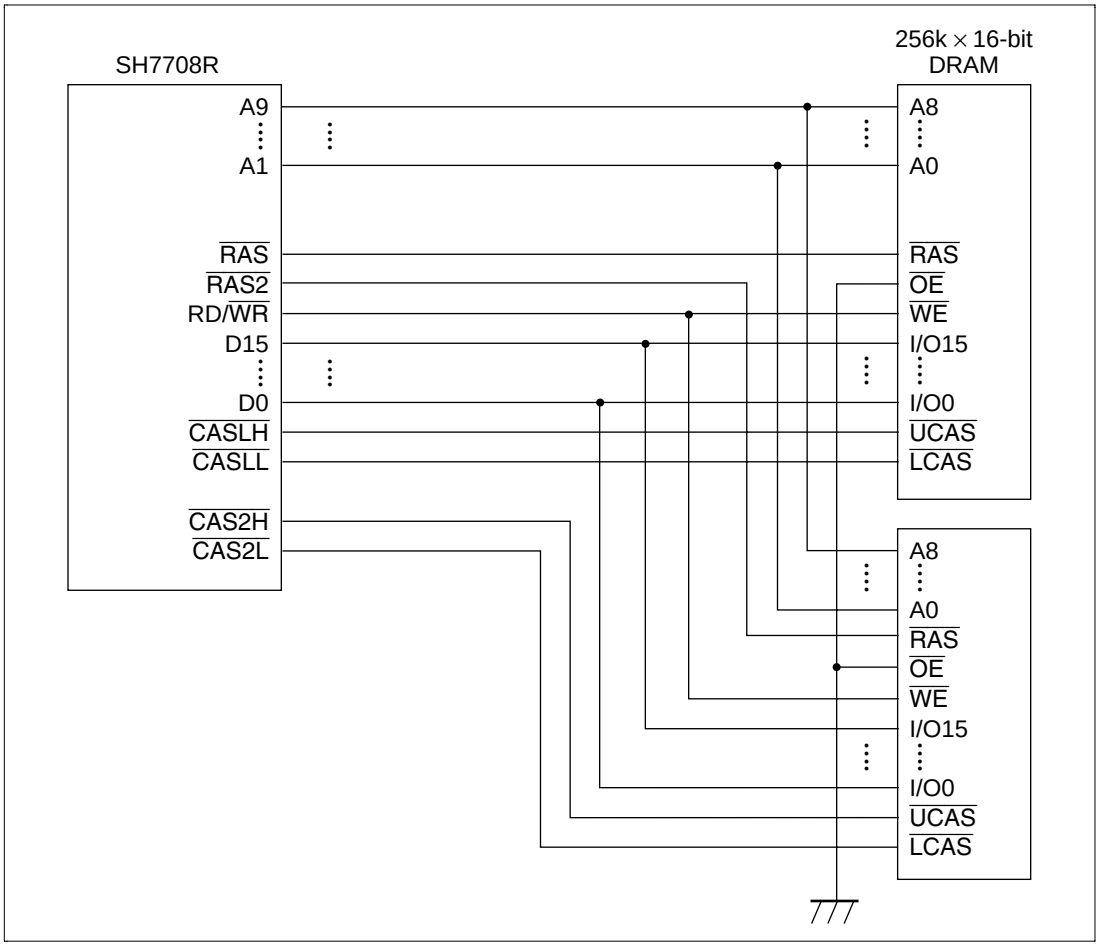


Figure 10.14 Example of DRAM Connection (16-Bit Data Width)

13.1.3 Pin Configuration

The SCI has the serial pins summarized in table 13.1.

Table 13.1 SCI Pins

Pin Name	Abbreviation	Input/Output	Function
Serial clock pin	SCK	Input/output	Clock input/output
Receive data pin	RxD	Input	Receive data input
Transmit data pin	TxD	Output	Transmit data output

Note: These pins function as mode input pins MD0–MD02 after a power-on reset. They are made to function as serial pins by performing SCI operation settings with the TE, RE, CKEI, and CKE0 bits in SCSCR and the C/$\overline{A}$ bit in SCSMR. Break status transmission and detection can be performed by means of the SCI's SCSPTR register.

13.1.4 Register Configuration

Table 13.2 summarizes the SCI internal registers. These registers select the communication mode (asynchronous or synchronous), specify the data format and bit rate, and control the transmitter and receiver sections.

Table 13.2 Registers

Name	Abbreviation	R/W	Initial Value*[2]	Address	Access Size
Serial mode register	SCSMR	R/W	H'00	H'FFFFFE80	8
Bit rate register	SCBRR	R/W	H'FF	H'FFFFFE82	8
Serial control register	SCSCR	R/W	H'00	H'FFFFFE84	8
Transmit data register	SCTDR	R/W	H'FF	H'FFFFFE86	8
Serial status register	SCSSR	R/(W)*[1]	H'84	H'FFFFFE88	8
Receive data register	SCRDR	R	H'00	H'FFFFFE8A	8
Serial port register	SCSPTR	R/W	Undefined (Initialized)*[3]	H'FFFFFF7C	8

Notes: 1 Only 0 can be written, to clear the flags.
2 Initialized by power-on reset or manual reset.
3. All bits except 2 and 0 are initialized to 0. The value of bits 2 and 0 is undefined.

Bit 3—Stop Bit Length (STOP): Selects one or two bits as the stop bit length in asynchronous mode. This setting is used only in asynchronous mode. It is ignored in synchronous mode because no stop bits are added.

In receiving, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit, but if the second stop bit is 0, it is treated as the start bit of the next incoming character.

Bit 3: STOP	Description	
0	One stop bit	(Initial value)
	In transmitting, a single 1-bit is added at the end of each transmitted character.	
1	Two stop bits	
	In transmitting, two 1-bits are added at the end of each transmitted character.	

Bit 2—Multiprocessor Mode (MP): Selects multiprocessor format. When multiprocessor format is selected, settings of the parity enable (PE) and parity mode (O/$\overline{E}$) bits are ignored. The MP bit setting is used only in asynchronous mode; it is ignored in synchronous mode. For the multiprocessor communication function, see section 13.3.3, Multiprocessor Communication.

Bit 2: MP	Description	
0	Multiprocessor function disabled	(Initial value)
1	Multiprocessor format selected	

Bits 1 and 0—Clock Select 1 and 0 (CKS1 and CKS0): These bits select the internal clock source of the on-chip baud rate generator. Four clock sources are available: Pϕ, Pϕ/4, Pϕ/16 and Pϕ/64. For further information on the clock source, bit rate register settings, and baud rate, see section 13.2.9, Bit Rate Register.

Bit 1: CKS1	Bit 0: CKS0	Description	
0	0	Pϕ	(Initial value)
	1	Pϕ/4	
1	0	Pϕ/16	
	1	Pϕ/64	

Note: Pϕ: Peripheral clock

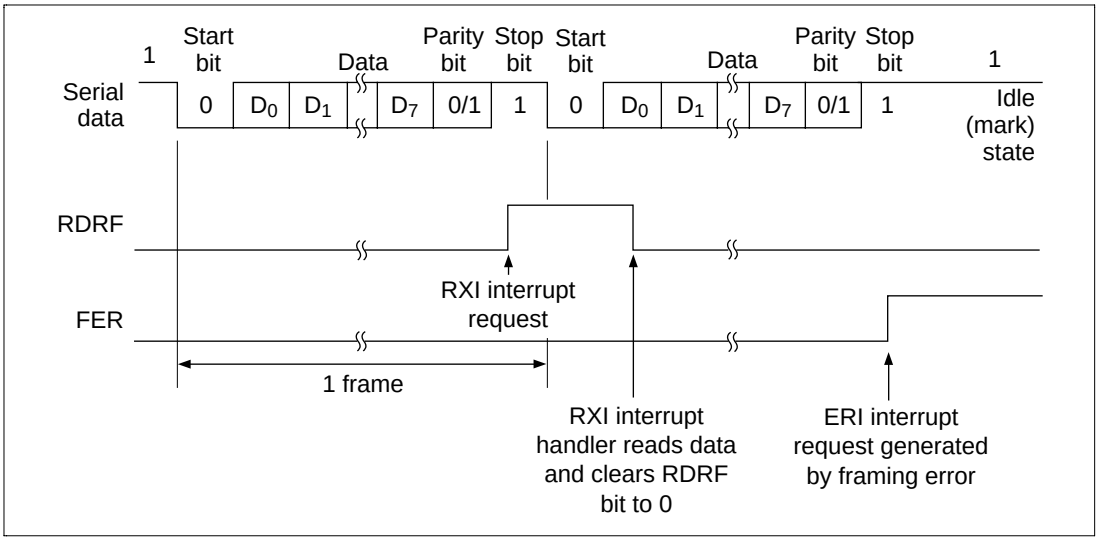


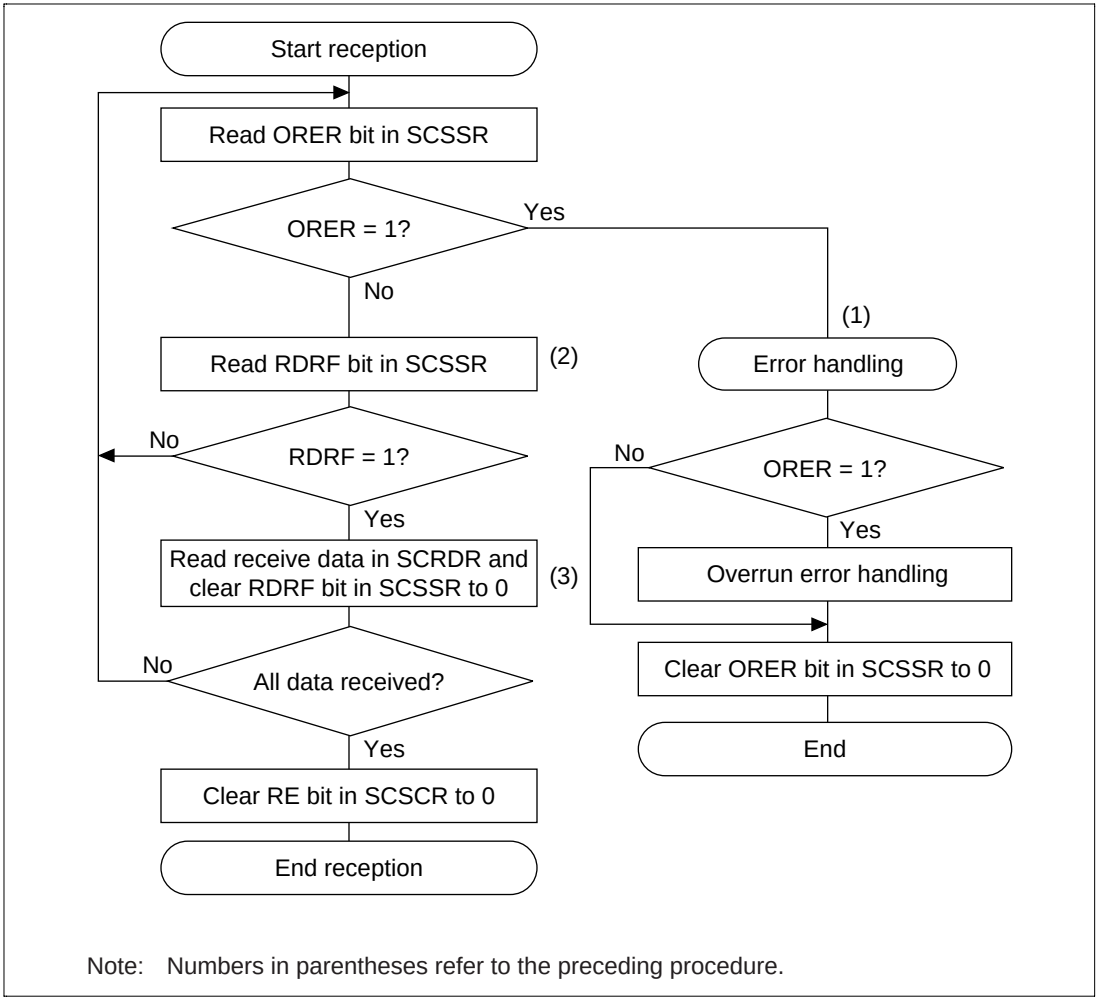
Figure 13.8 SCI Receive Operation (Example: 8-bit Data with Parity and One Stop Bit)

13.3.3 Multiprocessor Communication

The multiprocessor communication function enables several processors to share a single serial communication line. The processors communicate in asynchronous mode using a format with an additional multiprocessor bit (multiprocessor format).

In multiprocessor communication, each receiving processor is addressed by a unique ID. A serial communication cycle consists of an ID-sending cycle that identifies the receiving processor, and a data-sending cycle. The multiprocessor bit distinguishes ID-sending cycles from data-sending cycles. The transmitting processor starts by sending the ID of the receiving processor with which it wants to communicate as data with the multiprocessor bit set to 1. Next the transmitting processor sends transmit data with the multiprocessor bit cleared to 0.

Receiving processors skip incoming data until they receive data with the multiprocessor bit set to 1. When they receive data with the multiprocessor bit set to 1, receiving processors compare the data with their IDs. The receiving processor with a matching ID continues to receive further incoming data. Processors with IDs not matching the received data skip further incoming data until they again receive data with the multiprocessor bit set to 1. Multiple processors can send and receive data in this way.



Note: Numbers in parentheses refer to the preceding procedure.

Figure 13.18 Sample Flowchart for Serial Receiving

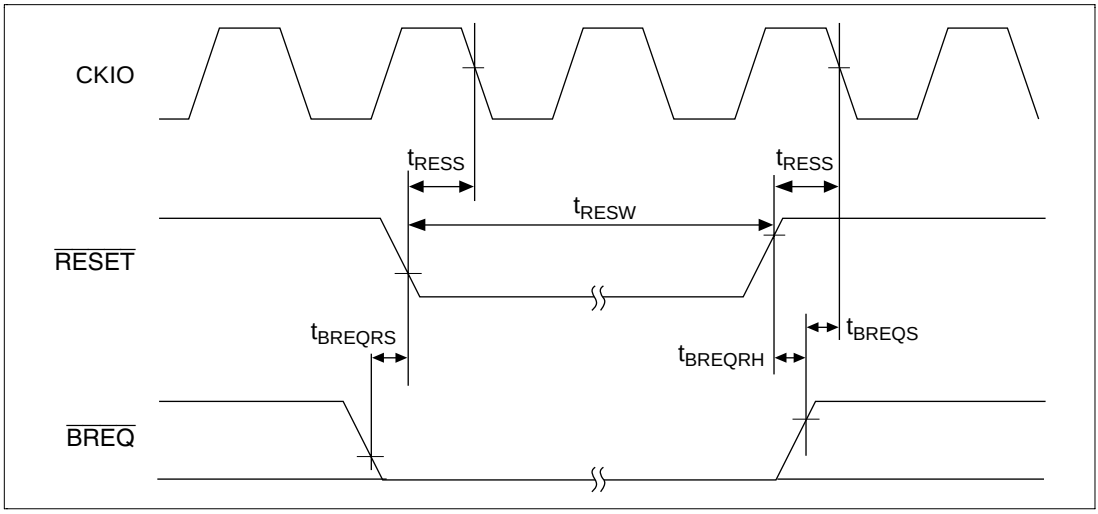


Figure 16.11 Manual Reset Input Timing

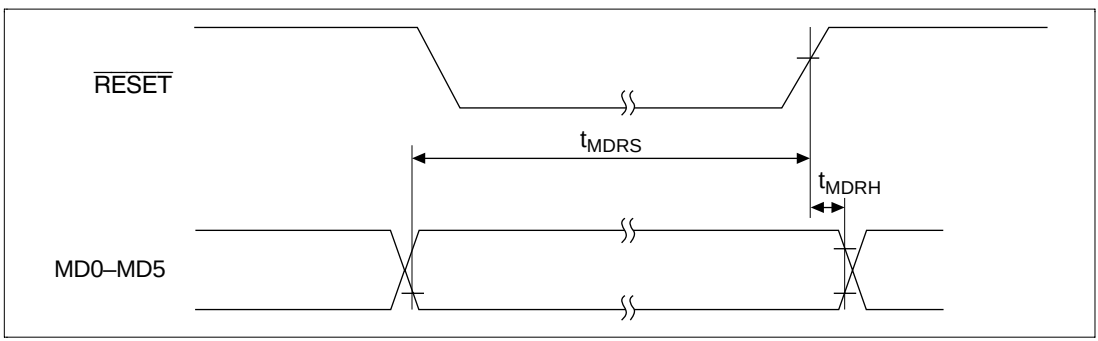


Figure 16.12 Mode Input Timing

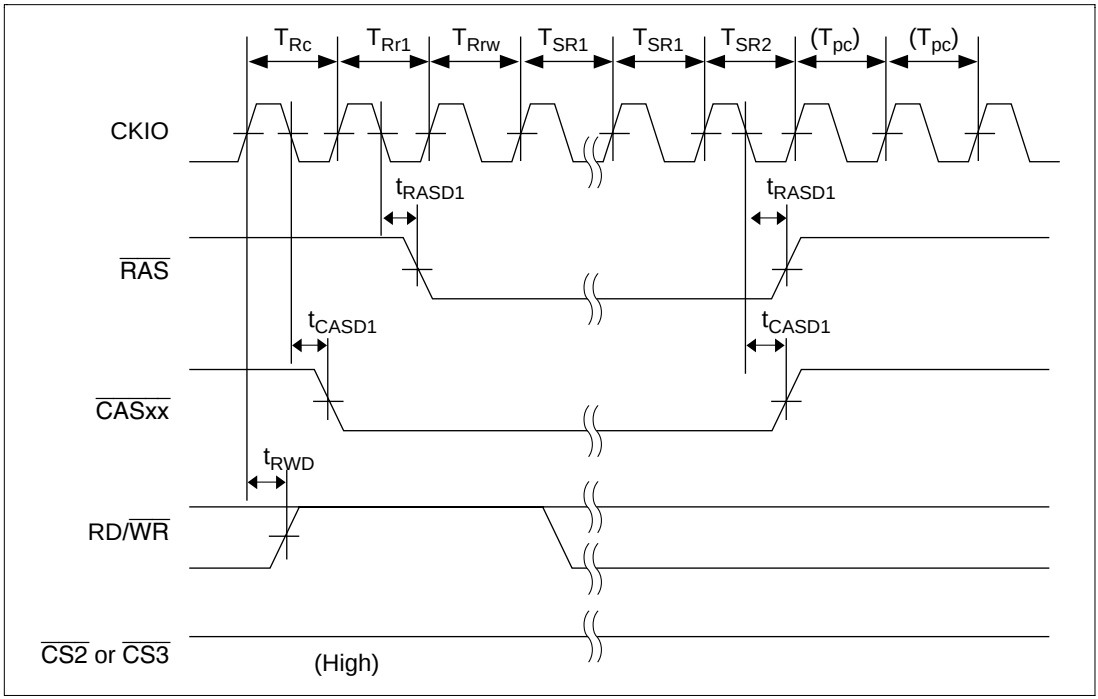


Figure 16.33 DRAM Self-Refresh Cycle (TPC = 0)

16.3.7 Synchronous DRAM Timing

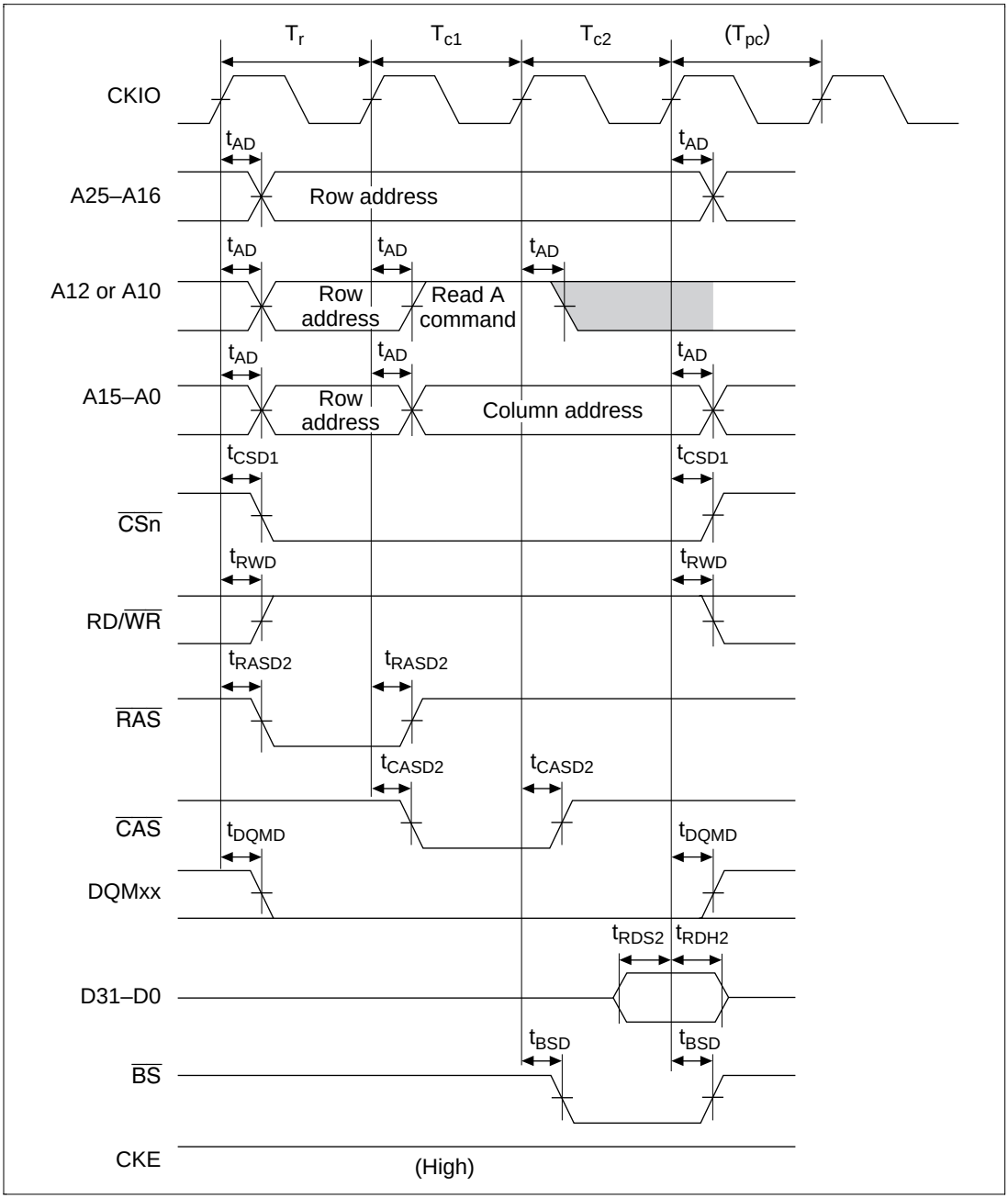


Figure 16.34 Synchronous DRAM Read Bus Cycle (RCD = 0, CAS Latency = 1, TPC = 0)

17.2 DC Characteristics

Table 17.2 DC Characteristics (Ta = –20 to 75°C)

Item		Symbol	Min	Typ	Max	Unit	Remarks
Power supply voltage		V_{CC}	3.15	3.3	3.6	V	In normal operation, sleep mode, and standby mode
Current	Normal operation	I_{CC}	—	120*[1]	200 *[1]	mA	V_{CC} = 3.3 V *1 Iø = 100 MHz Bø = 50 MHz
	In sleep mode		—	75*[2]	100 *[2]		*2 Bø = 60 MHz Pø = 30 MHz
	In standby mode		—	0.1*[3]	1*[3]	mA	*3 V_{CC} = 3.3 V/ Ta= 30 °C
Input voltage	RESET, NMI	VIH	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	BREQ, IRL3–IRL0, MD5–MD0		V_{CC} – 0.5	—	V_{CC} + 0.3		Standby mode
			V_{CC} – 0.7	—	V_{CC} + 0.3		Normal operation
	EXTAL, CKIO		V_{CC} – 0.7	—	V_{CC} + 0.3		
	Other input pins		2.0	—	V_{CC} + 0.3		
	RESET, NMI	VIL	–0.3	—	$V_{CC} \times 0.1$		
	BREQ, IRL3–IRL0, MD5–MD0		–0.3	—	0.5		Standby mode
			–0.3	—	$V_{CC} \times 0.2$		Normal operation
	Other input pins		–0.3	—	$V_{CC} \times 0.2$		
Input leak current	All input pins	|Iin|	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Three-state leak current	I/O, output, all pins (off condition)	|Isti|	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V

Table A.4 Pin States (Normal Memory/Big-Endian) (cont)

	32-Bit Bus Width						
Pin	**Byte Access (Address 4n)**	**Byte Access (Address 4n + 1)**	**Byte Access (Address 4n + 2)**	**Byte Access (Address 4n + 3)**	**Word Access (Address 4n)**	**Word Access (Address 4n + 2)**	**Longword Access**
D15 to D8	Invalid data	Invalid data	Valid data	Invalid data	Invalid data	Valid data	Valid data
D23 to D16/ PORT7 to PORT0	Invalid data	Valid data	Invalid data	Invalid data	Valid data	Invalid data	Valid data
D31 to D24	Valid data	Invalid data	Invalid data	Invalid data	Valid data	Invalid data	Valid data

Notes: 1. When BCR1.A5PCM = 0, high-Z.
2. When BCR1.A6PCM = 0, high-Z.
3. When BCR1.DRAMTP (2–0) ≠ 101, high-Z.
4. When WCR2 register wait setting is 0, disabled.
5. When BCR2.PORTEN = 0, high-Z. When BCR2.PORTEN = 1, dependent on PCTR register .
6. When BCR2.PORTEN = 0, high-Z. When BCR2.PORTEN = 1, D31 and D30 only data output.

Table B.1 Memory-Mapped Control Register Address Map (cont)

Register	Abbreviation	Module	Bus	Address	Size	Access Size
Interrupt control register	ICR	INTC	P	H'FFFFFEE0	16	16
Interrupt priority level setting register A	IPRA	INTC	P	H'FFFFFEE2	16	16
Interrupt priority level setting register B	IPRB	INTC	P	H'FFFFFEE4	16	16
Timer output control register	TOCR	TMU	P	H'FFFFFE90	8	8
Timer start register	TSTR	TMU	P	H'FFFFFE92	8	8
Timer constant register 0	TCOR0	TMU	P	H'FFFFFE94	32	32
Timer counter 0	TCNT0	TMU	P	H'FFFFFE98	32	32
Timer control register 0	TCR0	TMU	P	H'FFFFFE9C	16	16
Timer constant register 1	TCOR1	TMU	P	H'FFFFFEA0	32	32
Timer counter 1	TCNT1	TMU	P	H'FFFFFEA4	32	32
Timer control register 1	TCR1	TMU	P	H'FFFFFEA8	16	16
Timer constant register 2	TCOR2	TMU	P	H'FFFFFEAC	32	32
Timer counter 2	TCNT2	TMU	P	H'FFFFFEB0	32	32
Timer control register 2	TCR2	TMU	P	H'FFFFFEB4	16	16
Input capture register 2	TCPR2	TMU	P	H'FFFFFEB8	32	32
Serial mode register	SCSMR	SCI	P	H'FFFFFE80	8	8
Bit rate register	SCBRR	SCI	P	H'FFFFFE82	8	8
Serial control register	SCSCR	SCI	P	H'FFFFFE84	8	8
Transmit data register	SCTDR	SCI	P	H'FFFFFE86	8	8
Serial status register	SCSSR	SCI	P	H'FFFFFE88	8	8
Receive data register	SCRDR	SCI	P	H'FFFFFE8A	8	8
Smartcard mode register	SCSCMR	SCI	P	H'FFFFFE8C	8	8