

Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c60413-16lkxct

Functional Overview

The enCoRe V LV family of devices are designed to replace multiple traditional low voltage microcontroller system components with one, low cost single chip programmable component. Communication peripherals (I²C/SPI), a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in [enCoRe V LV Block Diagram](#), is comprised of two main areas: the CPU core and the system resources. Depending on the enCoRe V LV package, up to 36 GPIO are also included.

Enhancements over the Cypress's legacy low-voltage microcontrollers include faster CPU at lower voltage operation, lower current consumption, twice the RAM and flash, hot-swappable I/Os, I²C hardware address recognition, new very low-current sleep mode, and new package options.

The enCoRe V LV Core

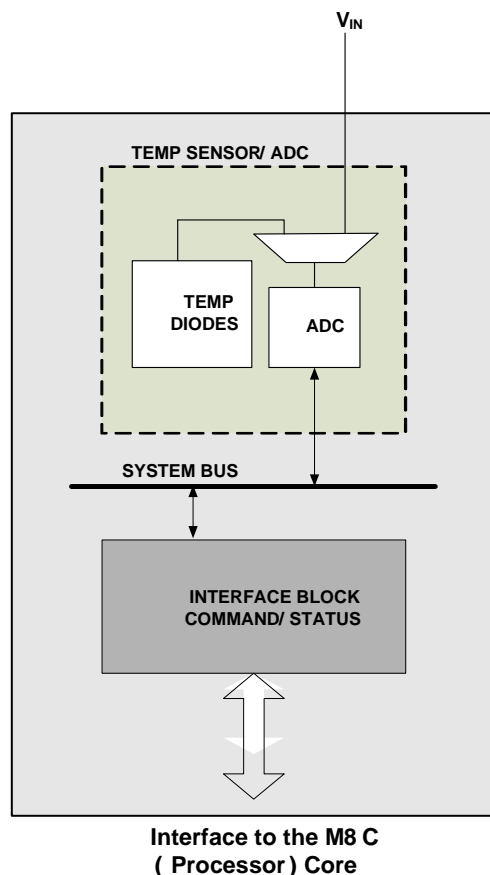
The enCoRe V LV Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low-speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as a configurable I²C slave and SPI master-slave communication interface and various system resets supported by the M8C.

10-bit ADC

The ADC on enCoRe V LV device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog Mux Bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 1. ADC System Performance Block Diagram



The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the Analog Global Input Mux or the temperature sensor with an input voltage range of 0 V to 1.3 V, where 1.3 V is 72% of full scale.

In the ADC only configuration (the ADC MUX selects the Analog Mux Bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the resolution of the ADC desired by the user. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

The basic I²C features include:

- *Slave, transmitter, and receiver operation
- *Byte processing for low CPU overhead
- *Interrupt or polling CPU interface
- *Support for clock rates of up to 400 kHz
- *7- or 10-bit addressing (through firmware support)
- *SMBus operation (through firmware support)

Enhanced features of the I²C Slave Enhanced Module include:

- *Support for 7-bit hardware address compare
- *Flexible data buffering schemes
- *A 'no bus stalling' operating mode
- *A low power bus monitoring mode

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V LV CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource:

- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- The 3.6 V maximum input, 1.8, 2.5, or 3 V selectable output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V LV family of parts.

Getting Started

The quickest way to understanding the enCoRe V silicon is by reading this datasheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer to the *PSoC Programmable System-on-Chip Technical Reference Manual*, for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, reference the latest enCoRe V device datasheets on the web at <http://www.cypress.com>.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

32-Pin Part Pinout

Figure 6. CY7C60445 32-Pin enCoRe V LV Device

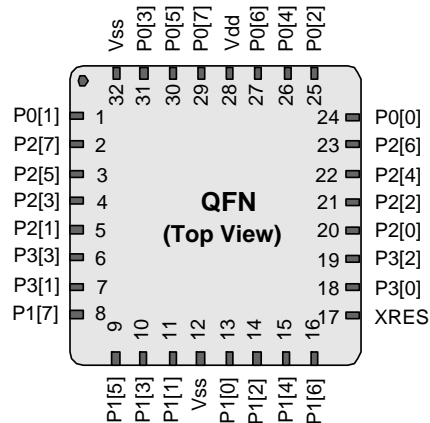


Table 2. 32-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	IOH	P0[1]	Digital I/O
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, crystal out (Xout)
4	I/O	P2[3]	Digital I/O, crystal in (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P3[3]	Digital I/O
7	I/O	P3[1]	Digital I/O
8	IOHR	P1[7]	Digital I/O, I ² C SCL, SPI SS
9	IOHR	P1[5]	Digital I/O, I ² C SDA, SPI MISO
10	IOHR	P1[3]	Digital I/O, SPI CLK
11	IOHR	P1[1] ^(1,2)	Digital I/O, ISSP CLK, I ² C SCL, SPI MOSI
12	Power	Vss	Ground connection
13	IOHR	P1[0] ^(1,2)	Digital I/O, ISSP DATA, I ² C SDA, SPI CLK
14	IOHR	P1[2]	Digital I/O
15	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
16	IOHR	P1[6]	Digital I/O
17	Reset Input	XRES	Active high external reset with internal pull-down
18	I/O	P3[0]	Digital I/O
19	I/O	P3[2]	Digital I/O
20	I/O	P2[0]	Digital I/O
21	I/O	P2[2]	Digital I/O
22	I/O	P2[4]	Digital I/O
23	I/O	P2[6]	Digital I/O
24	IOH	P0[0]	Digital I/O
25	IOH	P0[2]	Digital I/O
26	IOH	P0[4]	Digital I/O
27	IOH	P0[6]	Digital I/O

48-Pin Part Pinout

Figure 7. CY7C60455/CY7C60456 48-Pin enCoRe V LV Device

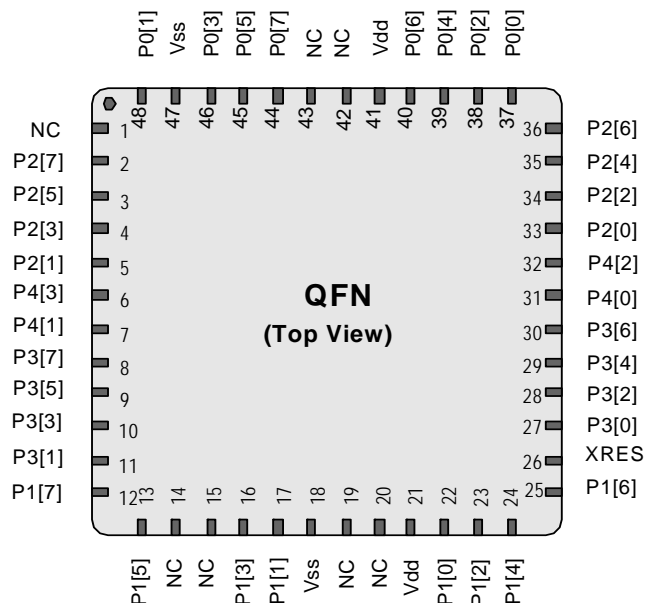


Table 3. 48-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	NC	NC	No connection
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, crystal out (Xout)
4	I/O	P2[3]	Digital I/O, crystal in (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P4[3]	Digital I/O
7	I/O	P4[1]	Digital I/O
8	I/O	P3[7]	Digital I/O
9	I/O	P3[5]	Digital I/O
10	I/O	P3[3]	Digital I/O
11	I/O	P3[1]	Digital I/O
12	IOHR	P1[7]	Digital I/O, I ² C SCL, SPI SS
13	IOHR	P1[5]	Digital I/O, I ² C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	IOHR	P1[3]	Digital I/O, SPI CLK
17	IOHR	P1[1] ^(1,2)	Digital I/O, ISSP CLK, I ² C SCL, SPI MOSI
18	Power	Vss	Supply ground
19	NC	NC	No connection
20	NC	NC	No connection
21	Power	Vdd	Supply voltage

Register Reference

The section discusses the registers of the enCoRe V LV device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V LV device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the 'extended' address space or the 'configuration' registers.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
	02			42			82			C2	
	03			43			83			C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45			85			C5	
	06			46			86			C6	
	07			47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
PRT4DM0	10	RW		50			90			D0	
PRT4DM1	11	RW		51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C		IO_CFG	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E			DE	
	1F			5F			9F			DF	
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
	34			74			B4			F4	
	35			75			B5			F5	
	36			76			B6			F6	
	37			77			B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE			FE	
	3F			7F			BF			FF	

Gray fields are reserved and should not be accessed. # Access is bit specific.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{STG}	Storage temperature ^[3]	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
V _{DD}	Supply voltage relative to V _{SS}		–0.5	–	+6.0	V
V _{IO}	DC input voltage		V _{SS} – 0.5	–	V _{DD} + 0.5	V
V _{IOZ}	DC voltage applied to tristate		V _{SS} – 0.5	–	V _{DD} + 0.5	V
I _{MIO}	Maximum current into any Port pin		–25	–	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	–	–	V
LU	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{AC}	Ambient commercial temperature		0		+70	°C
T _{JC}	Operational commercial die temperature ^[4]	The temperature rise from ambient to junction is package specific. Refer the table “ Thermal Impedances ” on page 30. The user must limit the power consumption to comply with this requirement.	0		+85	°C

Notes

3. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
4. The temperature rise from ambient to junction is package specific. See [Thermal Impedances on page 30](#). The user must limit the power consumption to comply with this requirement.

DC General Purpose I/O Specifications ^[7]

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 1.71 V to 3.6 V and $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. Typical parameters apply to 3.3 V at 25°C . These are for design guidance only.

Table 10. 3.0 V to 3.6 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor	–	4	5.6	8	k Ω
V _{OH1}	High output voltage Port 2 or 3 pins	IOH \leq 10 μA , maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V _{OH2}	High output voltage Port 2 or 3 pins	IOH = 1 mA, maximum of 20 mA source current in all I/Os	Vdd – 0.9	–	–	V
V _{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH $<$ 10 μA , maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V _{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 5 mA, maximum of 20 mA source current in all I/Os	Vdd – 0.9	–	–	V
V _{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	IOH $<$ 10 μA , Vdd $>$ 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V _{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	IOH = 5 mA, Vdd $>$ 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V _{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	IOH $<$ 10 μA , Vdd $>$ 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V _{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	IOH = 2 mA, Vdd $>$ 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V _{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH $<$ 10 μA , Vdd $>$ 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V _{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH = 1 mA, Vdd $>$ 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low output voltage	IOL = 25 mA, Vdd $>$ 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input low voltage	–	–	–	0.80	V
V _{IH}	Input high voltage	–	2.00	–	–	V
V _H	Input hysteresis voltage	–	–	80	–	mV
I _{IL}	Input leakage (absolute value)	–	–	0.001	1	μA
C _{PIN}	Pin capacitance	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Note

7. **Errata:** P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins. Add a series resistor $>$ 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits. For more information please refer to "Errata" on page 33.

ADC Electrical Specifications

Table 13. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	V_{REFADC}	V
C_{IIN}	Input capacitance	–		–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500fF \times \text{data clock})$	$1/(400fF \times \text{data clock})$	$1/(300fF \times \text{data clock})$	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data Clock set to 6 MHz. Sample Rate = $0.001 / (2^{\text{Resolution}} / \text{Data Clock})$	–	–	–	ksps
S10	10-bit sample rate	Data Clock set to 6 MHz. Sample Rate = $0.001 / (2^{\text{Resolution}} / \text{Data Clock})$	–	5.859	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR ($V_{dd} > 3.0 \text{ V}$)	–	24	–	dB
		PSRR ($V_{dd} < 3.0 \text{ V}$)	–	30	–	dB

AC Electrical Characteristics

AC Chip Level Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{CPU}	Processing frequency		5.7	—	25.2	MHz
F _{32K1}	Internal low speed oscillator frequency	Trimmed for 3.3 V operation using factory trim values	19	32	50	kHz
F _{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	—	13	32	82	kHz
F _{32K2}	Internal low speed oscillator frequency	Untrimmed	13	32	82	kHz
F _{IMO24}	Internal main oscillator stability for 24 MHz \pm 5%	—	22.8	24	25.2	MHz
F _{IMO12}	Internal main oscillator stability for 12 MHz	—	11.4	12	12.6	MHz
F _{IMO6}	Internal main oscillator stability for 6 MHz	—	5.7	6.0	6.3	MHz
DC _{IMO}	Duty Cycle of IMO	—	40	50	60	%
DC _{ILO}	Internal low speed oscillator duty cycle	—	40	50	60	%
SR _{POWER_UP}	Power supply slew rate	—	—	—	250	V/ms
T _{XRST}	External reset pulse width at power up	After supply voltage is valid	1	—	—	ms
T _{XRST2}	External reset pulse width after power up ^[17]	Applies after part has booted	10	—	—	μ s

Note

17. The minimum required XRES pulse length is longer when programming the device (see Table 19 on page 25).

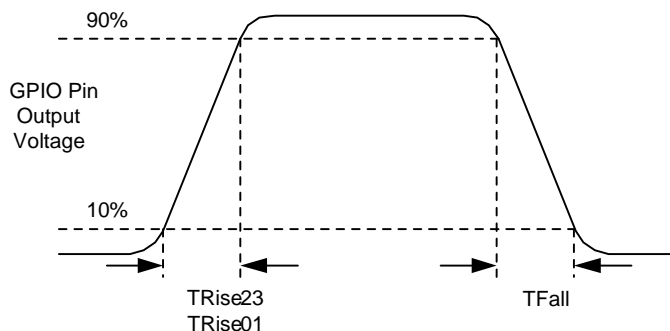
AC General Purpose IO Specifications

Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{GPIO}	GPIO operating frequency	Normal strong mode, port 0, 1	0	—	6 MHz for 1.71 V < V _{dd} < 2.4 V	MHz
			0	—	12 MHz for 2.4 V < V _{dd} < 3.6 V	
		Normal strong mode, Port 2, 3	0	—	3 MHz for 1.71 V < V _{dd} < 2.4 V	MHz
					6 MHz for 3.0 V < V _{dd} < 3.6 V	
TRise23	Rise time, strong mode, load = 50 pF Ports 2 or 3	V _{dd} = 3.0 to 3.6 V, 10% – 90%	15	—	80	ns
TRise23L	Rise time, strong mode low supply, load = 50 pF Ports 2 or 3	V _{dd} = 1.71 to 3.0 V, 10% – 90%	15	—	80	ns
TRise01	Rise time, strong mode, load = 50 pF Ports 0 or 1	V _{dd} = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	—	50	ns
TRise01L	Rise time, strong mode low supply, load = 50 pF Ports 0 or 1	V _{dd} = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	15	—	80	ns
TFall	Fall time, strong mode, load = 50 pF, All Ports	V _{dd} = 3.0 to 3.6 V, 10% – 90%	10	—	50	ns
TFallL	Fall time, strong mode low supply, load = 50 pF, all ports	V _{dd} = 1.71 to 3.0 V, 10% - 90%	10	—	70	ns

Figure 10. GPIO Timing Diagram



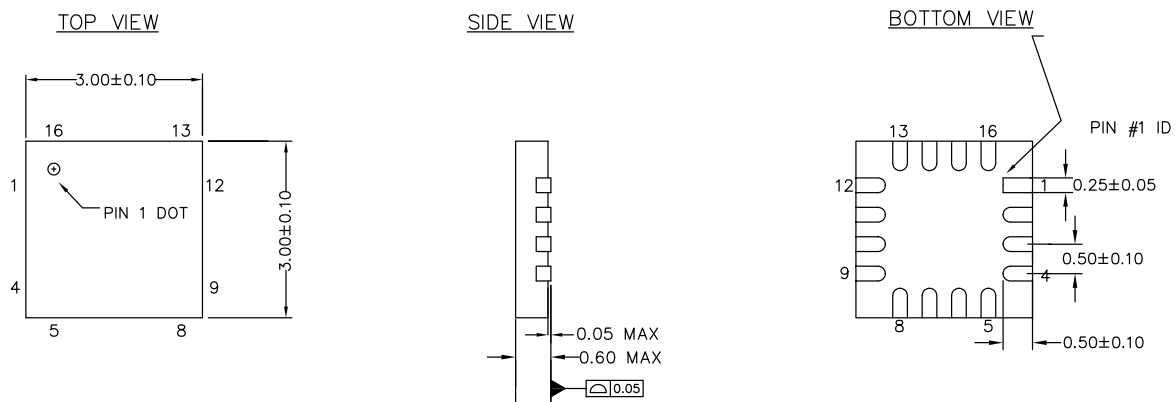
Package Diagram

This section illustrates the packaging specifications for the enCoRe V LV device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V LV emulation tools and their dimensions, refer to the development kit.

Packaging Dimensions

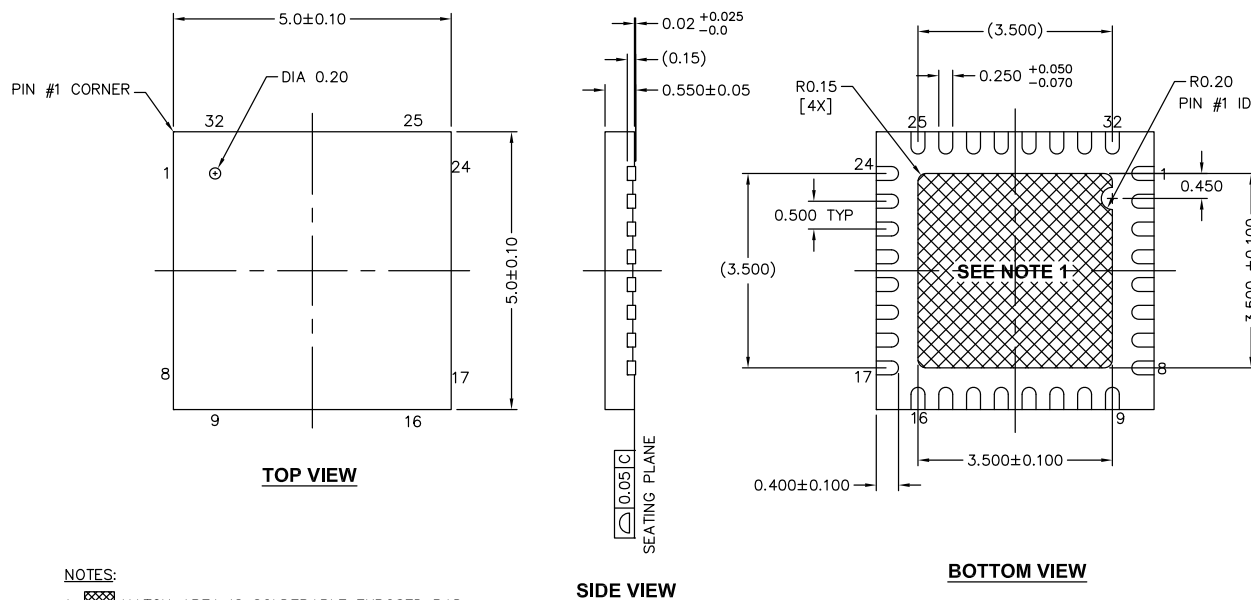
Figure 13. 16-pin Chip-On-Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116



NOTES

1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *1

Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168

NOTES:


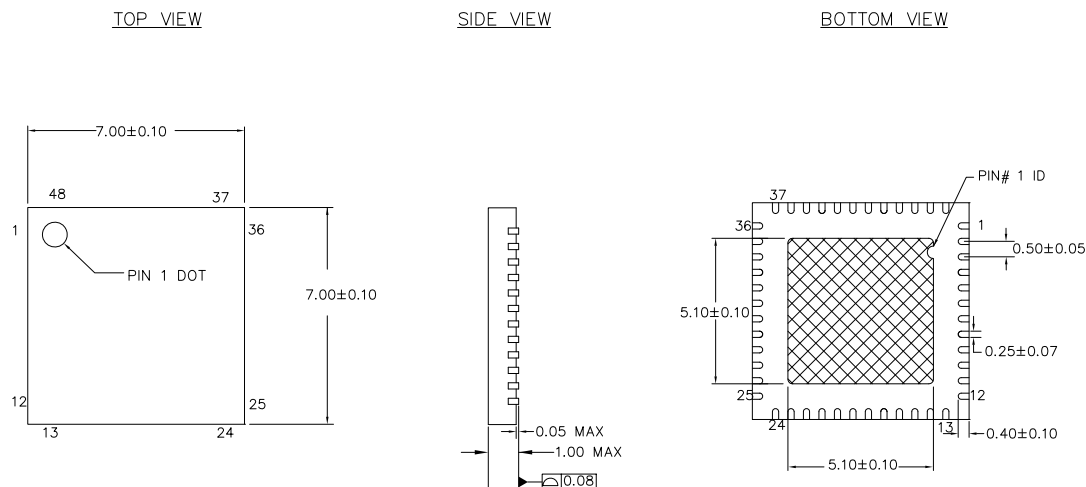

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

Figure 15. 48-pin QFN (7 × 7 × 1 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191

NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 23. Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake Temperature	–	125	See package label	°C
TBAKETIME	Bake Time	See package label	–	72	hours

Thermal Impedances

Package	Typical θ_{JA} ⁽¹⁹⁾
16 QFN	32.69 °C/W
32 QFN ⁽²⁰⁾	19.51 °C/W
48 QFN ⁽²⁰⁾	17.68 °C/W

Capacitance on Crystal Pins

Table 24. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 QFN	3.2 pF
48 QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature ⁽²¹⁾	Maximum Peak Temperature
16 QFN	240 °C	260 °C
32 QFN	240 °C	260 °C
48 QFN	240 °C	260 °C

Notes

19. $T_J = T_A + \text{Power} \times \theta_{JA}$.

20. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.

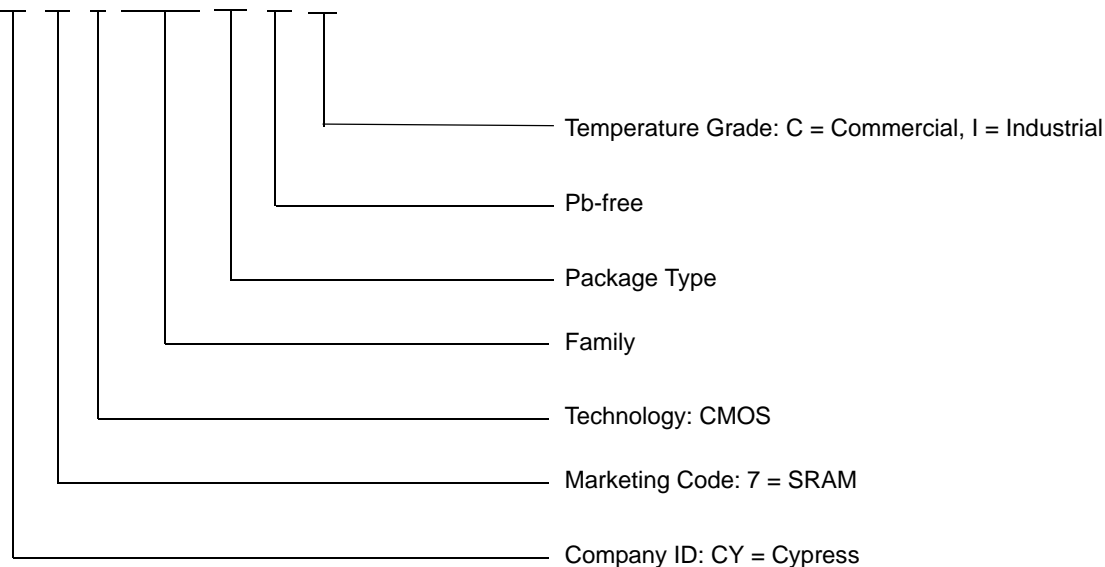
21. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

Ordering Code	Package Information	Flash	SRAM	No. of GPIOs	Target Applications
CY7C60413-16LKXC	16-Pin QFN (3x3 mm)	8 K	1 K	13	Feature-rich wireless mouse
CY7C60413-16LKXCT	16-Pin QFN - (Tape and Reel) (3X3 mm)	8 K	1 K	13	Feature-rich wireless mouse
CY7C60445-32LQXC	32-Pin QFN (5x5x0.55 mm)	16 K	1 K	28	Feature-rich wireless mouse
CY7C60445-32LQXCT	32-Pin QFN - (Tape and Reel) (5x5x0.55 mm)	16 K	1 K	28	Feature-rich wireless mouse
CY7C60455-48LTXC	48-Pin QFN (7x7x0.9 mm)	16 K	1 K	36	Mid-tier wireless keyboard
CY7C60455-48LTXCT	48-Pin QFN - (Tape and Reel) (7x7x0.9 mm)	16 K	1 K	36	Mid-tier wireless keyboard
CY7C60456-48LTXC	48-Pin QFN (7x7x0.9 mm)	32 K	2 K	36	Feature-rich wireless keyboard
CY7C60456-48LTXCT	48-Pin QFN - (Tape and Reel) (7x7x0.9 mm)	32 K	2 K	36	Feature-rich wireless keyboard

Ordering Code Definitions

CY 7 C XXXXX XX X CT



Document History Page

Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	626516	TYJ	See ECN	New data sheet
*A	735721	TYJ / ARI	See ECN	Added new block diagram, replaced TBDs, corrected values, updated pinout information, changed part number to reflect new specifications.
*B	1120504	ARI	See ECN	Corrected the description to pin 29 on Table 1, the Typ/Max values for I_{SB0} on the DC chip-level specifications, and the Min voltage value for $V_{ddIWRITE}$ in the DC Programming Specifications table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template.
*C	1225864	AESA / ARI	See ECN	Corrected the description to pin 13, 29 on Table 1 and 22,44 on Table 2. Added sections Register Reference, Register Conventions and Register Mapping Tables. Corrected Max values on the DC Chip-Level Specifications table.
*D	1446763	AESA	See ECN	Changed T_{ERASEB} parameter, max value to 18ms in Table 13, AC Programming Specification.
*E	1639963	AESA	See ECN	Post to www.cypress.com
*F	2138889	TYJ / PYRS	See ECN	Updated Ordering Code table: - Ordering code changed for 32-QFN package: From -32LKXC to -32LTXC - Added a new package type – “LTXC” for 48-QFN - Included Tape and Reel ordering code for 32-QFN and 48-QFN packages Changed active current values at 24, 12 and 6MHz in table “DC Chip-Level Specifications” - $IDD24$: 2.15 to 3.1mA - $IDD12$: 1.45 to 2.0mA - $IDD6$: 1.1 to 1.5mA Added information on using P1[0] and P1[1] as the I2C interface during POR or reset events

Document History Page (continued)

Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*G	2583853	TYJ / PYRS / HMT	10/10/08	<p>Converted from Preliminary to Final</p> <p>ADC resolution changed from 10-bit to 8-bit</p> <p>On Page1, SPI Master and Slave – speeds changed</p> <p>Rephrased battery monitoring clause in page 1 to include “with external components”</p> <p>Included ADC specifications table</p> <p>Voh5, Voh7, Voh9 specs changed</p> <p>Flash data retention – condition added to Note [15]</p> <p>Input leakage spec changed to 25 nA max</p> <p>Under AC Char, Frequency accuracy of ILO corrected</p> <p>GPIO rise time for ports 0,1 and ports 2,3 made common</p> <p>AC Programming specifications updated</p> <p>Included AC Programming cycle timing diagram</p> <p>AC SPI specification updated</p> <p>Spec change for 32-QFN package</p> <p>Input Leakage Current maximum value changed to 1 uA</p> <p>Maximum specification for V_{OH5A} parameter changed from 2.0 to 2.1V</p> <p>Minimum voltages for F_{SPIM} and F_{SPIS} specifications changed from 1.8V to 1.71V (Table 18)</p> <p>Updated V_{OHV} parameter in Table 13</p> <p>Updated Thermal impedance values for the packages - Table 20.</p> <p>Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs. Update maximum data in Table 12. DC POR and LVD Specifications.</p>
*H	2653717	DVJA / PYRS	02/04/09	<p>Changed master page from CY7C60445, CY7C6045X to CY7C604XX.</p> <p>Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections.</p> <p>Removed ‘GUI - graphical user interface’ from Document Conventions acronym table.</p> <p>Added Figure 1 and Table 1 (16-pin part information) to Pin Configurations section.</p> <p>Removed ‘O - Only a read/write register or bits’ in Table 4</p> <p>Edited Table 8: removed 10-bit resolution information and corrected units column.</p> <p>Added Figure 9 (16-pin part information) to Package Dimensions section.</p> <p>Added ‘Package Handling’ section.</p> <p>Added 8K part ‘CY7C60413-16LKXC’ to Ordering Information.</p>
*I	2714694	DVJA / AESA	06/04/2009	<p>Updated Block Diagram.</p> <p>Added 10-bit ADC, SPI, and I2C Slave sections.</p> <p>ADC Resolution changed from 8-bit to 10-bit</p> <p>Updated Figure 9: 5.7 MHz minimum CPU frequency</p> <p>Updated Table 15 AC Chip Level Specs</p> <p>Figure 8: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz</p>
*J	2764460	DVJA / AESA	09/15/2009	<p>Added footnote #5 to Table 10: DC Chip Level Specs</p> <p>Added F_{32K2} (Untrimmed) spec to Table 17: AC Chip level Specs</p> <p>Changed T_{RAMP} spec to SR_{POWER_UP} in Table 17: AC Chip Level Specs</p> <p>Changed Table 14: ADC Specs</p> <p>Added Table 25: Typical Package Capacitance on Crystal Pins</p>
*K	2811903	DVJA	11/23/2009	Added Note 6 on page 18. Changed V_{IHP} in Table 15 on page 22
*L	3075921	NXZ	11/01/2010	Added Ordering Code Definition.
*M	3283876	DIVA	06/15/2011	Updated Getting Started , Development Tools , and Designing with PSoC Designer .

Document History Page (continued)

Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*N	3980412	CSAI	04/24/2013	Updated Packaging Dimensions : spec 001-09116 – Changed revision from *E to *H. spec 001-42168 – Changed revision from *D to *E. spec 001-13191 – Changed revision from *E to *G. Added Errata .
*O	4074141	CSAI	07/23/2013	Added Errata footnote (Note 7). Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC General Purpose I/O Specifications [7] : Added Note 7 and referred the same note in the heading. Updated Errata . Updated in new template.
*P	4189348	CSAI	11/12/2013	Updated Packaging Dimensions : spec 001-09116 – Changed revision from *H to *I. Completing Sunset Review.