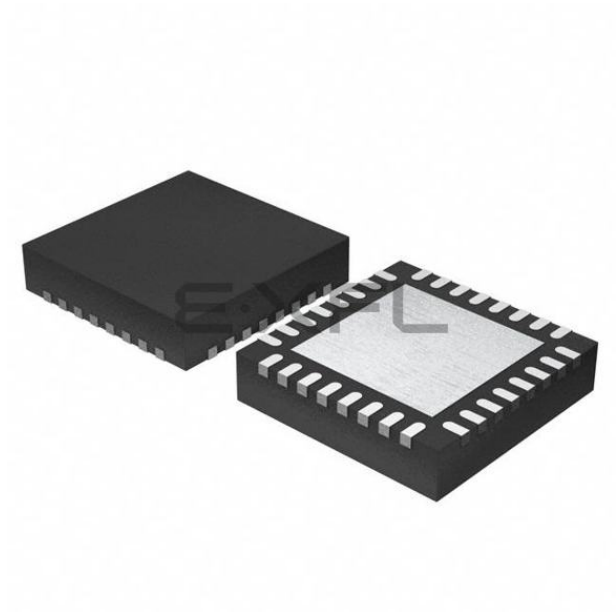

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

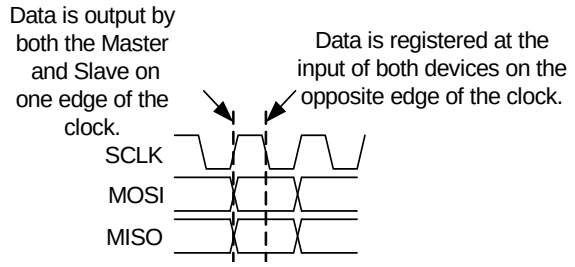
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c60445-32lqxct

SPI

The serial peripheral interconnect (SPI) 3-wire protocol uses both edges of the clock to enable synchronous communication without the need for stringent setup and hold requirements.

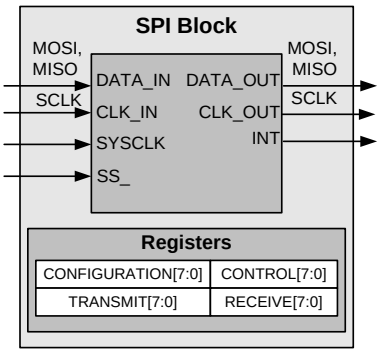
Figure 2. Basic SPI Configuration



A device can be a master or slave. A master outputs clock and data to the slave device and inputs slave data. A slave device inputs clock and data from the master device and outputs data for input to the master. Together, the master and slave are essentially a circular Shift register, where the master generates the clocking and initiates data transfers.

A basic data transfer occurs when the master sends eight bits of data, along with eight clocks. In any transfer, both master and slave transmit and receive simultaneously. If the master only sends data, the received data from the slave is ignored. If the master wishes to receive data from the slave, the master must send dummy bytes to generate the clocking for the slave to send data back.

Figure 3. SPI Block Diagram



SPI configuration register (SPI_CFG) sets master/slave functionality, clock speed and interrupt select. SPI control register (SPI_CR) provides four control bits and four status bits for device interfacing and synchronization.

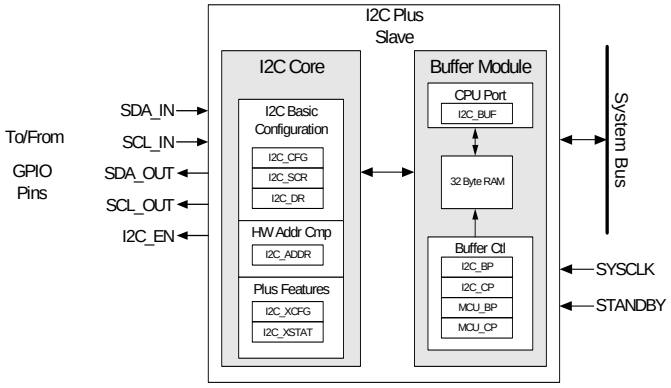
The SPIM hardware has no support for driving the Slave Select (SS_) signal. The behavior and use of this signal is application and enCoRe V device dependent and, if required, must be implemented in firmware.

There is an additional data input in the SPIS, Slave Select (SS_), which is an active low signal. SS_ must be asserted to enable the SPIS to receive and transmit. SS_ has two high level functions: 1) To allow for the selection of a given slave in a multi-slave environment, and 2) To provide additional clocking for TX data queuing in SPI modes 0 and 1.

I²C Slave

The I²C slave enhanced communications block is a serial-to-parallel processor, designed to interface the enCoRe V LV device to a two-wire I²C serial communications bus. To eliminate the need for excessive CPU intervention and overhead, the block provides I²C-specific support for status detection and generation of framing bits. By default, the I²C Slave Enhanced module is firmware compatible with the previous generation of I²C slave functionality. However, this module provides new features that are configurable to implement significant flexibility for both internal and external interfacing.

Figure 4. I²C Block Diagram



The basic I²C features include:

- Slave, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for clock rates of up to 400 kHz
- 7- or 10-bit addressing (through firmware support)
- SMBus operation (through firmware support)

Enhanced features of the I²C Slave Enhanced Module include:

- Support for 7-bit hardware address compare
- Flexible data buffering schemes
- A 'no bus stalling' operating mode
- A low power bus monitoring mode

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V LV CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource:

- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- The 3.6 V maximum input, 1.8, 2.5, or 3 V selectable output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V LV family of parts.

Getting Started

The quickest way to understanding the enCoRe V silicon is by reading this datasheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer to the *PSoC Programmable System-on-Chip Technical Reference Manual*, for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, reference the latest enCoRe V device datasheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select user modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Table 3. 48-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
22	IOHR	P1[0][1,2]	Digital I/O, ISSP DATA, I2C SDA, SPI CLK
23	IOHR	P1[2]	Digital I/O
24	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	IOHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull-down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	IOH	P0[0]	Digital I/O
38	IOH	P0[2]	Digital I/O
39	IOH	P0[4]	Digital I/O
40	IOH	P0[6]	Digital I/O
41	Power	Vdd	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	IOH	P0[7]	Digital I/O
45	IOH	P0[5]	Digital I/O
46	IOH	P0[3]	Digital I/O
47	Power	Vss	Supply ground
48	IOH	P0[1]	Digital I/O
CP	Power	Vss	Center pad must be connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Register Reference

The section discusses the registers of the enCoRe V LV device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V LV device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the ‘extended’ address space or the ‘configuration’ registers.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature[3]	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
Vdd	Supply voltage relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC input voltage		Vss – 0.5	–	Vdd + 0.5	V
V_{IOZ}	DC voltage applied to tristate		Vss –0.5	–	Vdd + 0.5	V
I_{MIO}	Maximum current into any Port pin		–25	–	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	–	–	V
LU	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{AC}	Ambient commercial temperature		0		+70	°C
T_{JC}	Operational commercial die temperature[4]	The temperature rise from ambient to junction is package specific. Refer the table "Thermal Impedances" on page 30. The user must limit the power consumption to comply with this requirement.	0		+85	°C

Notes

3. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
4. The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 30. The user must limit the power consumption to comply with this requirement.

Table 11. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	IOH < 10 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	IOH = 0.2 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.4	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH < 10 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.5	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH < 10 µA, Vdd > 2.4V, maximum of 20 mA source current in all I/Os.	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH = 1 mA, Vdd > 2.4V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	1.4	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	0.001	1	µA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.5	1.7	5	pF

Table 12. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	IOH = 10 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	IOH = 0.5 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.5	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 100 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.5	–	–	V
V_{OL}	Low output voltage	IOL = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.4	V
V_{IL}	Input low voltage	–	–	–	0.3 x Vdd	V
V_{IH}	Input high voltage	–	0.65 x Vdd	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	0.001	1	µA
C_{PIN}	Capacitive load on pins	Package and pin dependent. Temp = 25 ° C	0.5	1.7	5	pF

DC POR and LVD Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units
	Vdd Value for PPOR Trip[8]				
V_{PPOR0}	PORLEV[1:0] = 00b, HPOR = 0	1.61	1.66	1.71	V
V_{PPOR1}	PORLEV[1:0] = 00b, HPOR = 1		2.36	2.41	V
V_{PPOR2}	PORLEV[1:0] = 01b, HPOR = 1		2.60	2.66	V
V_{PPOR3}	PORLEV[1:0] = 10b, HPOR = 1		2.82	2.95	V
	Vdd Value for LVD Trip				
V_{LVD0}	VM[2:0] = 000b[9]	2.40	2.45	2.51	V
V_{LVD1}	VM[2:0] = 001b[10]	2.64	2.71	2.78	V
V_{LVD2}	VM[2:0] = 010b[11]	2.85	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b	2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b	3.06	3.13	3.20	V
V_{LVD5}	VM[2:0] = 101b	1.84	1.9	2.32	V
V_{LVD6}	VM[2:0] = 110b[12]	1.75	1.8	1.84	V

DC Programming Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply voltage for flash write operations	1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	–	–	V_{IL}[11]	V
V_{IHP}	Input high voltage during programming or verify	1.71	–	Vdd_{IWRITE} +0.3	V
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify[13]	–	–	0.2	mA
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify[13]	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify	–	–	Vss + 0.75	V
V_{OHP}	Output high voltage during programming or verify	Vdd_{IWRITE} - 0.9 V	–	Vdd_{IWRITE}	V
$Flash_{ENPB}$	Flash write endurance[15]	50,000	–	–	Cycles
$Flash_{DR}$	Flash data retention[16]	10	20	–	Years

Notes
8. Vdd must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.
9. Always greater than 50 mV above V_{PPOR1} for falling supply.
10. Always greater than 50 mV above V_{PPOR2} for falling supply.
11. Always greater than 50 mV above V_{PPOR3} for falling supply.
12. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.
13. Driving internal pull-down resistor.
14. See appropriate DC General Purpose I/O Specifications [7] table.
15. Erase/write cycles per block.
16. Following maximum Flash write cycles at Tamb = 55C and Tj = 70C.

AC Electrical Characteristics

AC Chip Level Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	Processing frequency		5.7	–	25.2	MHz
F_{32K1}	Internal low speed oscillator frequency	Trimmed for 3.3 V operation using factory trim values	19	32	50	kHz
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency)	–	13	32	82	kHz
F_{32K2}	Internal low speed oscillator frequency	Untrimmed	13	32	82	kHz
F_{IMO24}	Internal main oscillator stability for 24 MHz ± 5%	–	22.8	24	25.2	MHz
F_{IMO12}	Internal main oscillator stability for 12 MHz	–	11.4	12	12.6	MHz
F_{IMO6}	Internal main oscillator stability for 6 MHz	–	5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO	–	40	50	60	%
DC_{ILO}	Internal low speed oscillator duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	–	–	–	250	V/ms
T_{XRST}	External reset pulse width at power up	After supply voltage is valid	1	–	–	ms
T_{XRST2}	External reset pulse width after power up[17]	Applies after part has booted	10	–	–	µs

Note
17. The minimum required XRES pulse length is longer when programming the device (see Table 19 on page 25).

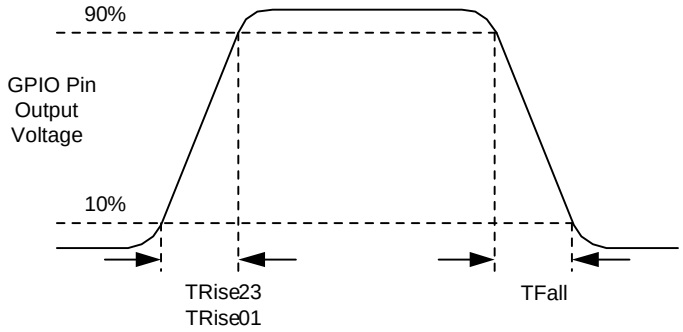
AC General Purpose IO Specifications

Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, port 0, 1	0 0	– –	6 MHz for 1.71 V < Vdd < 2.4 V 12 MHz for 2.4 V < Vdd < 3.6 V	MHz
		Normal strong mode, Port 2, 3	0	–	3 MHz for 1.71 V < Vdd < 2.4 V 6 MHz for 3.0 V< Vdd < 3.6 V	MHz
TRise23	Rise time, strong mode, cload = 50 pF Ports 2 or 3	Vdd = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
TRise23L	Rise time, strong mode low supply, cload = 50 pF Ports 2 or 3	Vdd = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
TRise01	Rise time, strong mode, cload = 50 pF Ports 0 or 1	Vdd = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	– –	50	ns
TRise01L	Rise time, strong mode low supply, cload = 50 pF Ports 0 or 1	Vdd = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	15	–	80	ns
TFall	Fall time, strong mode, cload = 50 pF, All Ports	Vdd = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
TFallL	Fall time, strong mode low supply, cload = 50 pF, all ports	Vdd = 1.71 to 3.0 V, 10% - 90%	10	–	70	ns

Figure 10. GPIO Timing Diagram



AC External Clock Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	–	0.750	–	25.2	MHz
–	High period	–	20.6	–	5300	ns
–	Low period	–	20.6	–	–	ns
–	Power up IMO to switch	–	150	–	–	µs

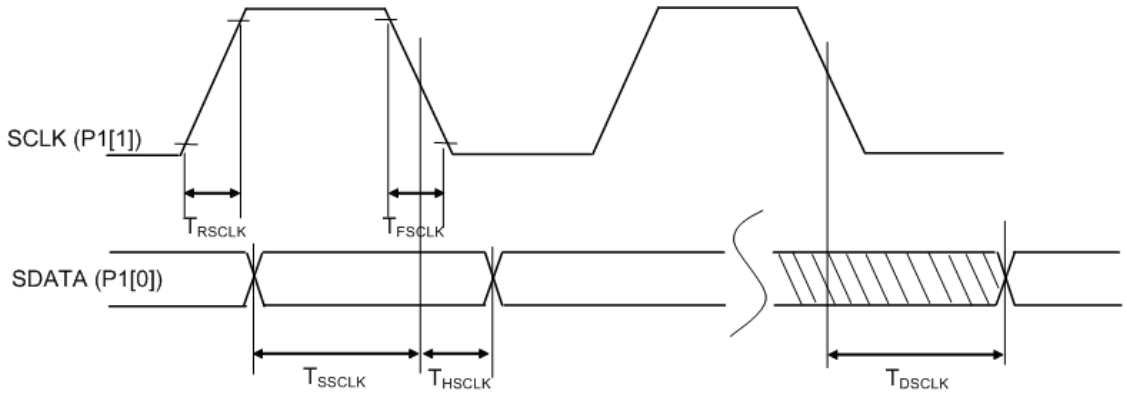
AC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
T_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
T_{SSCLK}	Data set up time to falling edge of SCLK	–	40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
T_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
T_{WRITE}	Flash block write time	–	–	–	25	ms
T_{DSCLK1}	Data out delay from falling edge of SCLK	3.0 V < Vdd < 3.6 V	–	–	85	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	1.71 V < Vdd < 3.0 V	–	–	130	ns
T_{XRST3}	External reset pulse width after power up	Required to enter programming mode when coming out of sleep	263	–	–	µs

Figure 11. Timing Diagram - AC Programming Cycle



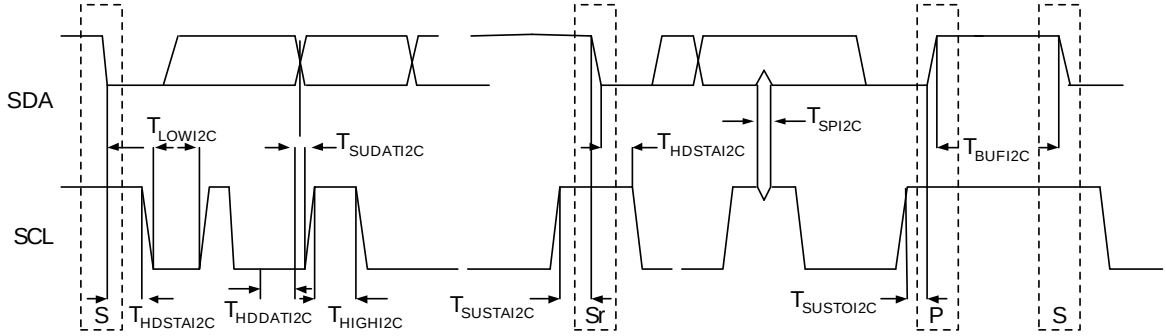
AC I²C Specifications

Table 20 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[18]	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 12. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

18. A fast mode I2C bus device can be used in a standard mode I2C bus system, but the requirement $t_{SU;DAT}$ Š 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard mode I2C bus specification) before the SCL line is released.

Table 21. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	–	–	6 3	MHz
DC	SCLK duty cycle	–	–	50	–	%
T_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	60 100	–	–	ns
T_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
T_{OUT_HIGH}	MOSI high time	–	40	–	–	ns

Table 22.SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	–	–	12 6	MHz
T_{LOW}	SCLK low time	–	41.67	–	–	ns
T_{HIGH}	SCLK high time	–	41.67	–	–	ns
T_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
T_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
T_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
T_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
T_{SS_HIGH}	SS high time	–	–	–	50	ns
T_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
T_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 23.Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake Temperature	–	125	See package label	°C
TBAKETIME	Bake Time	See package label	–	72	hours

Thermal Impedances

Package	Typical θ_{JA} (19)
16 QFN	32.69 °C/W
32 QFN(20)	19.51 °C/W
48 QFN(20)	17.68 °C/W

Capacitance on Crystal Pins

Table 24. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 QFN	3.2 pF
48 QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

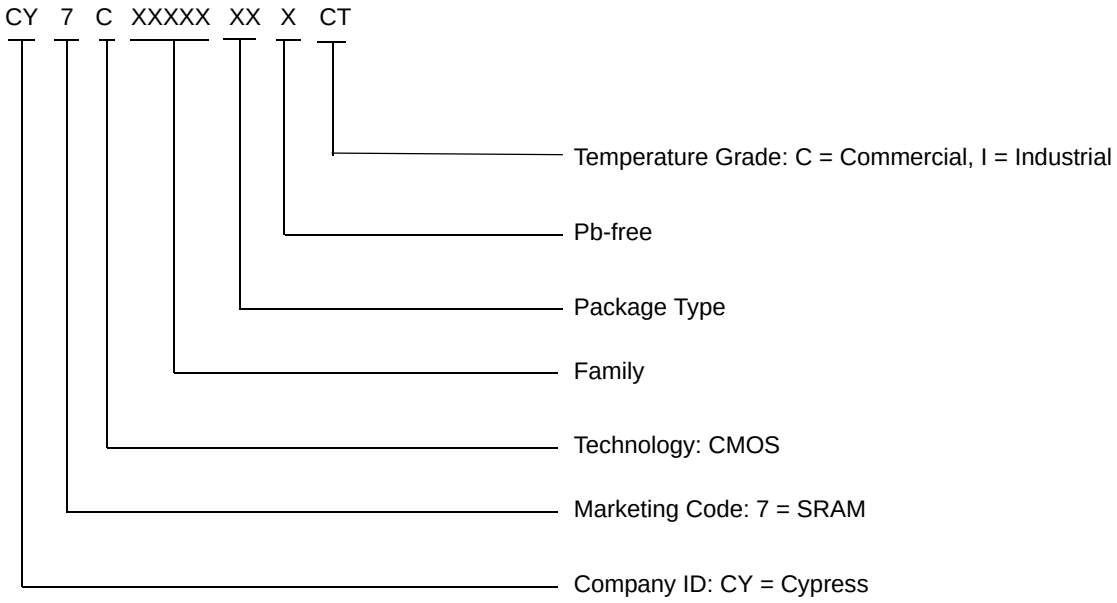
Package	Minimum Peak Temperature(21)	Maximum Peak Temperature
16 QFN	240 °C	260 °C
32 QFN	240 °C	260 °C
48 QFN	240 °C	260 °C

Notes
19. $T_J = T_A$ + Power x θ_{JA}.
20. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.
21. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

Ordering Code	Package Information	Flash	SRAM	No. of GPIOs	Target Applications
CY7C60413-16LKXC	16-Pin QFN (3x3 mm)	8 K	1 K	13	Feature-rich wireless mouse
CY7C64013-16LKXCT	16-Pin QFN - (Tape and Reel) (3X3 mm)	8 K	1 K	13	Feature-rich wireless mouse
CY7C60445-32LQXC	32-Pin QFN (5x5x0.55 mm)	16 K	1 K	28	Feature-rich wireless mouse
CY7C60445-32LQXCT	32-Pin QFN - (Tape and Reel) (5x5x0.55 mm)	16 K	1 K	28	Feature-rich wireless mouse
CY7C60455-48LTXC	48-Pin QFN (7x7x0.9 mm)	16 K	1 K	36	Mid-tier wireless keyboard
CY7C60455-48LTXCT	48-Pin QFN - (Tape and Reel) (7x7x0.9 mm)	16 K	1 K	36	Mid-tier wireless keyboard
CY7C60456-48LTXC	48-Pin QFN (7x7x0.9 mm)	32 K	2 K	36	Feature-rich wireless keyboard
CY7C60456-48LTXCT	48-Pin QFN - (Tape and Reel) (7x7x0.9 mm)	32 K	2 K	36	Feature-rich wireless keyboard

Ordering Code Definitions



Acronyms

The following table lists the acronyms that are used in this document.

Acronym	Description
API	application programming interface
CPU	central processing unit
GPIO	general purpose IO
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least significant bit
LVD	low voltage detect
MSb	most significant bit
POR	power on reset
PPOR	precision power on reset
PSoC	Programmable System-on-Chip
SLIMO	slow IMO
SRAM	static random access memory

Document Conventions

Units of Measure

The following table lists the units of measure that are used in this document.

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolts
µVrms	microvolts root-mean-square
µW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volts

Errata

This section describes the errata for the enCoRe V – CY7C643xx and enCoRe V LV – CY7C604xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY7C604xx Errata Summary

The following Errata item applies to the **CY7C643xx** and **CY7C604xx** data sheets.

1. Latch up susceptibility when maximum I/O sink current exceeded

- **PROBLEM DEFINITION**
  P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.
- **PARAMETERS AFFECTED**
  LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.
- **TRIGGER CONDITIONS**
  Latch up occurs when both the following conditions are met:
  A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.
  B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below Vss (signal undershoot) and a current greater than 200 mA to flow out of the pin.
- **SCOPE OF IMPACT**
  The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx and CY7C604xx data sheets.
- **WORKAROUND**
  Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.
- **FIX STATUS**
  This issue will be corrected in the next new silicon revision.

Document History Page (continued)

Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	2583853	TYJ / PYRS / HMT	10/10/08	Converted from Preliminary to Final ADC resolution changed from 10-bit to 8-bit On Page1, SPI Master and Slave – speeds changed Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Voh5, Voh7, Voh9 specs changed Flash data retention – condition added to Note [15] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 uA Maximum specification for V_{OH5A} parameter changed from 2.0 to 2.1V Minimum voltages for F_{SPIM} and F_{SPIS} specifications changed from 1.8V to 1.71V (Table 18) Updated V_{OHV} parameter in Table 13 Updated Thermal impedance values for the packages - Table 20. Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs. Update maximum data in Table 12. DC POR and LVD Specifications.
*H	2653717	DVJA / PYRS	02/04/09	Changed master page from CY7C60445, CY7C6045X to CY7C604XX. Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections. Removed ‘GUI - graphical user interface’ from Document Conventions acronym table. Added Figure 1 and Table 1 (16-pin part information) to Pin Configurations section. Removed ‘O - Only a read/write register or bits’ in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added Figure 9 (16-pin part information) to Package Dimensions section. Added ‘Package Handling’ section. Added 8K part ‘CY7C60413-16LKXC’ to Ordering Information.
*I	2714694	DVJA / AESA	06/04/2009	Updated Block Diagram. Added 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Figure 9: 5.7 MHz minimum CPU frequency Updated Table 15 AC Chip Level Specs Figure 8: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz
*J	2764460	DVJA / AESA	09/15/2009	Added footnote #5 to Table 10: DC Chip Level Specs Added F_{32K2} (Untrimmed) spec to Table 17: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 17: AC Chip Level Specs Changed Table 14: ADC Specs Added Table 25: Typical Package Capacitance on Crystal Pins
*K	2811903	DVJA	11/23/2009	Added Note 6 on page 18. Changed V_{IHP} in Table 15 on page 22
*L	3075921	NXZ	11/01/2010	Added Ordering Code Definition.
*M	3283876	DIVA	06/15/2011	Updated Getting Started, Development Tools, and Designing with PSoC Designer.

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