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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c60455-48ltxc

Functional Overview

The enCoRe V LV family of devices are designed to replace multiple traditional low voltage microcontroller system components with one, low cost single chip programmable component. Communication peripherals (I²C/SPI), a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in [enCoRe V LV Block Diagram](#), is comprised of two main areas: the CPU core and the system resources. Depending on the enCoRe V LV package, up to 36 GPIO are also included.

Enhancements over the Cypress's legacy low-voltage microcontrollers include faster CPU at lower voltage operation, lower current consumption, twice the RAM and flash, hot-swappable I/Os, I²C hardware address recognition, new very low-current sleep mode, and new package options.

The enCoRe V LV Core

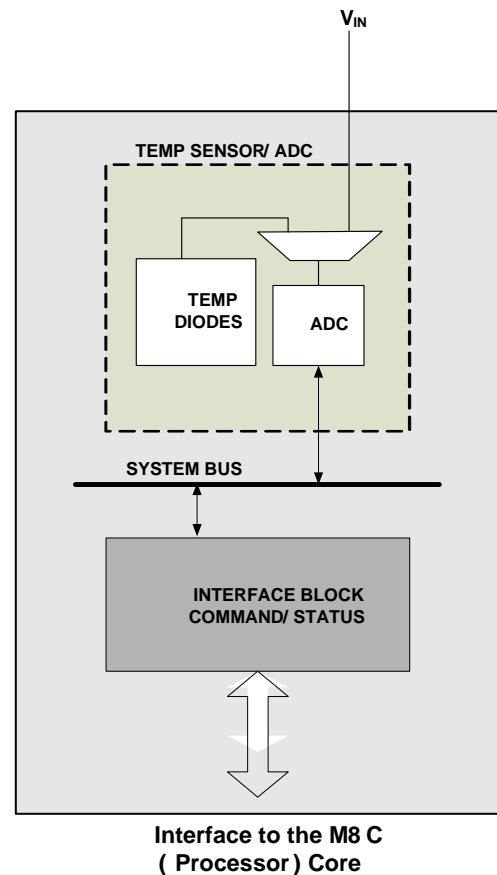
The enCoRe V LV Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low-speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as a configurable I²C slave and SPI master-slave communication interface and various system resets supported by the M8C.

10-bit ADC

The ADC on enCoRe V LV device is an independent block with a state machine interface to control accesses to the block. The ADC is housed together with the temperature sensor core and can be connected to this or the Analog Mux Bus. As a default operation, the ADC is connected to the temperature sensor diodes to give digital values of the temperature.

Figure 1. ADC System Performance Block Diagram



The ADC User Module contains an integrator block and one comparator with positive and negative input set by the MUXes. The input to the integrator stage comes from the Analog Global Input Mux or the temperature sensor with an input voltage range of 0 V to 1.3 V, where 1.3 V is 72% of full scale.

In the ADC only configuration (the ADC MUX selects the Analog Mux Bus, not the default temperature sensor connection), an external voltage can be connected to the input of the modulator for voltage conversion. The ADC is run for a number of cycles set by the timer, depending upon the resolution of the ADC desired by the user. A counter counts the number of trips by the comparator, which is proportional to the input voltage. The Temp Sensor block clock speed is 36 MHz and is divided down to 1 to 12 MHz for ADC operation.

The basic I²C features include:

- *Slave, transmitter, and receiver operation
- *Byte processing for low CPU overhead
- *Interrupt or polling CPU interface
- *Support for clock rates of up to 400 kHz
- *7- or 10-bit addressing (through firmware support)
- *SMBus operation (through firmware support)

Enhanced features of the I²C Slave Enhanced Module include:

- *Support for 7-bit hardware address compare
- *Flexible data buffering schemes
- *A 'no bus stalling' operating mode
- *A low power bus monitoring mode

The I²C block controls the data (SDA) and the clock (SCL) to the external I²C interface through direct connections to two dedicated GPIO pins. When I²C is enabled, these GPIO pins are not available for general purpose use. The enCoRe V LV CPU firmware interacts with the block through I/O register reads and writes, and firmware synchronization is implemented through polling and/or interrupts.

In the default operating mode, which is firmware compatible with previous versions of I²C slave modules, the I²C bus is stalled upon every received address or byte, and the CPU is required to read the data or supply data as required before the I²C bus continues. However, this I²C Slave Enhanced module provides new data buffering capability as an enhanced feature. In the EZI²C buffering mode, the I²C slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave never stalls the bus. In this protocol, the data available in the RAM (this is managed by the CPU) is valid.

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The following statements describe the merits of each system resource:

- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- The 3.6 V maximum input, 1.8, 2.5, or 3 V selectable output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the enCoRe V LV family of parts.

Getting Started

The quickest way to understanding the enCoRe V silicon is by reading this datasheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer to the *PSoC Programmable System-on-Chip Technical Reference Manual*, for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, reference the latest enCoRe V device datasheets on the web at <http://www.cypress.com>.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Table 2. 32-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
28	Power	Vdd	Supply voltage
29	IOH	P0[7]	Digital I/O
30	IOH	P0[5]	Digital I/O
31	IOH	P0[3]	Digital I/O
32	Power	Vss	Ground connection
CP	Power	Vss	Center pad must be connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Table 3. 48-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
22	IOHR	P1[0] ^(1,2)	Digital I/O, ISSP DATA, I2C SDA, SPI CLK
23	IOHR	P1[2]	Digital I/O
24	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	IOHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull-down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	IOH	P0[0]	Digital I/O
38	IOH	P0[2]	Digital I/O
39	IOH	P0[4]	Digital I/O
40	IOH	P0[6]	Digital I/O
41	Power	Vdd	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	IOH	P0[7]	Digital I/O
45	IOH	P0[5]	Digital I/O
46	IOH	P0[3]	Digital I/O
47	Power	Vss	Supply ground
48	IOH	P0[1]	Digital I/O
CP	Power	Vss	Center pad must be connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
	02			42			82			C2	
	03			43			83			C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45			85			C5	
	06			46			86			C6	
	07			47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
PRT4DM0	10	RW		50			90			D0	
PRT4DM1	11	RW		51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C		IO_CFG	DC	RW
	1D			5D			9D		OUT_P1	DD	RW
	1E			5E			9E			DE	
	1F			5F			9F			DF	
	20			60			A0		OSC_CR0	E0	RW
	21			61			A1		ECO_CFG	E1	#
	22			62			A2		OSC_CR2	E2	RW
	23			63			A3		VLT_CR	E3	RW
	24			64			A4		VLT_CMP	E4	R
	25			65			A5			E5	
	26			66			A6			E6	
	27			67			A7			E7	
	28			68			A8		IMO_TR	E8	W
SPI_CFG	29	RW		69			A9		ILO_TR	E9	W
	2A			6A			AA			EA	
	2B			6B			AB		SLP_CFG	EB	RW
	2C		TMP_DR0	6C	RW		AC		SLP_CFG2	EC	RW
	2D		TMP_DR1	6D	RW		AD		SLP_CFG3	ED	RW
	2E		TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70			B0			F0	
	31			71			B1			F1	
	32			72			B2			F2	
	33			73			B3			F3	
	34			74			B4			F4	
	35			75			B5			F5	
	36			76			B6			F6	
	37			77			B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE			FE	
	3F			7F			BF			FF	

Gray fields are reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe V LV devices. For the most up to date electrical specifications, verify that you have the most recent datasheet available by visiting the company web site at <http://www.cypress.com>.

Figure 8. Voltage versus CPU Frequency

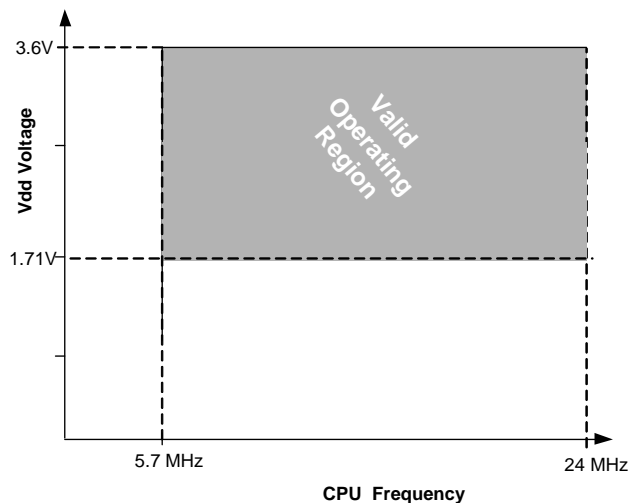
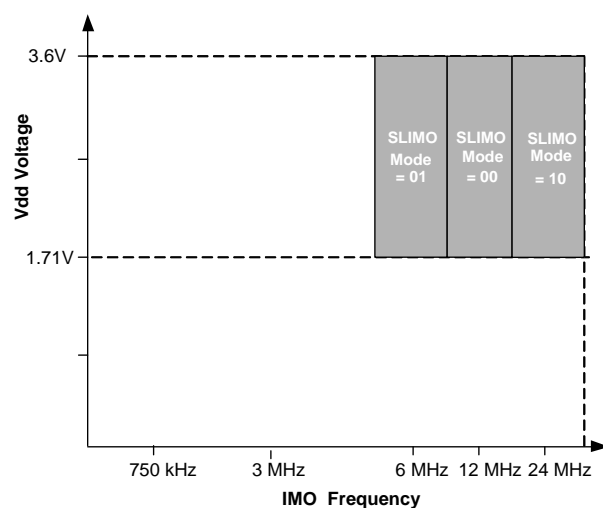


Figure 9. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{STG}	Storage temperature ^[3]	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	–55	+25	+125	°C
V _{DD}	Supply voltage relative to V _{SS}		–0.5	–	+6.0	V
V _{IO}	DC input voltage		V _{SS} – 0.5	–	V _{DD} + 0.5	V
V _{IOZ}	DC voltage applied to tristate		V _{SS} – 0.5	–	V _{DD} + 0.5	V
I _{MIO}	Maximum current into any Port pin		–25	–	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	–	–	V
LU	Latch up current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{AC}	Ambient commercial temperature		0		+70	°C
T _{JC}	Operational commercial die temperature ^[4]	The temperature rise from ambient to junction is package specific. Refer the table “ Thermal Impedances ” on page 30. The user must limit the power consumption to comply with this requirement.	0		+85	°C

Notes

3. Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
4. The temperature rise from ambient to junction is package specific. See [Thermal Impedances on page 30](#). The user must limit the power consumption to comply with this requirement.

DC General Purpose I/O Specifications ^[7]

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 1.71 V to 3.6 V and $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. Typical parameters apply to 3.3 V at 25°C . These are for design guidance only.

Table 10. 3.0 V to 3.6 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor	–	4	5.6	8	k Ω
V _{OH1}	High output voltage Port 2 or 3 pins	IOH \leq 10 μA , maximum of 10 mA source current in all I/Os	V _{DD} – 0.2	–	–	V
V _{OH2}	High output voltage Port 2 or 3 pins	IOH = 1 mA, maximum of 20 mA source current in all I/Os	V _{DD} – 0.9	–	–	V
V _{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH < 10 μA , maximum of 10 mA source current in all I/Os	V _{DD} – 0.2	–	–	V
V _{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 5 mA, maximum of 20 mA source current in all I/Os	V _{DD} – 0.9	–	–	V
V _{OH5}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	IOH < 10 μA , V _{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.3	V
V _{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	IOH = 5 mA, V _{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V _{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	IOH < 10 μA , V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V _{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	IOH = 2 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V _{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH < 10 μA , V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.1	V
V _{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH = 1 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low output voltage	IOL = 25 mA, V _{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input low voltage	–	–	–	0.80	V
V _{IH}	Input high voltage	–	2.00	–	–	V
V _H	Input hysteresis voltage	–	–	80	–	mV
I _{IL}	Input leakage (absolute value)	–	–	0.001	1	μA
C _{PIN}	Pin capacitance	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Note

7. **Errata:** P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins. Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits. For more information please refer to "Errata" on page 33.

ADC Electrical Specifications

Table 13.ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	V_{REFADC}	V
C_{IIN}	Input capacitance	–		–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500fF \times \text{data clock})$	$1/(400fF \times \text{data clock})$	$1/(300fF \times \text{data clock})$	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data Clock set to 6 MHz. Sample Rate = $0.001/(2^{\text{Resolution}}/\text{Data Clock})$	–	–	–	ksps
S10	10-bit sample rate	Data Clock set to 6 MHz. Sample Rate = $0.001/(2^{\text{Resolution}}/\text{Data Clock})$	–	5.859	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR ($V_{dd} > 3.0\text{ V}$)	–	24	–	dB
		PSRR ($V_{dd} < 3.0\text{ V}$)	–	30	–	dB

DC POR and LVD Specifications

Table 14 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units
V _{PPOR0}	Vdd Value for PPOR Trip ⁽⁸⁾ PORLEV[1:0] = 00b, HPOR = 0	1.61	1.66	1.71	V
V _{PPOR1}	PORLEV[1:0] = 00b, HPOR = 1		2.36	2.41	V
V _{PPOR2}	PORLEV[1:0] = 01b, HPOR = 1		2.60	2.66	V
V _{PPOR3}	PORLEV[1:0] = 10b, HPOR = 1		2.82	2.95	V
V _{LVD0}	Vdd Value for LVD Trip VM[2:0] = 000b ⁽⁹⁾	2.40	2.45	2.51	V
V _{LVD1}	VM[2:0] = 001b ⁽¹⁰⁾	2.64	2.71	2.78	V
V _{LVD2}	VM[2:0] = 010b ⁽¹¹⁾	2.85	2.92	2.99	V
V _{LVD3}	VM[2:0] = 011b	2.95	3.02	3.09	V
V _{LVD4}	VM[2:0] = 100b	3.06	3.13	3.20	V
V _{LVD5}	VM[2:0] = 101b	1.84	1.9	2.32	V
V _{LVD6}	VM[2:0] = 110b ⁽¹²⁾	1.75	1.8	1.84	V

DC Programming Specifications

Table 15 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units
V _{ddIWRITE}	Supply voltage for flash write operations	1.71	—	5.25	V
I _{DDP}	Supply current during programming or verify	—	5	25	mA
V _{ILP}	Input low voltage during programming or verify	—	—	V _{IL} ^[11]	V
V _{IHP}	Input high voltage during programming or verify	1.71	—	V _{ddIWRITE} + 0.3	V
I _{ILP}	Input current when applying V _{ilp} to P1[0] or P1[1] during programming or verify ⁽¹³⁾	—	—	0.2	mA
I _{IHP}	Input current when applying V _{ihp} to P1[0] or P1[1] during programming or verify ⁽¹³⁾	—	—	1.5	mA
V _{OLP}	Output low voltage during programming or verify	—	—	V _{ss} + 0.75	V
V _{OHP}	Output high voltage during programming or verify	V _{ddIWRITE} - 0.9 V	—	V _{ddIWRITE}	V
Flash _{ENPB}	Flash write endurance ⁽¹⁵⁾	50,000	—	—	Cycles
Flash _{DR}	Flash data retention ⁽¹⁶⁾	10	20	—	Years

Notes

8. Vdd must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.
9. Always greater than 50 mV above V_{PPOR1} for falling supply.
10. Always greater than 50 mV above V_{PPOR2} for falling supply.
11. Always greater than 50 mV above V_{PPOR3} for falling supply.
12. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.
13. Driving internal pull-down resistor.
14. See appropriate [DC General Purpose I/O Specifications \[7\]](#) table.
15. Erase/write cycles per block.
16. Following maximum Flash write cycles at Tamb = 55C and Tj = 70C.

AC Electrical Characteristics

AC Chip Level Specifications

Table 16 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16. AC Chip Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{CPU}	Processing frequency		5.7	—	25.2	MHz
F _{32K1}	Internal low speed oscillator frequency	Trimmed for 3.3 V operation using factory trim values	19	32	50	kHz
F _{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	—	13	32	82	kHz
F _{32K2}	Internal low speed oscillator frequency	Untrimmed	13	32	82	kHz
F _{IMO24}	Internal main oscillator stability for 24 MHz \pm 5%	—	22.8	24	25.2	MHz
F _{IMO12}	Internal main oscillator stability for 12 MHz	—	11.4	12	12.6	MHz
F _{IMO6}	Internal main oscillator stability for 6 MHz	—	5.7	6.0	6.3	MHz
DC _{IMO}	Duty Cycle of IMO	—	40	50	60	%
DC _{ILO}	Internal low speed oscillator duty cycle	—	40	50	60	%
SR _{POWER_UP}	Power supply slew rate	—	—	—	250	V/ms
T _{XRST}	External reset pulse width at power up	After supply voltage is valid	1	—	—	ms
T _{XRST2}	External reset pulse width after power up ^[17]	Applies after part has booted	10	—	—	μ s

Note

17. The minimum required XRES pulse length is longer when programming the device (see Table 19 on page 25).

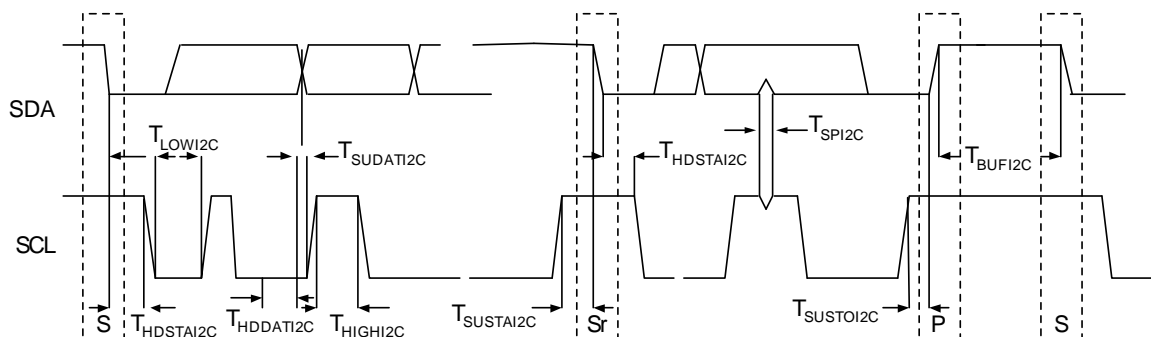
AC I²C Specifications

Table 20 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$F_{SCL I2C}$	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTA I2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μ s
$T_{LOW I2C}$	LOW period of the SCL clock	4.7	–	1.3	–	μ s
$T_{HIGH I2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	μ s
$T_{SUSTA I2C}$	Setup Time for a Repeated START condition	4.7	–	0.6	–	μ s
$T_{HDDAT I2C}$	Data hold time	0	–	0	–	μ s
$T_{SUDAT I2C}$	Data setup time	250	–	100 ⁽¹⁸⁾	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	μ s
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	μ s
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 12. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

18. A fast mode I2C bus device can be used in a standard mode I2C bus system, but the requirement $t_{SU, DAT} \leq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU, DAT} = 1000 + 250 = 1250$ ns (according to the standard mode I2C bus specification) before the SCL line is released.

Table 21. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{SCLK}	SCLK clock frequency	V _{DD} ≥ 2.4 V V _{DD} < 2.4 V	–	–	6 3	MHz
DC	SCLK duty cycle	–	–	50	–	%
T _{SETUP}	MISO to SCLK setup time	V _{DD} ≥ 2.4 V V _{DD} < 2.4 V	60 100	–	–	ns
T _{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
T _{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
T _{OUT_HIGH}	MOSI high time	–	40	–	–	ns

Table 22. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{SCLK}	SCLK clock frequency	V _{DD} ≥ 2.4 V V _{DD} < 2.4 V	–	–	12 6	MHz
T _{LOW}	SCLK low time	–	41.67	–	–	ns
T _{HIGH}	SCLK high time	–	41.67	–	–	ns
T _{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
T _{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
T _{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
T _{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
T _{SS_HIGH}	SS high time	–	–	–	50	ns
T _{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
T _{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

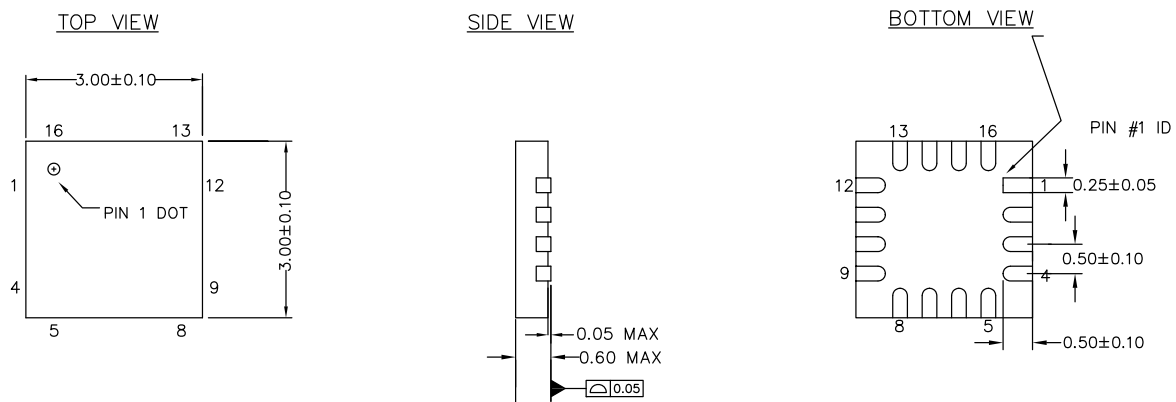
Package Diagram

This section illustrates the packaging specifications for the enCoRe V LV device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V LV emulation tools and their dimensions, refer to the development kit.

Packaging Dimensions

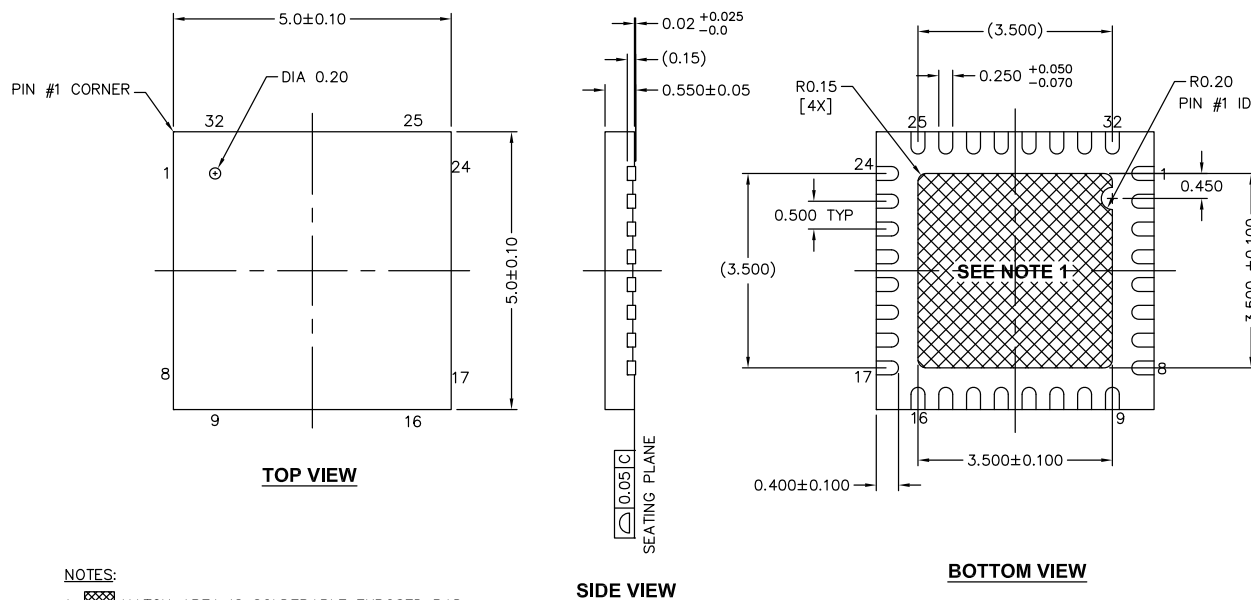
Figure 13. 16-pin Chip-On-Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116



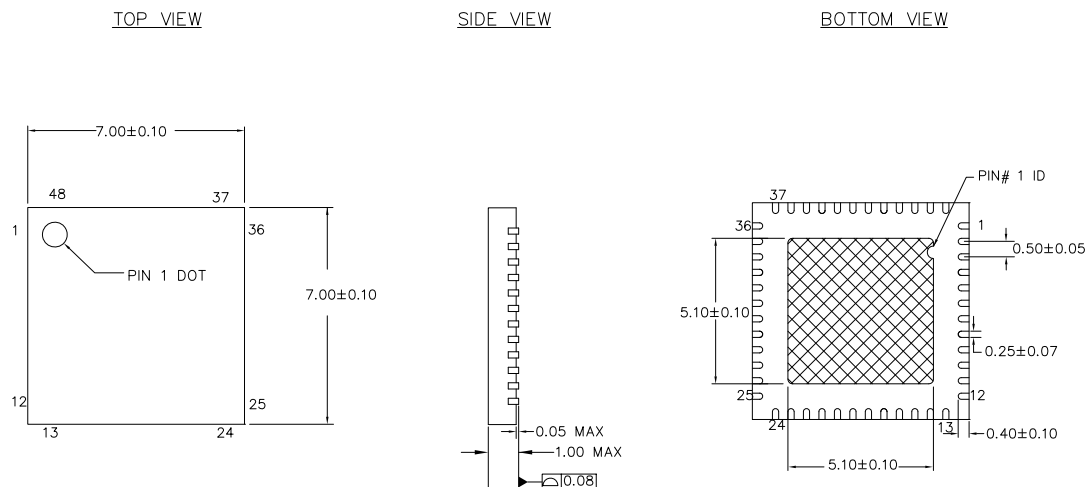
NOTES

1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *1

Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168


001-42168 *E

Figure 15. 48-pin QFN (7 × 7 × 1 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191


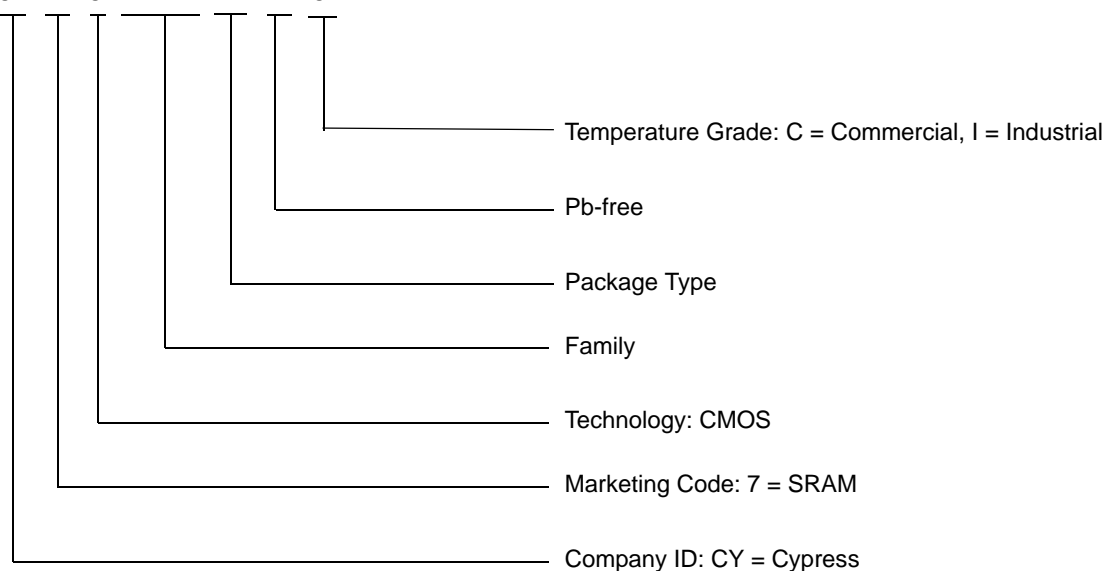
001-13191 *G

Ordering Information

Ordering Code	Package Information	Flash	SRAM	No. of GPIOs	Target Applications
CY7C60413-16LKXC	16-Pin QFN (3x3 mm)	8 K	1 K	13	Feature-rich wireless mouse
CY7C60413-16LKXCT	16-Pin QFN - (Tape and Reel) (3x3 mm)	8 K	1 K	13	Feature-rich wireless mouse
CY7C60445-32LQXC	32-Pin QFN (5x5x0.55 mm)	16 K	1 K	28	Feature-rich wireless mouse
CY7C60445-32LQXCT	32-Pin QFN - (Tape and Reel) (5x5x0.55 mm)	16 K	1 K	28	Feature-rich wireless mouse
CY7C60455-48LTXC	48-Pin QFN (7x7x0.9 mm)	16 K	1 K	36	Mid-tier wireless keyboard
CY7C60455-48LTXCT	48-Pin QFN - (Tape and Reel) (7x7x0.9 mm)	16 K	1 K	36	Mid-tier wireless keyboard
CY7C60456-48LTXC	48-Pin QFN (7x7x0.9 mm)	32 K	2 K	36	Feature-rich wireless keyboard
CY7C60456-48LTXCT	48-Pin QFN - (Tape and Reel) (7x7x0.9 mm)	32 K	2 K	36	Feature-rich wireless keyboard

Ordering Code Definitions

CY 7 C XXXXX XX X CT



Acronyms

The following table lists the acronyms that are used in this document.

Acronym	Description
API	application programming interface
CPU	central processing unit
GPIO	general purpose IO
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least significant bit
LVD	low voltage detect
MSb	most significant bit
POR	power on reset
PPOR	precision power on reset
PSoC	Programmable System-on-Chip
SLIMO	slow IMO
SRAM	static random access memory

Document Conventions

Units of Measure

The following table lists the units of measure that are used in this document.

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolts
μVrms	microvolts root-mean-square
μW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volts

Errata

This section describes the errata for the enCoRe V – CY7C643xx and enCoRe V LV – CY7C604xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY7C604xx Errata Summary

The following Errata item applies to the **CY7C643xx** and **CY7C604xx** data sheets.

1. Latch up susceptibility when maximum I/O sink current exceeded

■ **PROBLEM DEFINITION**

P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.

■ **PARAMETERS AFFECTED**

LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.

■ **TRIGGER CONDITIONS**

Latch up occurs when both the following conditions are met:

- A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.
- B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below Vss (signal undershoot) and a current greater than 200 mA to flow out of the pin.

■ **SCOPE OF IMPACT**

The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx and CY7C604xx data sheets.

■ **WORKAROUND**

Add a series resistor $> 300\ \Omega$ to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.

■ **FIX STATUS**

This issue will be corrected in the next new silicon revision.

Document History Page (continued)

Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*N	3980412	CSAI	04/24/2013	Updated Packaging Dimensions : spec 001-09116 – Changed revision from *E to *H. spec 001-42168 – Changed revision from *D to *E. spec 001-13191 – Changed revision from *E to *G. Added Errata .
*O	4074141	CSAI	07/23/2013	Added Errata footnote (Note 7). Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC General Purpose I/O Specifications [7] : Added Note 7 and referred the same note in the heading. Updated Errata . Updated in new template.
*P	4189348	CSAI	11/12/2013	Updated Packaging Dimensions : spec 001-09116 – Changed revision from *H to *I. Completing Sunset Review.