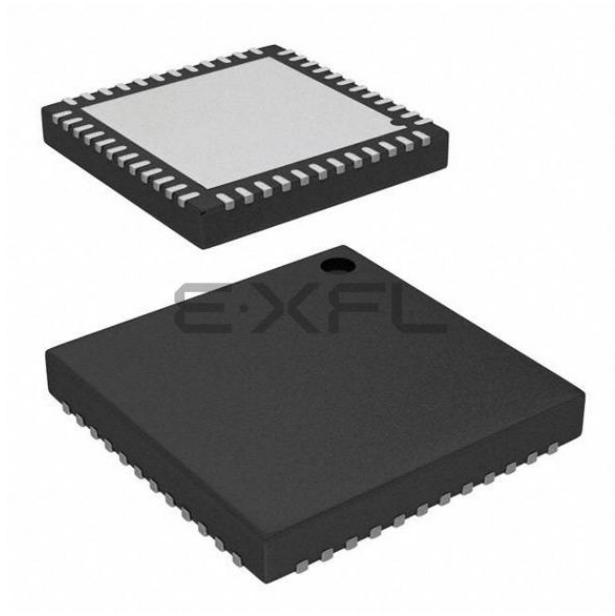

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c60456-48ltxct

Contents

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

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PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Pin Configuration

16-Pin Part Pinout

Figure 5. CY7C60413 16-Pin enCoRe V LV Device

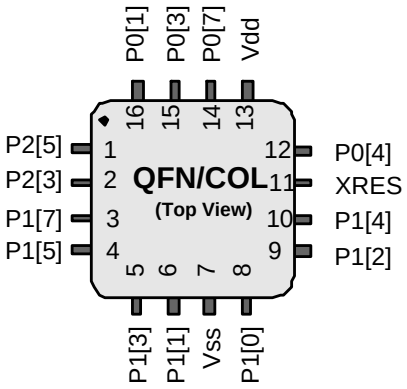


Table 1. 16-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	I/O	P2[5]	Digital I/O, crystal out (Xout)
2	I/O	P2[3]	Digital I/O, crystal in (Xin)
3	IOHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
4	IOHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
5	IOHR	P1[3]	Digital I/O, SPI CLK
6	IOHR	P1[1][1, 2]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
7	Power	Vss	Ground pin
8	IOHR	P1[0][1, 2]	Digital I/O, ISSP DATA, I^2C SDA, SPI CLK
9	IOHR	P1[2]	Digital I/O
10	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
11	Input	XRES	Active high external reset with internal pull-down
12	IOHR	P0[4]	Digital I/O
13	Power	Vdd	Power pin
14	IOHR	P0[7]	Digital I/O
15	IOHR	P0[3]	Digital I/O
16	IOHR	P0[1]	Digital I/O

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes
1. During power up or reset event, device P1[0] and P1[1] may disturb the I2C bus. Use alternate pins if issues are encountered.
2. These are the ISSP pins, that are not High Z at POR.

Table 2. 32-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
28	Power	Vdd	Supply voltage
29	IOH	P0[7]	Digital I/O
30	IOH	P0[5]	Digital I/O
31	IOH	P0[3]	Digital I/O
32	Power	Vss	Ground connection
CP	Power	Vss	Center pad must be connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

48-Pin Part Pinout

Figure 7. CY7C60455/CY7C60456 48-Pin enCoRe V LV Device

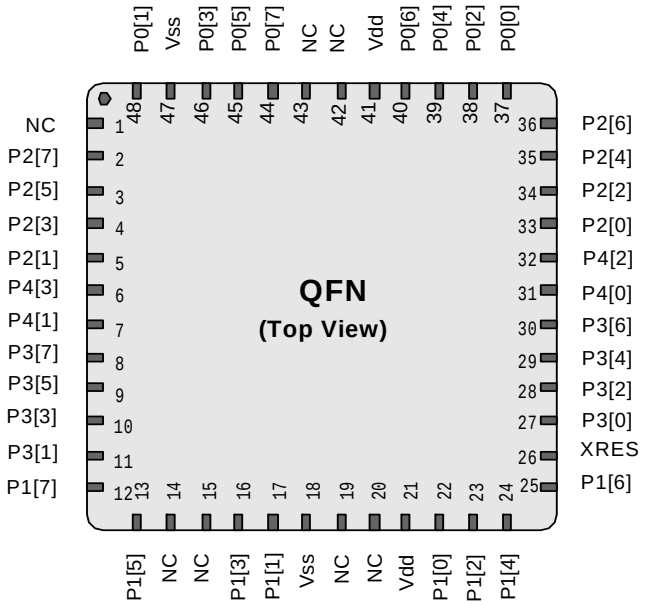


Table 3. 48-Pin Part Pinout (QFN)

Pin No.	Type	Name	Description
1	NC	NC	No connection
2	I/O	P2[7]	Digital I/O
3	I/O	P2[5]	Digital I/O, crystal out (Xout)
4	I/O	P2[3]	Digital I/O, crystal in (Xin)
5	I/O	P2[1]	Digital I/O
6	I/O	P4[3]	Digital I/O
7	I/O	P4[1]	Digital I/O
8	I/O	P3[7]	Digital I/O
9	I/O	P3[5]	Digital I/O
10	I/O	P3[3]	Digital I/O
11	I/O	P3[1]	Digital I/O
12	IOHR	P1[7]	Digital I/O, I^2C SCL, SPI SS
13	IOHR	P1[5]	Digital I/O, I^2C SDA, SPI MISO
14	NC	NC	No connection
15	NC	NC	No connection
16	IOHR	P1[3]	Digital I/O, SPI CLK
17	IOHR	P1[1][1,2]	Digital I/O, ISSP CLK, I^2C SCL, SPI MOSI
18	Power	Vss	Supply ground
19	NC	NC	No connection
20	NC	NC	No connection
21	Power	Vdd	Supply voltage

Table 3. 48-Pin Part Pinout (QFN) (continued)

Pin No.	Type	Name	Description
22	IOHR	P1[0][1,2]	Digital I/O, ISSP DATA, I2C SDA, SPI CLK
23	IOHR	P1[2]	Digital I/O
24	IOHR	P1[4]	Digital I/O, optional external clock input (EXTCLK)
25	IOHR	P1[6]	Digital I/O
26	XRES	Ext Reset	Active high external reset with internal pull-down
27	I/O	P3[0]	Digital I/O
28	I/O	P3[2]	Digital I/O
29	I/O	P3[4]	Digital I/O
30	I/O	P3[6]	Digital I/O
31	I/O	P4[0]	Digital I/O
32	I/O	P4[2]	Digital I/O
33	I/O	P2[0]	Digital I/O
34	I/O	P2[2]	Digital I/O
35	I/O	P2[4]	Digital I/O
36	I/O	P2[6]	Digital I/O
37	IOH	P0[0]	Digital I/O
38	IOH	P0[2]	Digital I/O
39	IOH	P0[4]	Digital I/O
40	IOH	P0[6]	Digital I/O
41	Power	Vdd	Supply voltage
42	NC	NC	No connection
43	NC	NC	No connection
44	IOH	P0[7]	Digital I/O
45	IOH	P0[5]	Digital I/O
46	IOH	P0[3]	Digital I/O
47	Power	Vss	Supply ground
48	IOH	P0[1]	Digital I/O
CP	Power	Vss	Center pad must be connected to ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Register Reference

The section discusses the registers of the enCoRe V LV device. It lists all the registers in mapping tables, in address order.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bits
W	Write register or bits
L	Logical register or bits
C	Clearable register or bits
#	Access is bit specific

Register Mapping Tables

The enCoRe V LV device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts: Bank 0 (user space) and Bank 1 (configuration space). The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the ‘extended’ address space or the ‘configuration’ registers.

Table 11. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	IOH < 10 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	IOH = 0.2 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.4	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH < 10 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.5	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH < 10 µA, Vdd > 2.4V, maximum of 20 mA source current in all I/Os.	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	IOH = 1 mA, Vdd > 2.4V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	1.4	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	0.001	1	µA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.5	1.7	5	pF

Table 12. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.6	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	IOH = 10 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	IOH = 0.5 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.5	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 100 µA, maximum of 10 mA source current in all I/Os	Vdd – 0.2	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all I/Os	Vdd – 0.5	–	–	V
V_{OL}	Low output voltage	IOL = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.4	V
V_{IL}	Input low voltage	–	–	–	0.3 x Vdd	V
V_{IH}	Input high voltage	–	0.65 x Vdd	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	0.001	1	µA
C_{PIN}	Capacitive load on pins	Package and pin dependent. Temp = 25 ° C	0.5	1.7	5	pF

ADC Electrical Specifications

Table 13.ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	VREFADC	V
C_{IIN}	Input capacitance	–		–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	–	–	ksps
S10	10-bit sample rate	Data Clock set to 6 MHz. Sample Rate = 0.001/ (2^Resolution/Data Clock)	–	5.859	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{Offset}	Offset error	8-bit resolution	0	3.2	19.2	LSB
		10-bit resolution	0	12.8	76.8	LSB
E_{gain}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.1	2.6	mA
PSRR	Power supply rejection ratio	PSRR (Vdd > 3.0 V)	–	24	–	dB
		PSRR (Vdd < 3.0 V)	–	30	–	dB

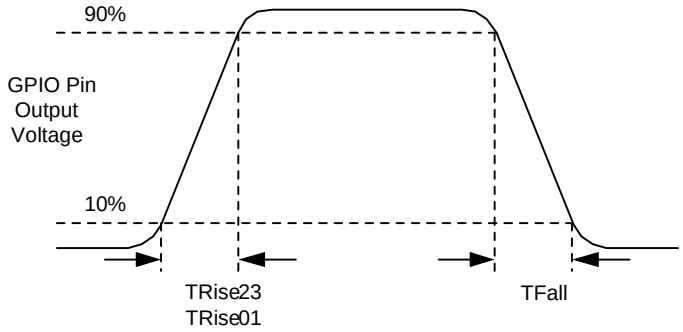
AC General Purpose IO Specifications

Table 17 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode, port 0, 1	0 0	– –	6 MHz for 1.71 V < Vdd < 2.4 V 12 MHz for 2.4 V < Vdd < 3.6 V	MHz
		Normal strong mode, Port 2, 3	0	–	3 MHz for 1.71 V < Vdd < 2.4 V 6 MHz for 3.0 V< Vdd < 3.6 V	MHz
TRise23	Rise time, strong mode, cload = 50 pF Ports 2 or 3	Vdd = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
TRise23L	Rise time, strong mode low supply, cload = 50 pF Ports 2 or 3	Vdd = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
TRise01	Rise time, strong mode, cload = 50 pF Ports 0 or 1	Vdd = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	– –	50	ns
TRise01L	Rise time, strong mode low supply, cload = 50 pF Ports 0 or 1	Vdd = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	15	–	80	ns
TFall	Fall time, strong mode, cload = 50 pF, All Ports	Vdd = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
TFallL	Fall time, strong mode low supply, cload = 50 pF, all ports	Vdd = 1.71 to 3.0 V, 10% - 90%	10	–	70	ns

Figure 10. GPIO Timing Diagram



AC External Clock Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	–	0.750	–	25.2	MHz
–	High period	–	20.6	–	5300	ns
–	Low period	–	20.6	–	–	ns
–	Power up IMO to switch	–	150	–	–	µs

AC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
T_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
T_{SSCLK}	Data set up time to falling edge of SCLK	–	40	–	–	ns
T_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
T_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
T_{WRITE}	Flash block write time	–	–	–	25	ms
T_{DSCLK1}	Data out delay from falling edge of SCLK	3.0 V < Vdd < 3.6 V	–	–	85	ns
T_{DSCLK2}	Data out delay from falling edge of SCLK	1.71 V < Vdd < 3.0 V	–	–	130	ns
T_{XRST3}	External reset pulse width after power up	Required to enter programming mode when coming out of sleep	263	–	–	µs

Figure 11. Timing Diagram - AC Programming Cycle

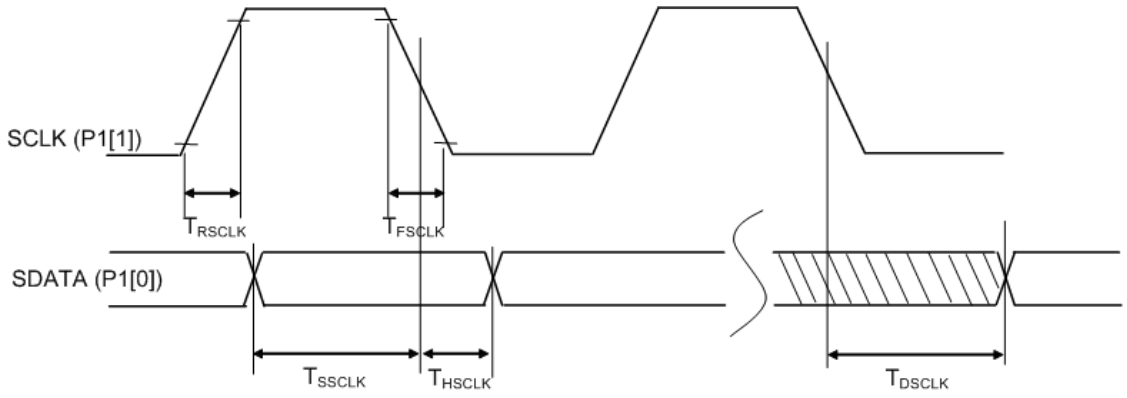


Table 21. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	–	–	6 3	MHz
DC	SCLK duty cycle	–	–	50	–	%
T_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	60 100	–	–	ns
T_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
T_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
T_{OUT_HIGH}	MOSI high time	–	40	–	–	ns

Table 22.SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	–	–	12 6	MHz
T_{LOW}	SCLK low time	–	41.67	–	–	ns
T_{HIGH}	SCLK high time	–	41.67	–	–	ns
T_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
T_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
T_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
T_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
T_{SS_HIGH}	SS high time	–	–	–	50	ns
T_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
T_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

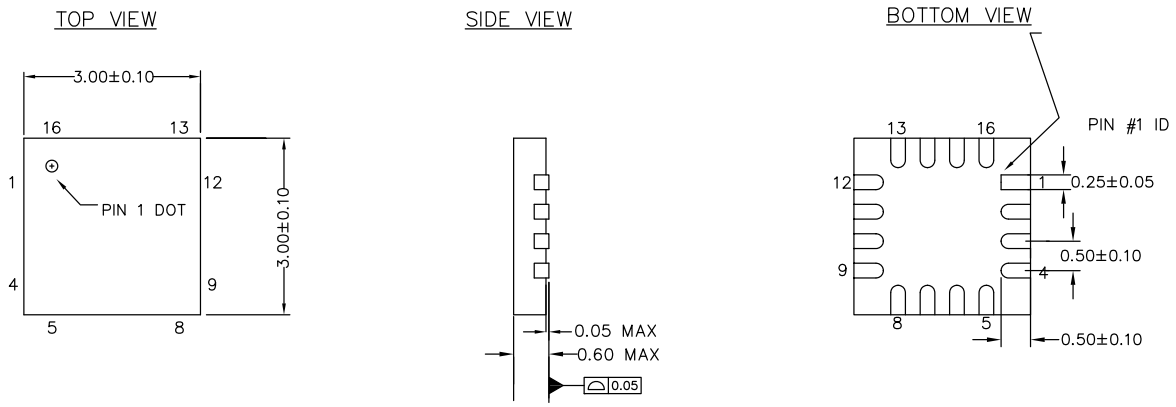
Package Diagram

This section illustrates the packaging specifications for the enCoRe V LV device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the enCoRe V LV emulation tools and their dimensions, refer to the development kit.

Packaging Dimensions

Figure 13. 16-pin Chip-On-Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116



NOTES
1. REFERENCE JEDEC # MO−220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *I

Figure 14. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168

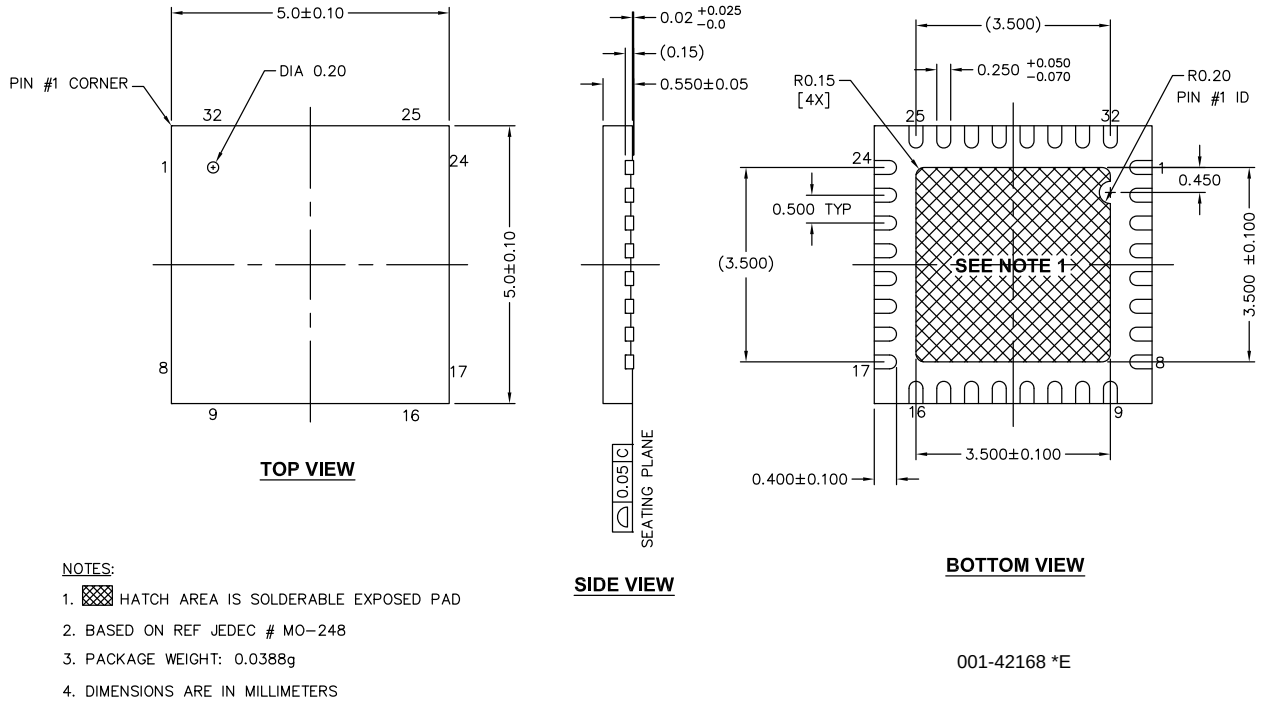
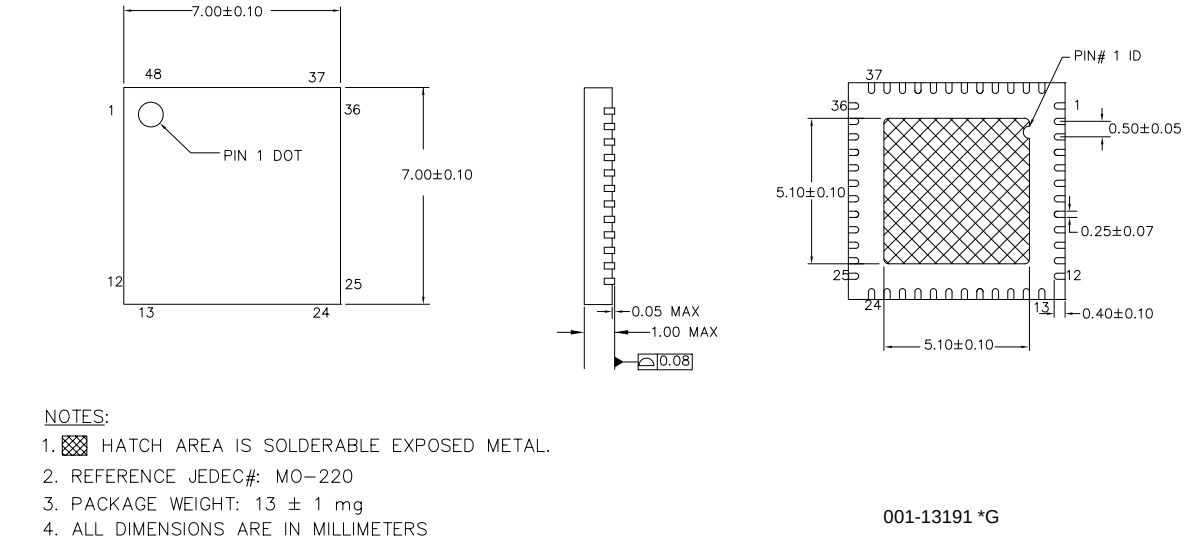


Figure 15. 48-pin QFN (7 × 7 × 1 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191



Package Handling

Some IC packages require baking before they are soldered onto a PCB to remove moisture that may have been absorbed after leaving the factory. A label on the package has details about the actual bake temperature and the minimum bake time to remove this moisture. The maximum bake time is the aggregate time that the parts exposed to the bake temperature. Exceeding this exposure may degrade device reliability.

Table 23.Package Handling

Parameter	Description	Minimum	Typical	Maximum	Unit
TBAKETEMP	Bake Temperature	–	125	See package label	°C
TBAKETIME	Bake Time	See package label	–	72	hours

Thermal Impedances

Package	Typical θ_{JA} (19)
16 QFN	32.69 °C/W
32 QFN(20)	19.51 °C/W
48 QFN(20)	17.68 °C/W

Capacitance on Crystal Pins

Table 24. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 QFN	3.2 pF
48 QFN	3.3 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature(21)	Maximum Peak Temperature
16 QFN	240 °C	260 °C
32 QFN	240 °C	260 °C
48 QFN	240 °C	260 °C

Notes
19. $T_J = T_A$ + Power x θ_{JA}.
20. To achieve the thermal impedance specified for the package, solder the center thermal pad to the PCB ground plane.
21. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Acronyms

The following table lists the acronyms that are used in this document.

Acronym	Description
API	application programming interface
CPU	central processing unit
GPIO	general purpose IO
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
LSb	least significant bit
LVD	low voltage detect
MSb	most significant bit
POR	power on reset
PPOR	precision power on reset
PSoC	Programmable System-on-Chip
SLIMO	slow IMO
SRAM	static random access memory

Document Conventions

Units of Measure

The following table lists the units of measure that are used in this document.

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolts
µVrms	microvolts root-mean-square
µW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volts

Errata

This section describes the errata for the enCoRe V – CY7C643xx and enCoRe V LV – CY7C604xx. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY7C604xx Errata Summary

The following Errata item applies to the **CY7C643xx** and **CY7C604xx** data sheets.

1. Latch up susceptibility when maximum I/O sink current exceeded

- **PROBLEM DEFINITION**
  P1[3], P1[6], and P1[7] pins are susceptible to latch up when the I/O sink current exceeds 25 mA per pin on these pins.
- **PARAMETERS AFFECTED**
  LU – Latch up current. Per JESD78A, the maximum allowable latch up current per pin is 100 mA. Cypress internal specification is 200 mA latch up current limit.
- **TRIGGER CONDITIONS**
  Latch up occurs when both the following conditions are met:
  A. The offending I/O is externally connected to a voltage higher than the I/O high state, causing a current to flow into the pin that exceeds 25 mA.
  B. A Port1 I/O (P1[1], P1[4], and P1[5] respectively) adjacent to the offending I/O is connected to a voltage lower than the I/O low state. This causes a signal that drops below Vss (signal undershoot) and a current greater than 200 mA to flow out of the pin.
- **SCOPE OF IMPACT**
  The trigger conditions outlined in this item exceed the maximum ratings specified in the CY7C643xx and CY7C604xx data sheets.
- **WORKAROUND**
  Add a series resistor > 300 Ω to P1[3], P1[6], and P1[7] pins to restrict current to within latch up limits.
- **FIX STATUS**
  This issue will be corrected in the next new silicon revision.

Document History Page

Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	626516	TYJ	See ECN	New data sheet
*A	735721	TYJ / ARI	See ECN	Added new block diagram, replaced TBDs, corrected values, updated pinout information, changed part number to reflect new specifications.
*B	1120504	ARI	See ECN	Corrected the description to pin 29 on Table 1, the Typ/Max values for I_{SB0} on the DC chip-level specifications, and the Min voltage value for Vdd_{IWRITE} in the DC Programming Specifications table. Corrected Flash Write Endurance minimum value in the DC Programming Specifications table. Corrected the Flash Erase Time max value and the Flash Block Write Time max value in the AC Programming Specifications table. Implemented new latest template.
*C	1225864	AESA / ARI	See ECN	Corrected the description to pin 13, 29 on Table 1 and 22,44 on Table 2. Added sections Register Reference, Register Conventions and Register Mapping Tables. Corrected Max values on the DC Chip-Level Specifications table.
*D	1446763	AESA	See ECN	Changed T_{ERASEB} parameter, max value to 18ms in Table 13, AC Programming Specification.
*E	1639963	AESA	See ECN	Post to www.cypress.com
*F	2138889	TYJ / PYRS	See ECN	Updated Ordering Code table: - Ordering code changed for 32-QFN package: From -32LKXC to -32LTXC - Added a new package type – “LTXC” for 48-QFN - Included Tape and Reel ordering code for 32-QFN and 48-QFN packages Changed active current values at 24, 12 and 6MHz in table “DC Chip-Level Specifications” - IDD24: 2.15 to 3.1mA - IDD12: 1.45 to 2.0mA - IDD6: 1.1 to 1.5mA Added information on using P1[0] and P1[1] as the I2C interface during POR or reset events

Document History Page (continued)

Document Title: CY7C604XX, enCoRe™ V Low Voltage Microcontroller Document Number: 001-12395				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G	2583853	TYJ / PYRS / HMT	10/10/08	Converted from Preliminary to Final ADC resolution changed from 10-bit to 8-bit On Page1, SPI Master and Slave – speeds changed Rephrased battery monitoring clause in page 1 to include “with external components” Included ADC specifications table Voh5, Voh7, Voh9 specs changed Flash data retention – condition added to Note [15] Input leakage spec changed to 25 nA max Under AC Char, Frequency accuracy of ILO corrected GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated Spec change for 32-QFN package Input Leakage Current maximum value changed to 1 uA Maximum specification for V_{OH5A} parameter changed from 2.0 to 2.1V Minimum voltages for F_{SPIM} and F_{SPIS} specifications changed from 1.8V to 1.71V (Table 18) Updated V_{OHV} parameter in Table 13 Updated Thermal impedance values for the packages - Table 20. Update Development Tools, add Designing with PSoC Designer. Edit, fix links and table format. Update TMs. Update maximum data in Table 12. DC POR and LVD Specifications.
*H	2653717	DVJA / PYRS	02/04/09	Changed master page from CY7C60445, CY7C6045X to CY7C604XX. Updated Features, Functional Overview, Development Tools, and Designing with PSoC Designer sections. Removed ‘GUI - graphical user interface’ from Document Conventions acronym table. Added Figure 1 and Table 1 (16-pin part information) to Pin Configurations section. Removed ‘O - Only a read/write register or bits’ in Table 4 Edited Table 8: removed 10-bit resolution information and corrected units column. Added Figure 9 (16-pin part information) to Package Dimensions section. Added ‘Package Handling’ section. Added 8K part ‘CY7C60413-16LKXC’ to Ordering Information.
*I	2714694	DVJA / AESA	06/04/2009	Updated Block Diagram. Added 10-bit ADC, SPI, and I2C Slave sections. ADC Resolution changed from 8-bit to 10-bit Updated Figure 9: 5.7 MHz minimum CPU frequency Updated Table 15 AC Chip Level Specs Figure 8: Changed minimum CPU Frequency from 750 kHz to 5.7 MHz
*J	2764460	DVJA / AESA	09/15/2009	Added footnote #5 to Table 10: DC Chip Level Specs Added F_{32K2} (Untrimmed) spec to Table 17: AC Chip level Specs Changed T_{RAMP} spec to SR_{POWER_UP} in Table 17: AC Chip Level Specs Changed Table 14: ADC Specs Added Table 25: Typical Package Capacitance on Crystal Pins
*K	2811903	DVJA	11/23/2009	Added Note 6 on page 18. Changed V_{IHP} in Table 15 on page 22
*L	3075921	NXZ	11/01/2010	Added Ordering Code Definition.
*M	3283876	DIVA	06/15/2011	Updated Getting Started, Development Tools, and Designing with PSoC Designer.

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