Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	10
Number of Gates	-
Number of I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.51x11.51)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/gal22v10d-7lji

Product Line	Ordering Part Number	Product Status	Reference PCN
GAL22V10D (Cont'd)	GAL22V10D-7LJ	Discontinued	PCN#13-10
	GAL22V10D-7LJN		
	GAL22V10D-10LJ		
	GAL22V10D-10LJN		
	GAL22V10D-15LJ		
	GAL22V10D-15LJN		
	GAL22V10D-25LJ		
	GAL22V10D-25LJN		
	GAL22V10D-7LJI		PCN#09-10
	GAL22V10D-7LJNI		
	GAL22V10D-10LJI		
	GAL22V10D-10LJNI		
	GAL22V10D-15LJI		PCN#13-10
	GAL22V10D-15LJNI		
	GAL22V10D-20LJI		
	GAL22V10D-20LJNI		
	GAL22V10D-25LJI		
	GAL22V10D-25LJNI		
	GAL22V10D-10QJ		
	GAL22V10D-10QJN		
	GAL22V10D-15QJ		
	GAL22V10D-15QJN		
	GAL22V10D-25QJ		
	GAL22V10D-25QJN		

5555 N.E. Moore Ct. ● Hillsboro, Oregon 97124-6421 ● Phone (503) 268-8000 ● FAX (503) 268-8347
Internet: http://www.latticesemi.com

GAL22V10

High Performance E²CMOS PLD Generic Array Logic™

Lead-Free Package Options Available!

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 4 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 3.5 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- ACTIVE PULL-UPS ON ALL PINS
- COMPATIBLE WITH STANDARD 22V10 DEVICES
  - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices
- 50% to 75% REDUCTION IN POWER VERSUS BIPOLAR
  - 90mA Typical Icc on Low Power Device
  - 45mA Typical Icc on Quarter Power Device
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- TEN OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
- PRELOAD AND POWER-ON RESET OF REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

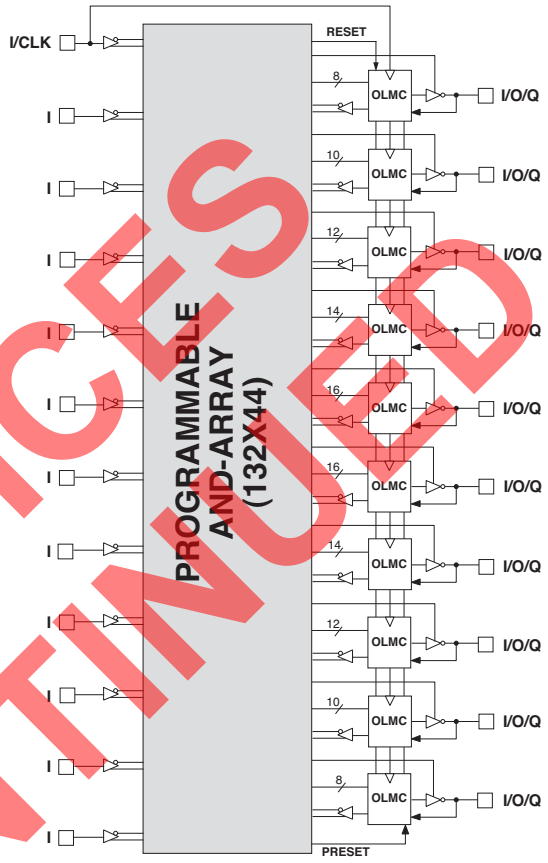
Description

The GAL22V10, at 4ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

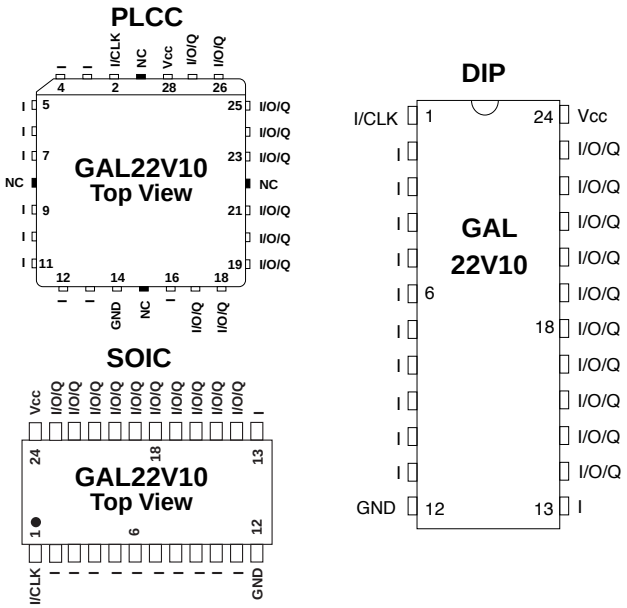
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram



Pin Configuration



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

December 2006

GAL22V10 Ordering Information

Conventional Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	2.5	3.5	140	GAL22V10D-4LJ	28-Lead PLCC
5	3	4	140	GAL22V10D-5LJ	28-Lead PLCC
7.5	4.5	4.5	140	GAL22V10D-7LP	24-Pin Plastic DIP
	4.5	4.5	140	GAL22V10D-7LJ	28-Lead PLCC
10	7	7	55	GAL22V10D-10QP	24-Pin Plastic DIP
			55	GAL22V10D-10QJ	28-Lead PLCC
			130	GAL22V10D-10LP	24-Pin Plastic DIP
			130	GAL22V10D-10LJ	28-Lead PLCC
			30	GAL22V10D-10LS[1]	24-Pin SOIC
15	10	8	55	GAL22V10D-15QP	24-Pin Plastic DIP
			55	GAL22V10D-15QJ	28-Lead PLCC
			90	GAL22V10D-15LP	24-Pin Plastic DIP
			90	GAL22V10D-15LJ	28-Lead PLCC
			90	GAL22V10D-15LS[1]	24-Pin SOIC
25	15	15	55	GAL22V10D-25QP	24-Pin Plastic DIP
			55	GAL22V10D-25QJ	28-Lead PLCC
			90	GAL22V10D-25LP	24-Pin Plastic Dip
			90	GAL22V10D-25LJ	28-Lead PLCC
			90	GAL22V10D-25LS[1]	24-Pin SOIC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	5	4.5	160	GAL22V10D-7LPI	24-Pin Plastic DIP
	4.5	4.5	160	GAL22V10D-7LJI	28-Lead PLCC
10	7	7	160	GAL22V10D-10LPI	24-Pin Plastic DIP
			160	GAL22V10D-10LJI	28-Lead PLCC
15	10	8	130	GAL22V10D-15LPI	24-Pin Plastic DIP
			130	GAL22V10D-15LJI	28-Lead PLCC
20	14	10	130	GAL22V10D-20LPI	24-Pin Plastic DIP
			130	GAL22V10D-20LJI	28-Lead PLCC
25	15	15	130	GAL22V10D-25LPI	24-Pin Plastic DIP
			130	GAL22V10D-25LJI	28-Lead PLCC

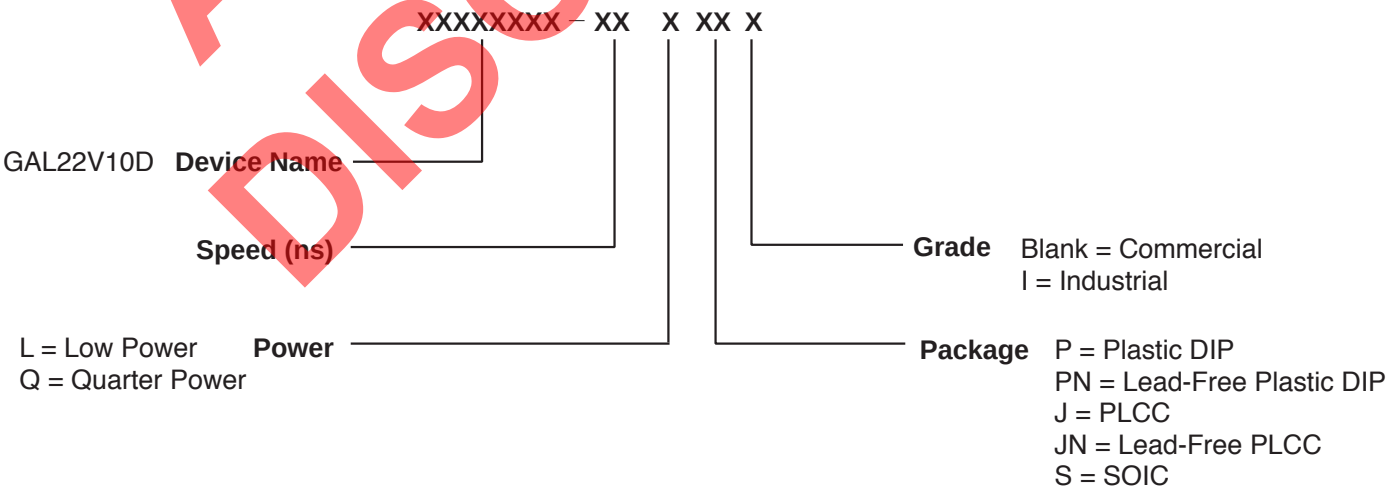
Lead-Free Packaging
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	2.5	3.5	140	GAL22V10D-4LJN	Lead-Free 28-Lead PLCC
5	3	4	140	GAL22V10D-5LJN	Lead-Free 28-Lead PLCC
7.5	4.5	4.5	140	GAL22V10D-7LPN	Lead-Free 24-Pin Plastic DIP
	4.5	4.5	140	GAL22V10D-7LJN	Lead-Free 28-Lead PLCC
10	7	7	55	GAL22V10D-10QPN	Lead-Free 24-Pin Plastic DIP
			55	GAL22V10D-10QJN	Lead-Free 28-Lead PLCC
			130	GAL22V10D-10LPN	Lead-Free 24-Pin Plastic DIP
			130	GAL22V10D-10LJN	Lead-Free 28-Lead PLCC
15	10	8	55	GAL22V10D-15QPN	Lead-Free 24-Pin Plastic DIP
			55	GAL22V10D-15QJN	Lead-Free 28-Lead PLCC
			90	GAL22V10D-15LPN	Lead-Free 24-Pin Plastic DIP
			90	GAL22V10D-15LJN	Lead-Free 28-Lead PLCC
25	15	15	55	GAL22V10D-25QPN	Lead-Free 24-Pin Plastic DIP
			55	GAL22V10D-25QJN	Lead-Free 28-Lead PLCC
			90	GAL22V10D-25LPN	Lead-Free 24-Pin Plastic Dip
			90	GAL22V10D-25LJN	Lead-Free 28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	5	4.5	160	GAL22V10D-7LPNI	Lead-Free 24-Pin Plastic DIP
	4.5	4.5	160	GAL22V10D-7LJNI	Lead-Free 28-Lead PLCC
10	7	7	160	GAL22V10D-10LPNI	Lead-Free 24-Pin Plastic DIP
			160	GAL22V10D-10LJNI	Lead-Free 28-Lead PLCC
15	10	8	130	GAL22V10D-15LPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL22V10D-15LJNI	Lead-Free 28-Lead PLCC
20	14	10	130	GAL22V10D-20LPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL22V10D-20LJNI	Lead-Free 28-Lead PLCC
25	15	15	130	GAL22V10D-25LPNI	Lead-Free 24-Pin Plastic Dip
			130	GAL22V10D-25LJNI	Lead-Free 28-Lead PLCC

Part Number Description



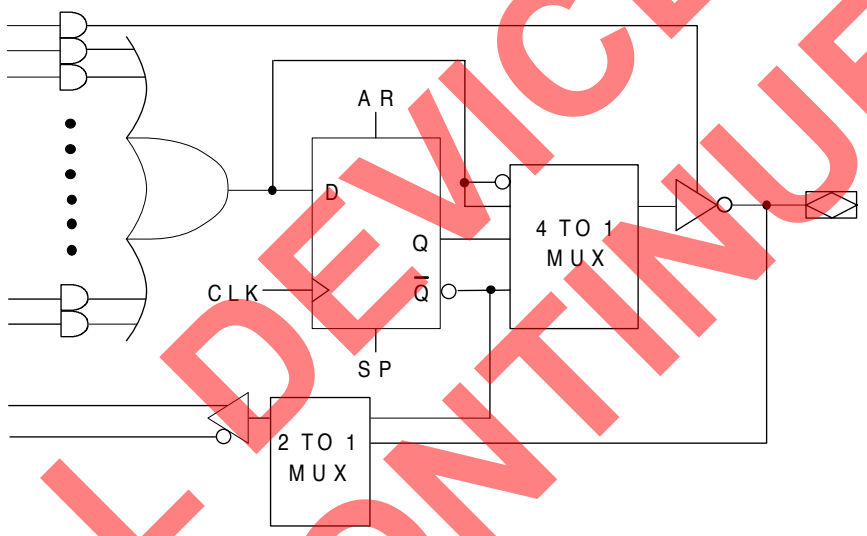
Output Logic Macrocell (OLMC)

The GAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23, DIP pinout), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the GAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (S0 and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

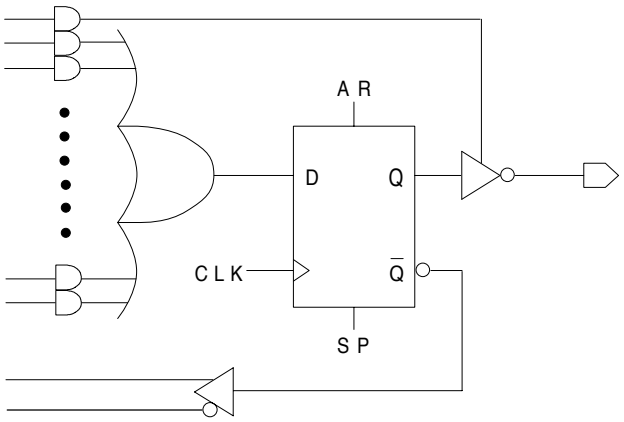
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

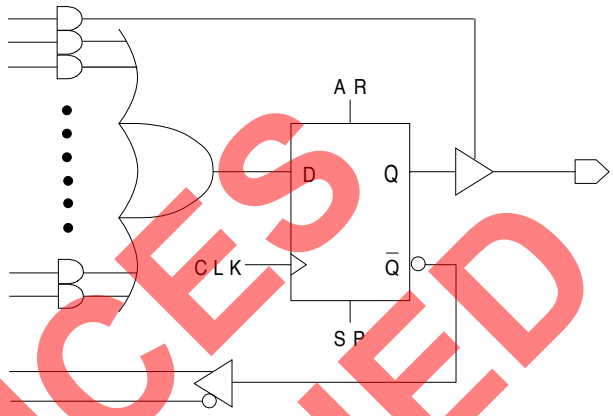
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

Registered Mode



ACTIVE LOW

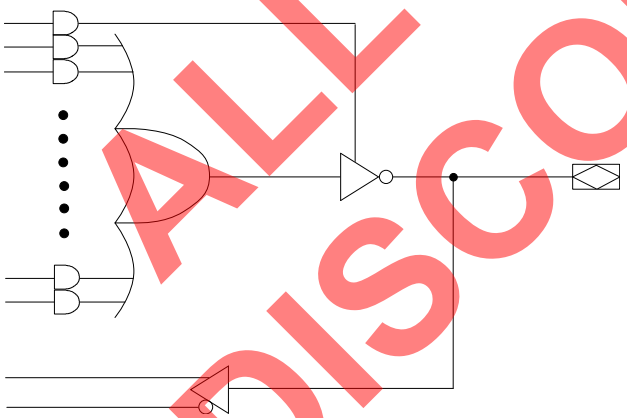
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

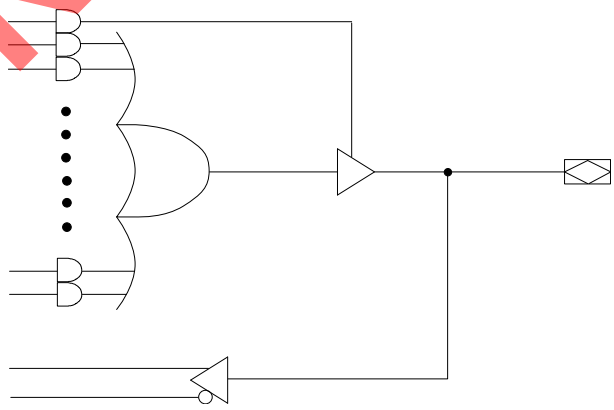
$S_0 = 1$
$S_1 = 0$

Combinatorial Mode



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

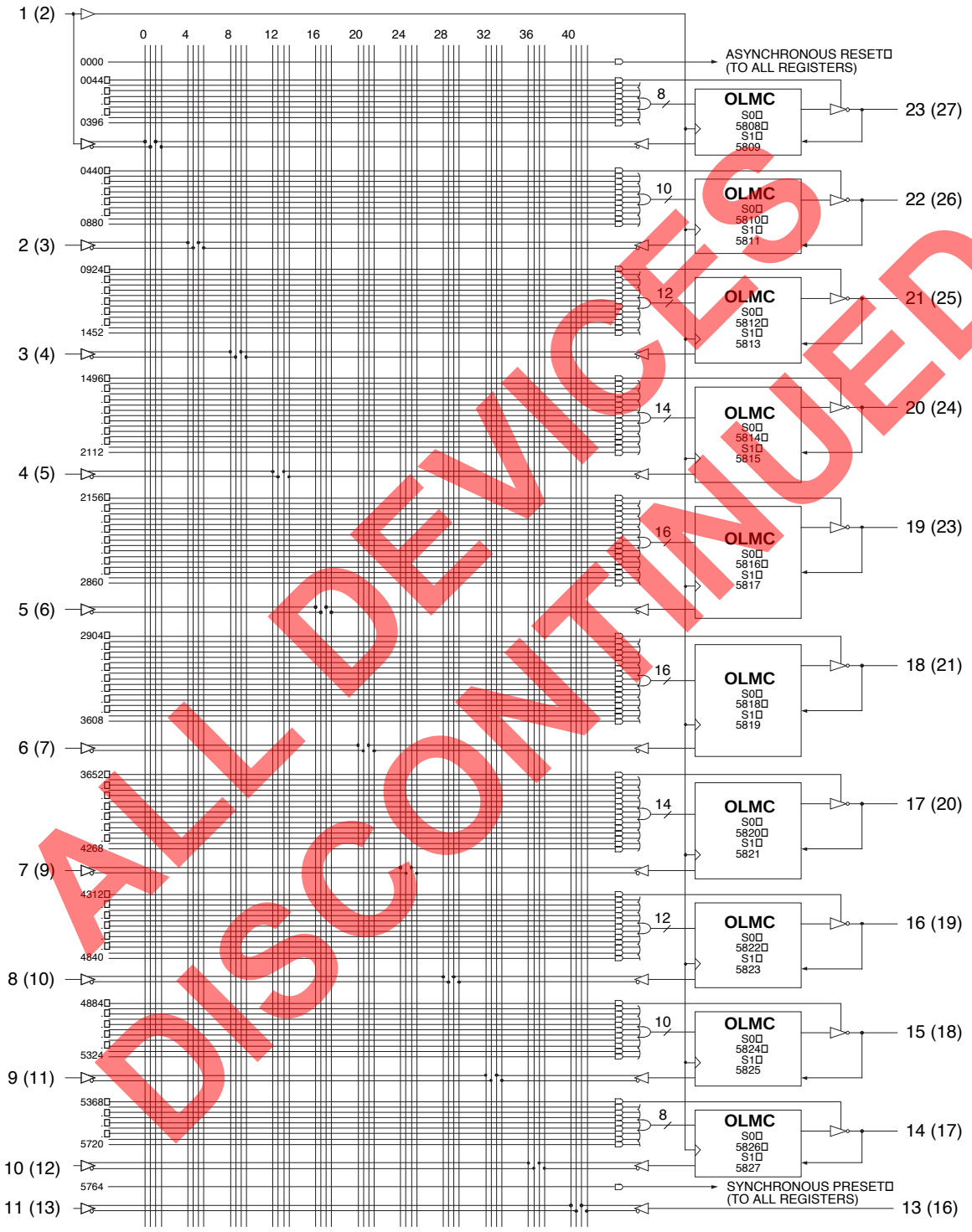


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL22V10 Logic Diagram / JEDEC Fuse Map

DIP (PLCC) Package Pinouts



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

MSB LSB

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -4		COM -5		COM/IND -7		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	1	4	1	5	1	7.5	ns
tco	A	Clock to Output Delay	1	3.5	1	4	1	4.5	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	3	—	3	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	2.5	—	3	—	4.5	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	167	—	142.8	—	111	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	133	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	200	—	166	—	MHz
twh	—	Clock Pulse Duration, High	2	—	2.5	—	3	—	ns
twl	—	Clock Pulse Duration, Low	2	—	2.5	—	3	—	ns
ten	B	Input or I/O to Output Enabled	1	5	1	6	1	7.5	ns
tdis	C	Input or I/O to Output Disabled	1	5	1	5.5	1	7.5	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	1	4.5	1	5.5	1	9	ns
tarw	—	Asynch. Reset Pulse Duration	4.5	—	4.5	—	7	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	3	—	4	—	5	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	3	—	4	—	5	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section. Characterized initially and after any design or process changes that may affect these parameters.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND.[1]	DESCRIPTION	COM / IND -10		COM / IND -15		IND -20		COM / IND -25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Comb. Output	1	10	3	15	3	20	3	25	ns
tco	A	Clock to Output Delay	1	7	2	8	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	8	—	13	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	6	—	10	—	12	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	83.3	—	55.5	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	110	—	80	—	45.4	—	35.7	—	MHz
	A	Maximum Clock Frequency with No Feedback	125	—	83.3	—	50	—	38.5	—	MHz
twh	—	Clock Pulse Duration, High	4	—	6	—	10	—	13	—	ns
twl	—	Clock Pulse Duration, Low	4	—	6	—	10	—	13	—	ns
ten	B	Input or I/O to Output Enabled	1	10	3	15	3	20	3	25	ns
tdis	C	Input or I/O to Output Disabled	1	9	3	15	3	20	3	25	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	1	13	3	20	3	25	3	25	ns
tarw	—	Asynch. Reset Pulse Duration	8	—	15	—	20	—	25	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	8	—	10	—	20	—	25	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	8	—	10	—	14	—	15	—	ns

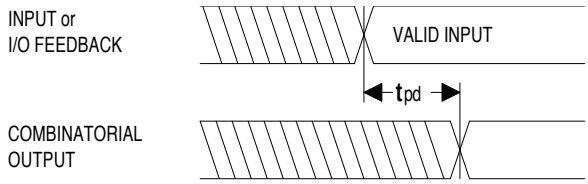
1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

Capacitance (T_A = 25°C, f = 1.0 MHz)

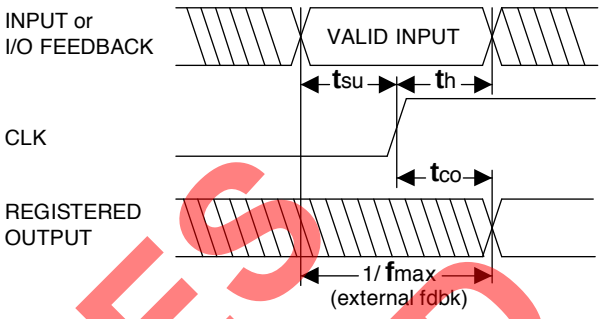
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

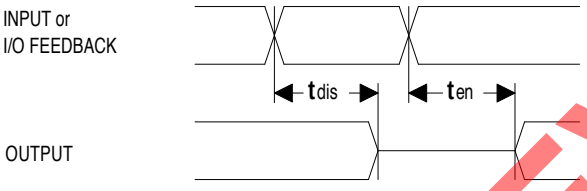
Switching Waveforms



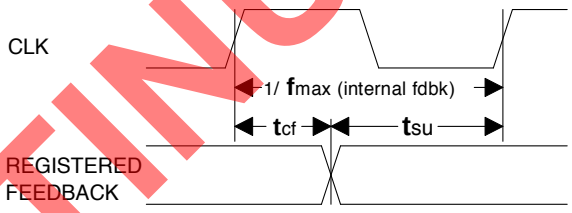
Combinatorial Output



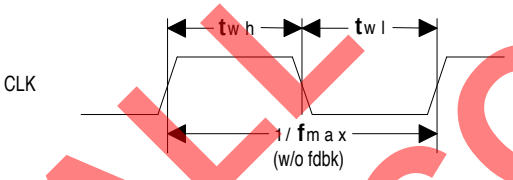
Registered Output



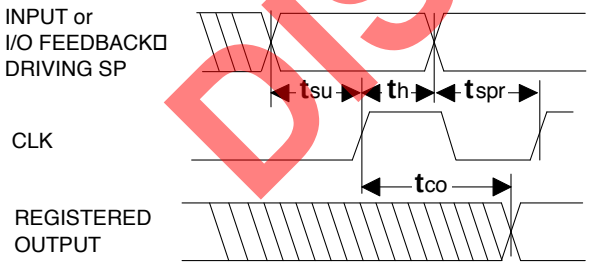
Input or I/O to Output Enable/Disable



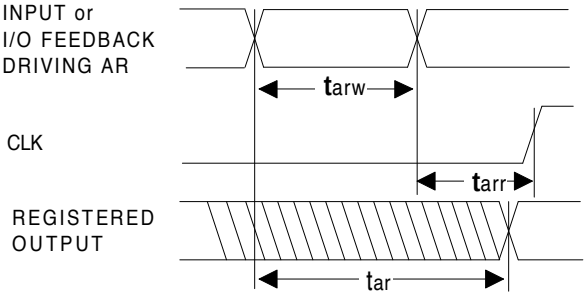
fmax with Feedback



Clock Width

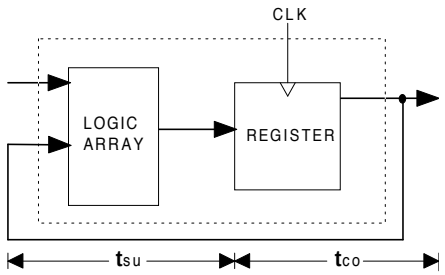


Synchronous Preset



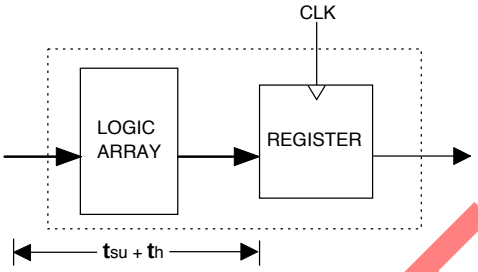
Asynchronous Reset

fmax Descriptions



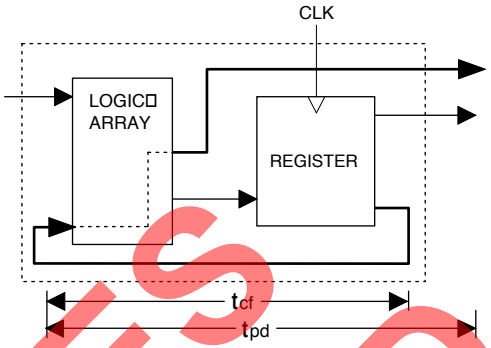
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

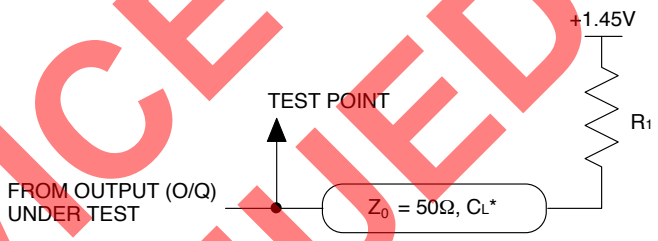
Switching Test Conditions

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	D-4/-5/-7	1.5ns 10% – 90%
	D-10/-15/-20/-25	2.0ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

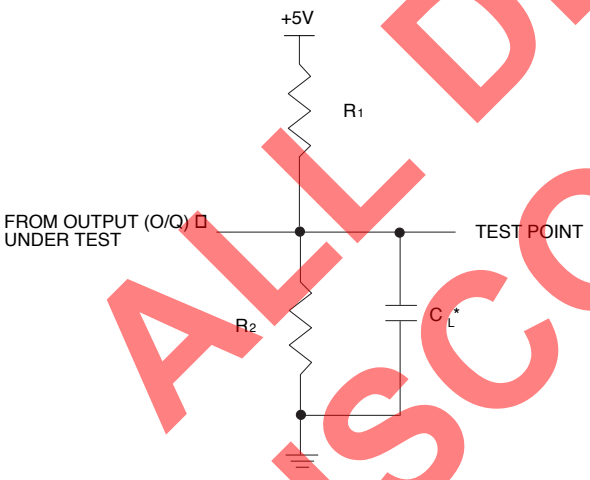
GAL22V10D-4 Output Load Conditions (see figure below)

Test Condition		R_1	C_L
A		50Ω	50pF
B	Z to Active High at 1.9V	50Ω	50pF
	Z to Active Low at 1.0V	50Ω	50pF
C	Active High to Z at 1.9V	50Ω	50pF
	Active Low to Z at 1.0V	50Ω	50pF



Output Load Conditions (except D-4) (see figure below)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Electronic Signature

An electronic signature (ES) is provided in every GAL22V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22V10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22V10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22V10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

Security Cell

A security cell is provided in every GAL22V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

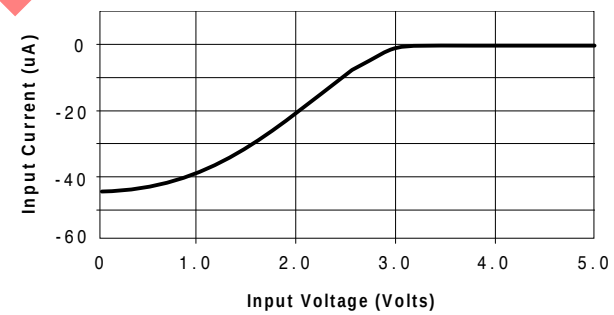
The GAL22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

Input Buffers

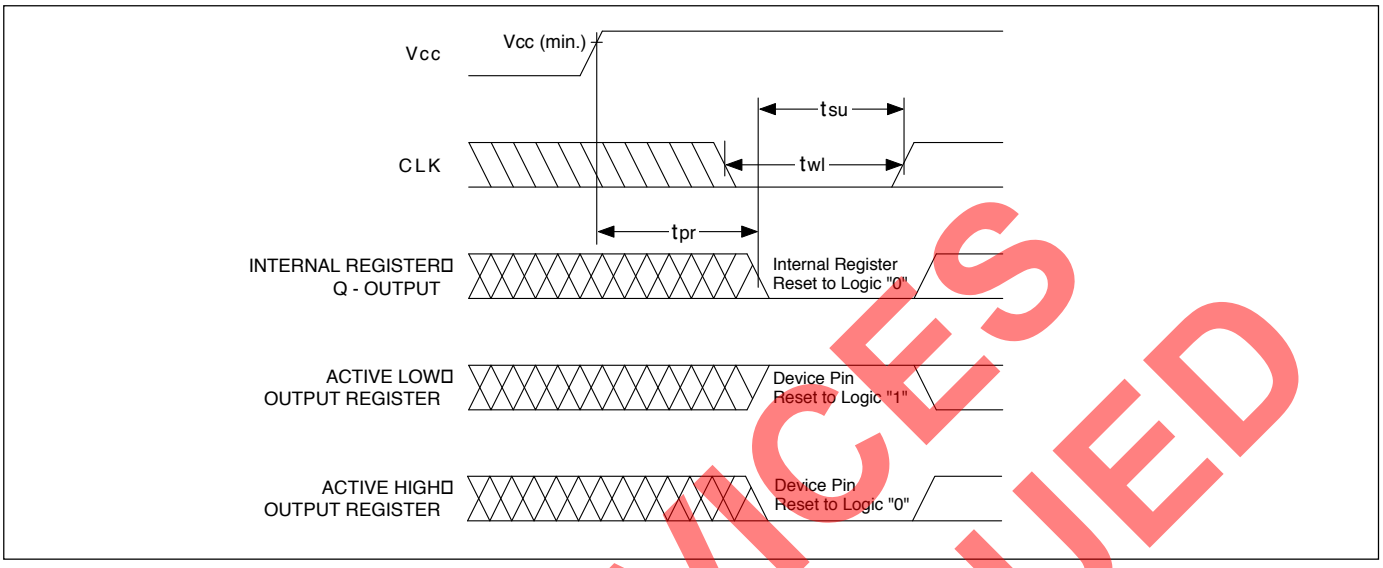
GAL22V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current

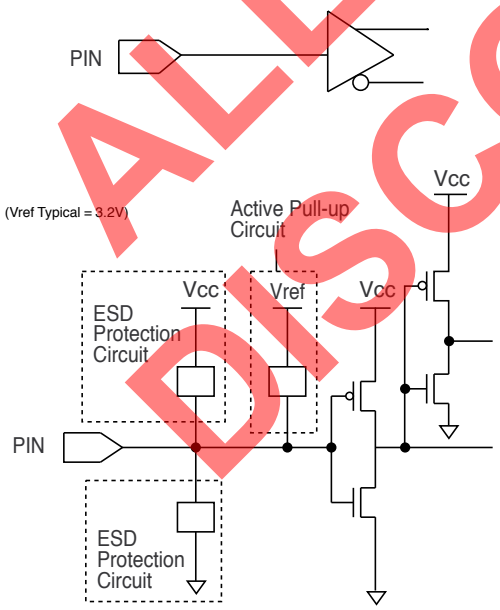


Power-Up Reset

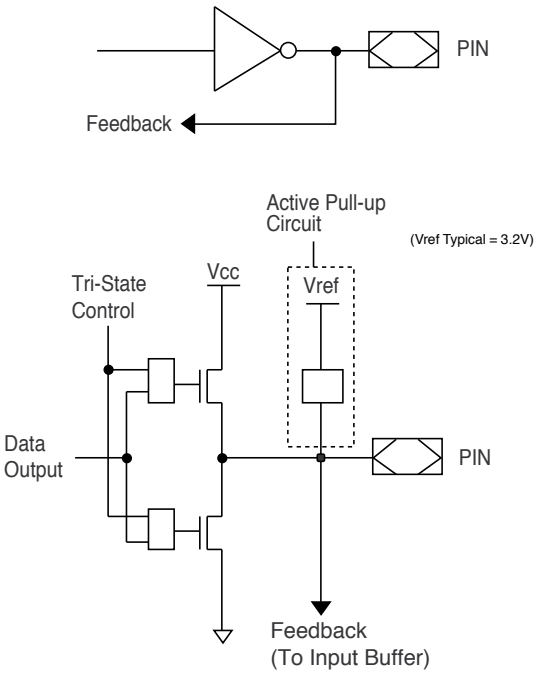


Circuitry within the GAL22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL22V10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics

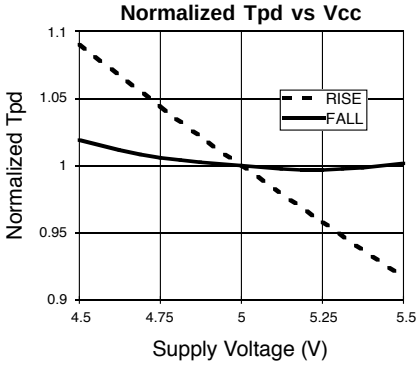


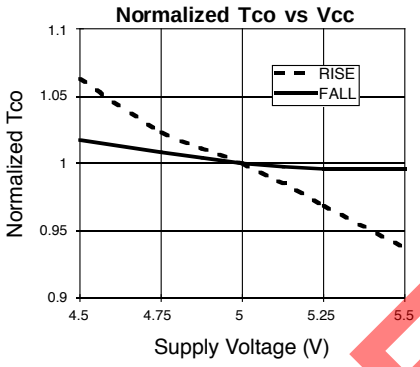
Typical Input

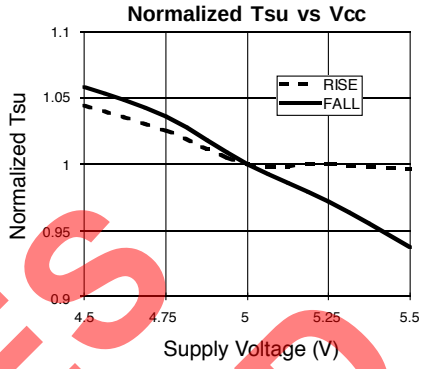


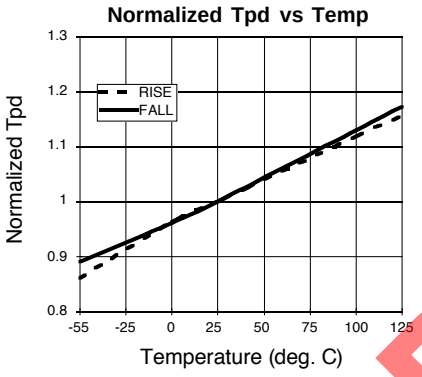
Typical Output

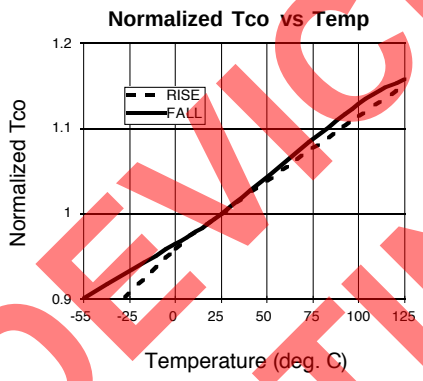
GAL22V10D-4/-5/-7/-10L (PLCC): Typical AC and DC Characteristic Diagrams

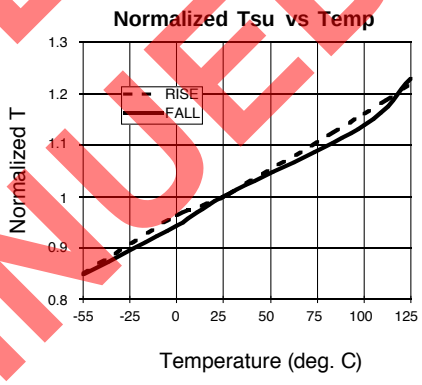


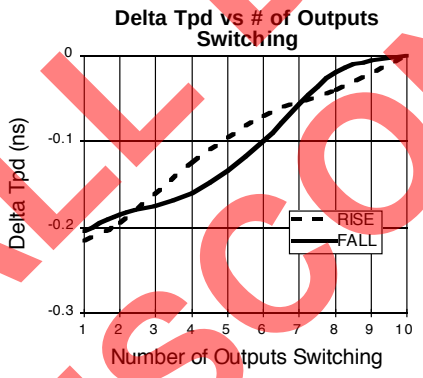


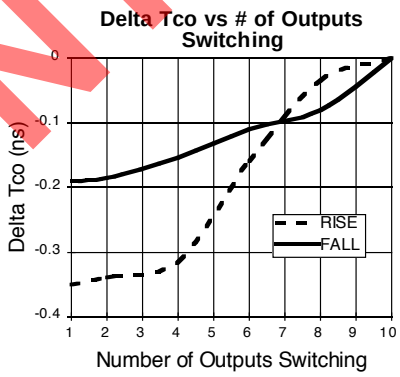


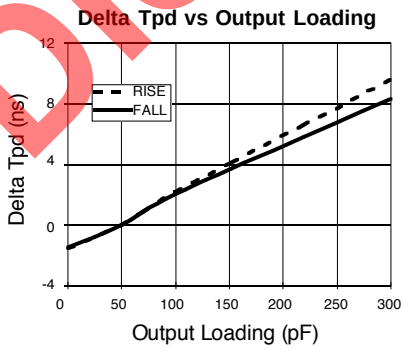


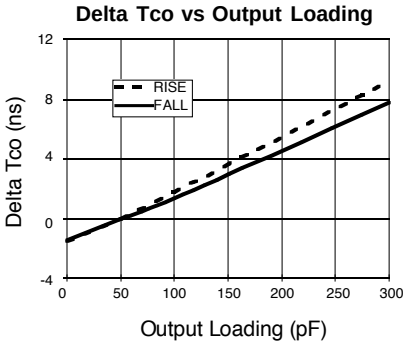






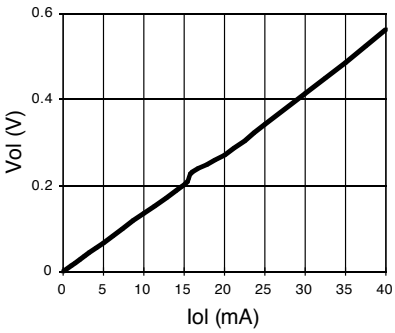




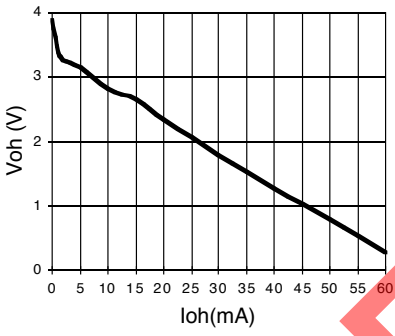


GAL22V10D-4/-5/-7/-10L (PLCC): Typical AC and DC Characteristic Diagrams

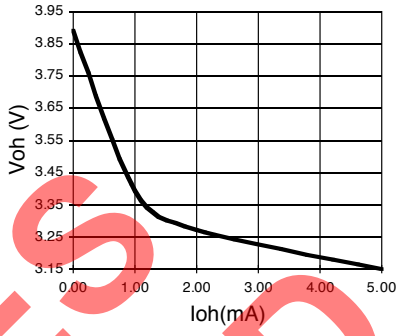
Vol vs Iol



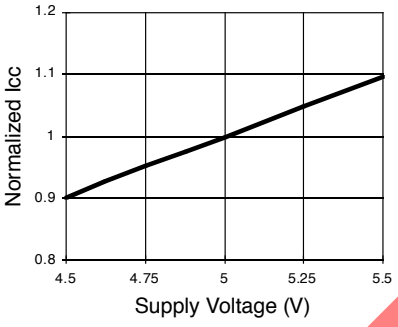
Voh vs Ioh



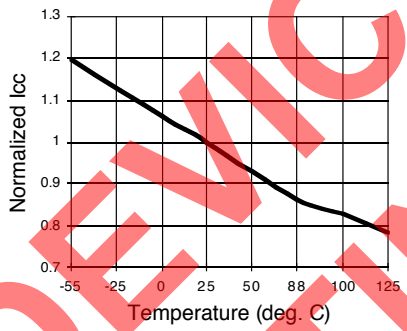
Voh vs Ioh



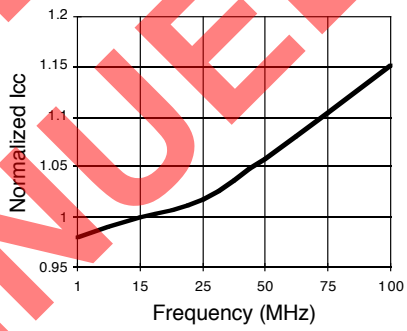
Normalized Icc vs Vcc



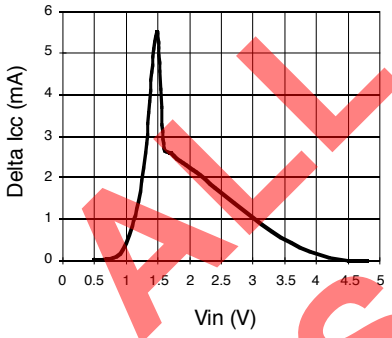
Normalized Icc vs Temp



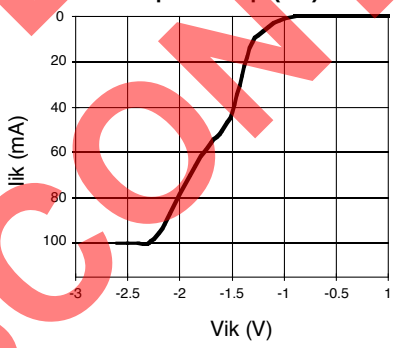
Normalized Icc vs Freq



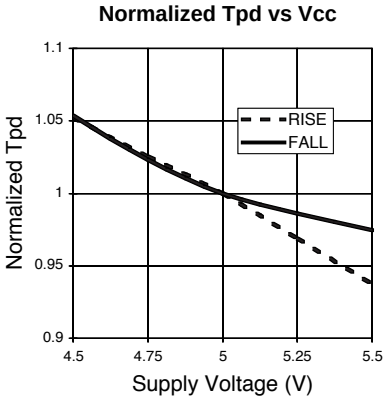
Delta Icc vs Vin (1 input)

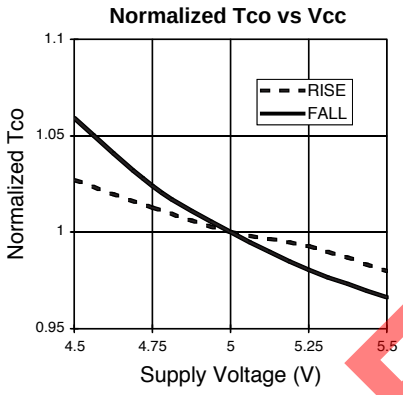


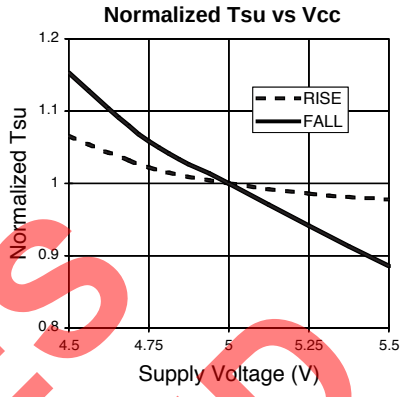
Input Clamp (Vik)

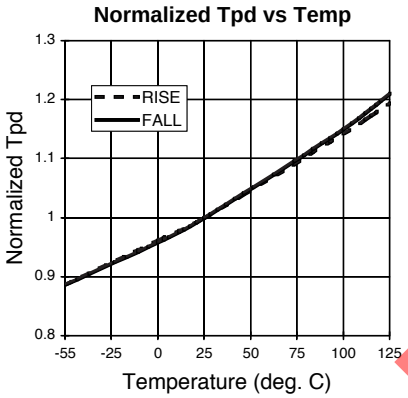


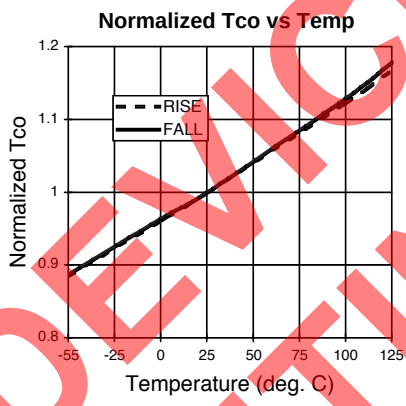
GAL22V10D-7/10L (PDIP): Typical AC and DC Characteristic Diagrams

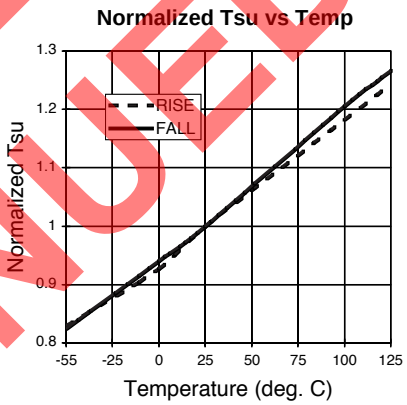


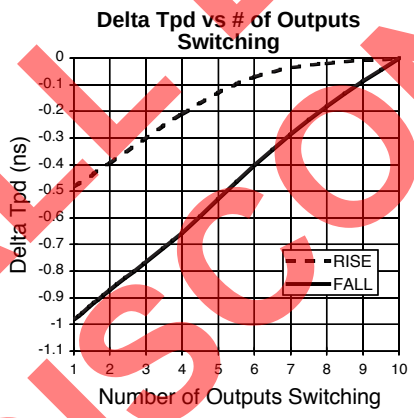


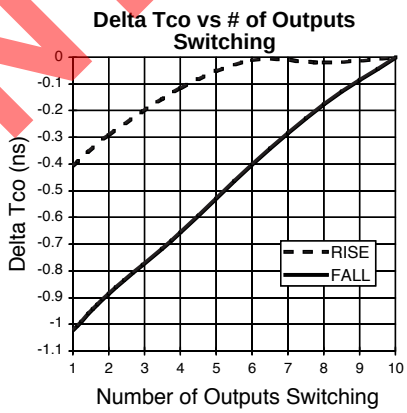


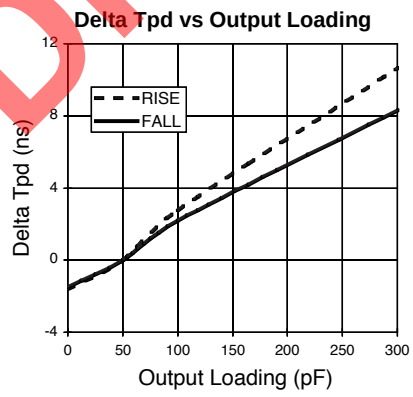


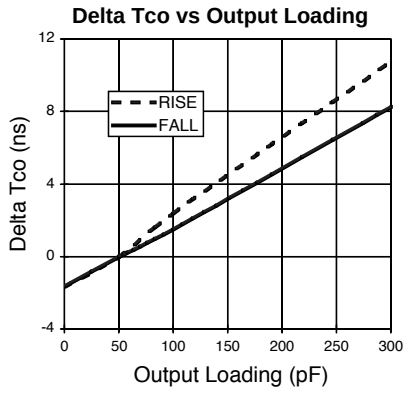






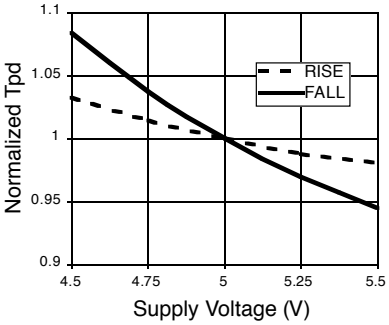




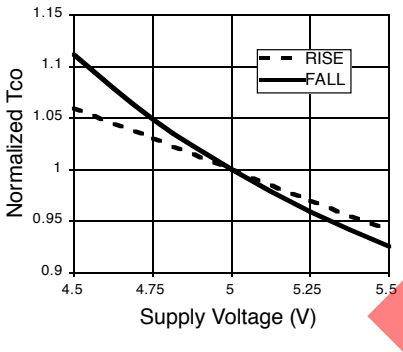


GAL22V10D-10Q and Slower (L & Q): Typical AC and DC Characteristic Diagrams

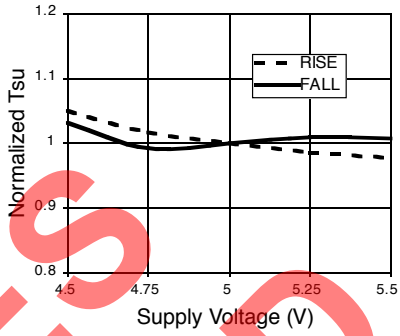
Normalized Tpd vs Vcc



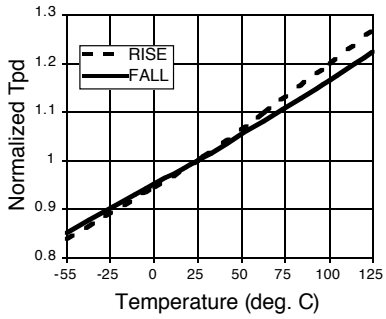
Normalized Tco vs Vcc



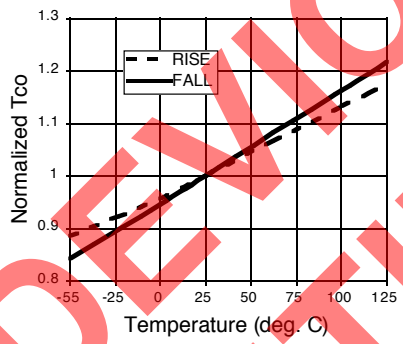
Normalized Tsu vs Vcc



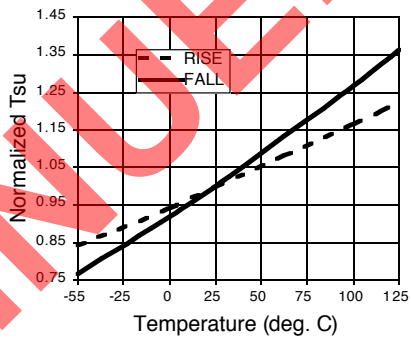
Normalized Tpd vs Temp



Normalized Tco vs Temp

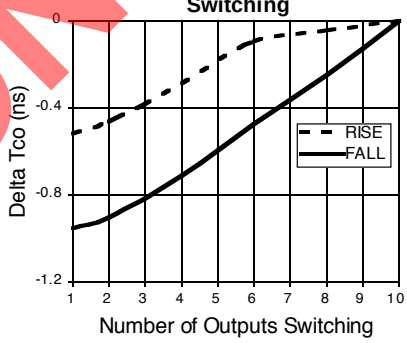


Normalized Tsu vs Temp

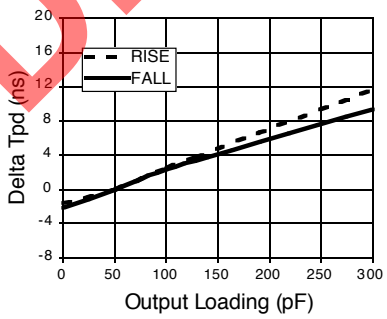


Delta Tpd vs # of Outputs Switching

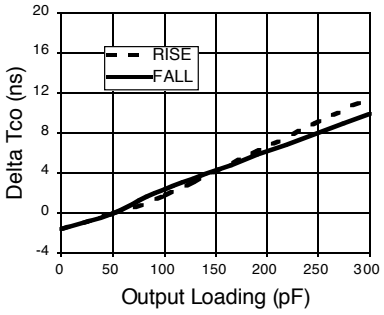
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

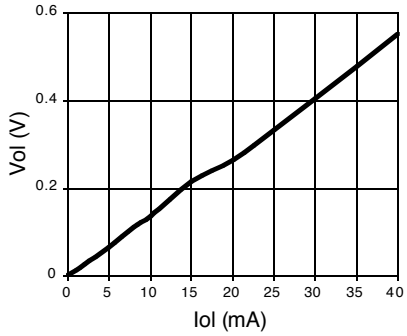


Delta Tco vs Output Loading

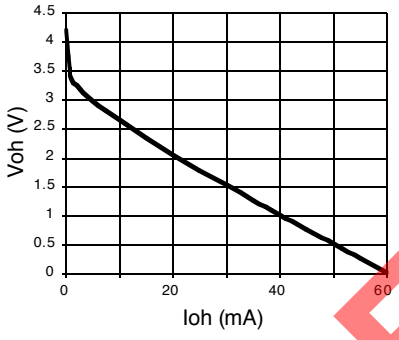


GAL22V10D-10Q and Slower (L & Q): Typical AC and DC Characteristic Diagrams

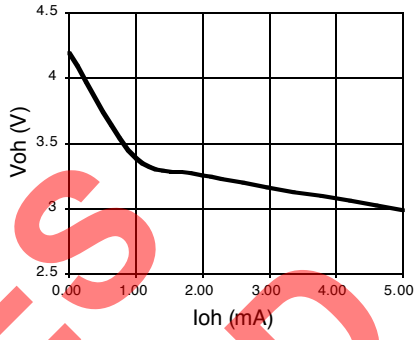
Vol vs Iol



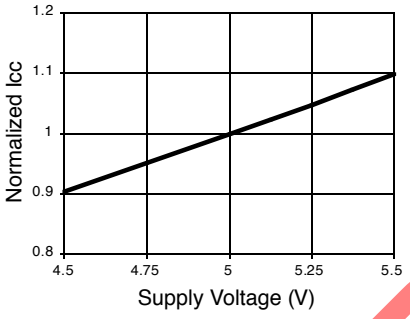
Voh vs Ioh



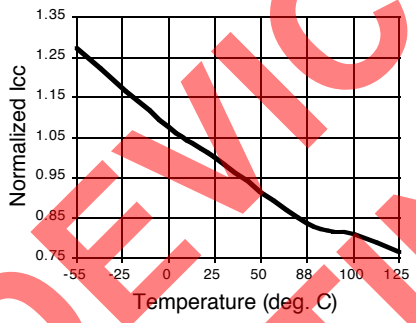
Voh vs Ioh



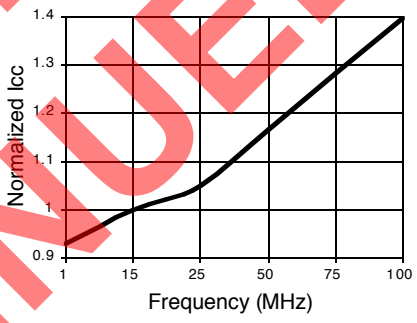
Normalized Icc vs Vcc



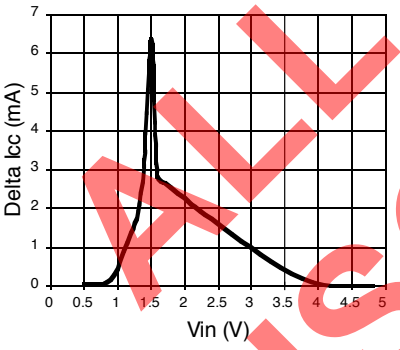
Normalized Icc vs Temp



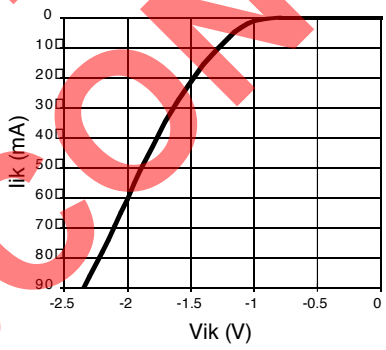
Normalized Icc vs Freq



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Revision History

Date	Version	Change Summary
-	22v10_08	Previous Lattice release.
August 2004	22v10_09	Added lead-free package options.
July 2006	22v10_10	Corrected SOIC pin configuration diagram. Pin 13.
August 2006	22v10_11	Updated for lead-free package options.
December 2006	22v10_12	Corrected Icc in the Ordering Part Number section on pages 2-3.