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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg980f512g-e-qfp100

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.1.27 Operational Amplifier (OPAMP)

The EFM32GG980 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.28 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSETM), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.29 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32GG980 to keep track of time and retain data, even if the main power source should drain out.

2.1.30 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.31 General Purpose Input/Output (GPIO)

In the EFM32GG980, there are 81 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.1.32 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x34 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

2.2 Configuration Summary

The features of the EFM32GG980 is a subset of the feature set described in the EFM32GG Reference Manual. Table 2.1 (p. 8) describes device specific implementation of the features.

3.4.3 EM4 Current Consumption





3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Тур	Max	Unit
tem10	Transition time from EM1 to EM0		0		HF- CORE- CLK cycles
t _{EM20}	Transition time from EM2 to EM0		2		μs
t _{EM30}	Transition time from EM3 to EM0		2		μs
t _{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

The EFM32GG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Тур	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
		T _{AMB} <150°C	10000			h
RET _{FLASH}	Flash data retention	T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) pro- gramming time		20			μs
	Page erase time	LPERASE == 0	20	20.4	20.8	ms
PERASE		LPERASE == 1	40	40.4	40.8	ms
t _{DERASE}	Device erase time				161.6	ms
	Frase current	LPERASE == 0			14 ¹	mA
'ERASE	Elase cullent	LPERASE == 1			7 ¹	mA
	Write ourrept	LPWRITE == 0			14 ¹	mA
WRITE	vvrite current	LPWRITE == 1			7 ¹	mA
V _{FLASH}	Supply voltage dur- ing flash erase and write		1.98		3.8	V

¹Measured at 25°C

3.8 General Purpose Input Output

Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
		Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
	Output high volt- age (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
VIOOH		Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
		Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V



Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = STANDARD





GPIO_Px_CTRL DRIVEMODE = HIGH



Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
f _{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR _{LFXO}	Supported crystal equivalent series re- sistance (ESR)			30	120	kOhm
C _{LFXOL}	Supported crystal external load range		X ¹		25	pF
DC _{LFXO}	Duty cycle		48	50	53.5	%
I _{LFXO}	Current consump- tion for core and buffer after startup.	ESR=30 kOhm, C _L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t _{LFXO}	Start- up time.	ESR=30 kOhm, C _L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

¹See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
f _{HFXO}	Supported nominal crystal Frequency		4		48	MHz
	Supported crystal	Crystal frequency 48 MHz			50	Ohm
ESR _{HFXO}	equivalent series re-	Crystal frequency 32 MHz		30	60	Ohm
	sistance (ESR)	Crystal frequency 4 MHz		400	1500	Ohm
9 _{mHFXO}	The transconduc- tance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C _{HFXOL}	Supported crystal external load range		5		25	pF
	Current consump-	4 MHz: ESR=400 Ohm, C _L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μA
IHFXO	startup	32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μA
t _{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μs



Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature



3.9.5 AUXHFRCO

Table 3.12. AUXHFRCO

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
	Oscillation frequen-	14 MHz frequency band	13.7	14.0	14.3	MHz
IAUXHFRCO	Cy, v _{DD} = 3.0 v, T _{AMB} =25°C	11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48 ¹	6.60 ¹	6.72 ¹	MHz
1		1 MHz frequency band	1.15 ²	1.20 ²	1.25 ²	MHz
t _{AUXHFRCO_settlir}	_g Settling time after start-up	f _{AUXHFRCO} = 14 MHz		0.6		Cycles
DC _{AUXHFRCO}	Duty cycle	f _{AUXHFRCO} = 14 MHz	48.5	50	51	%
TUNESTEP _{AU>} HFRCO	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

 2 For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		67		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	63	66		dB
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		70		dB
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
SINAD _{ADC}	SIgnal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		68		dB
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	65		dB







Figure 3.24. ADC Temperature sensor readout



3.11 Digital Analog Converter (DAC)

Table 3.15. DAC

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
M	Output voltage	VDD voltage reference, single ended	0		V _{DD}	V
V DACOUT	range	VDD voltage reference, differ- ential	-V _{DD}		V _{DD}	V
V _{DACCM}	Output common mode voltage range		0		V _{DD}	V
	Active current in-	500 kSamples/s, 12 bit		400 ¹	600 ¹	μA
I _{DAC}	cluding references	100 kSamples/s, 12 bit		200 ¹	260 ¹	μA
	for 2 channels	1 kSamples/s 12 bit NORMAL		17 ¹	25 ¹	μA
SR _{DAC}	Sample rate				500	ksam- ples/s
	DAC clock frequen- cy	Continuous Mode			1000	kHz
f _{DAC}		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
CYC _{DACCONV}	Clock cyckles per conversion			2		
t _{DACCONV}	Conversion time		2			μs
t _{DACSETTLE}	Settling time			5		μs
		500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		58		dB
SNR _{DAC}	Signal to Noise Ra- tio (SNR)	500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		58		dB



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	17	μA
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
G _{OL}	Open Loop Gain	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
GBW _{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, CL=75 pF		64		0
PM _{OPAMP}	Phase Margin	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, CL=75 pF		58		o
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		o
R _{INPUT}	Input Resistance			100		Mohm
R _{LOAD}	Load Resistance		200			Ohm
I _{LOAD_DC}	DC Load Current				11	mA
V		OPAxHCMDIS=0	V _{SS}		V _{DD}	V
VINPU1	input voltage	OPAxHCMDIS=1	V _{SS}		V _{DD} -1.2	V
V _{OUTPUT}	Output Voltage		V _{SS}		V _{DD}	V
Maria	Input Offeet Veltage	Unity Gain, V _{SS} <v<sub>in<v<sub>DD, OPAxHCMDIS=0</v<sub></v<sub>	-13	0	11	mV
VOFFSET	input Onset Voltage	Unity Gain, V _{SS} <v<sub>in<v<sub>DD-1.2, OPAxHCMDIS=1</v<sub></v<sub>		1		mV
V _{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/µs
SR _{OPAMP}	Slew Rate	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/µs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/µs
N		V _{out} =1V, RESSEL=0, 0.1 Hz <f<10 khz,="" opax-<br="">HCMDIS=0</f<10>		101		μV _{RMS}
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz <f<10 khz,="" opax-<br="">HCMDIS=1</f<10>		141		μV _{RMS}



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		V _{out} =1V, RESSEL=0, 0.1 Hz <f<1 mhz,="" opaxhcmdis="0</td"><td></td><td>196</td><td></td><td>μV_{RMS}</td></f<1>		196		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz <f<1 mhz,="" opaxhcmdis="1</td"><td></td><td>229</td><td></td><td>μV_{RMS}</td></f<1>		229		μV _{RMS}
		RESSEL=7, 0.1 Hz <f<10 khz,<br="">OPAxHCMDIS=0</f<10>		1230		μV _{RMS}
		RESSEL=7, 0.1 Hz <f<10 khz,<br="">OPAxHCMDIS=1</f<10>		2130		μV _{RMS}
		RESSEL=7, 0.1 Hz <f<1 mhz,<br="">OPAxHCMDIS=0</f<1>		1630		μV _{RMS}
		RESSEL=7, 0.1 Hz <f<1 mhz,<br="">OPAxHCMDIS=1</f<1>		2590		μV _{RMS}





Figure 3.26. OPAMP Positive Power Supply Rejection Ratio





Figure 3.34. EBI Read Enable Related Timing Requirements



Table 3.22. EBI Read Enable Related Timing Requirements

Symbol	Parameter	Min	Тур	Max	Unit
t _{SU_REn 1234}	Setup time, from EBI_AD valid to trailing EBI_REn edge	37			ns
t _{H_Ren} ^{1 2 3 4}	Hold time, from trailing EBI_REn edge to EBI_AD invalid	-1			ns

¹Applies for all addressing modes (figure only shows D16A8).

²Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

³Applies for all polarities (figure only shows active low signals)

 4 Measurement done at 10% and 90% of V_{DD} (figure shows 50% of _{VDD})

Figure 3.35. EBI Ready/Wait Related Timing Requirements



Table 3.23. EBI Ready/Wait Related Timing Requirements

Symbol	Parameter	Min	Тур	Мах	Unit
t _{SU_ARDY} ¹²³⁴	Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	37 + (3 * t _{HFCORECLK})			ns



Symbol	Parameter	Min	Тур	Мах	Unit
t _{H_ARDY} ¹²³⁴	Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	-1			ns

¹Applies for all addressing modes (figure only shows D16A8.)

²Applies for EBI_REn, EBI_WEn (figure only shows EBI_REn)

³Applies for all polarities (figure only shows active low signals)

 $^4\text{Measurement}$ done at 10% and 90% of V_{DD} (figure shows 50% of $_{\text{VDD}})$

3.16 LCD

Table 3.24. LCD

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
f _{LCDFR}	Frame rate		30		200	Hz
NUM _{SEG}	Number of seg- ments supported			34×8		seg
V _{LCD}	LCD supply voltage range	Internal boost circuit enabled	2.0		3.8	V
I _{LCD}		Display disconnected, stat- ic mode, framerate 32 Hz, all segments on.		250		nA
	Steady state current consumption.	Display disconnected, quadru- plex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register.		550		nA
	Steady state Cur- rent contribution of internal boost.	Internal voltage boost off		0		μA
I _{LCDBOOST}		Internal voltage boost on, boosting from 2.2 V to 3.0 V.		8.4		μA
		VBLEV of LCD_DISPCTRL register to LEVEL0		3.02		V
	Boost Voltage	VBLEV of LCD_DISPCTRL register to LEVEL1		3.15		V
		VBLEV of LCD_DISPCTRL register to LEVEL2		3.28		V
		VBLEV of LCD_DISPCTRL register to LEVEL3		3.41		V
VBOOST		VBLEV of LCD_DISPCTRL register to LEVEL4		3.54		V
		VBLEV of LCD_DISPCTRL register to LEVEL5		3.67		V
		VBLEV of LCD_DISPCTRL register to LEVEL6		3.73		V
		VBLEV of LCD_DISPCTRL register to LEVEL7		3.74		V

The total LCD current is given by Equation 3.3 (p. 49) . I_{LCDBOOST} is zero if internal boost is off.

Total LCD Current Based on Operational Mode and Internal Boost

 $I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST}$

(3.3)

Figure 3.37. SPI Slave Timing



Table 3.29. SPI Slave Timing

Symbol	Parameter	Min	Тур	Max	Unit
t _{SCLK_} sl ^{1 2}	SCKL period	2 * t _{HFPER-} CLK			ns
t _{SCLK_hi} ^{1 2}	SCLK high period	3 * t _{HFPER-} CLK			ns
t _{SCLK_lo} ^{1 2}	SCLK low period	3 * t _{HFPER-} CLK			ns
t _{CS_ACT_MI} ¹²	CS active to MISO	4.00		30.00	ns
t _{CS_DIS_MI} ¹²	CS disable to MISO	4.00		30.00	ns
t _{SU_MO} ¹²	MOSI setup time	4.00			ns
t _{H_MO} ^{1 2}	MOSI hold time	2 + 2* t _{HF-} PERCLK			ns
t _{SCLK_MI} ¹²	SCLK to MISO	9 + t _{HFPER-} CLK		36 + 2*t _{HF-} PERCLK	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

 $^2\text{Measurement}$ done at 10% and 90% of V_{DD} (figure shows 50% of $\text{V}_{\text{DD}})$

3.19 USB

The USB hardware in the EFM32GG980 passes all tests for USB 2.0 Full Speed certification. See the test-report distributed with application note "AN0046 - USB Hardware Design Guide".

3.20 Digital Peripherals

Table 3.30. Digital Peripherals

Symbol	Parameter	Condition	Min	Тур	Max	Unit
I _{USART}	USART current	USART idle current, clock en- abled		4.9		µA/ MHz
I _{UART}	UART current	UART idle current, clock en- abled		3.4		µA/ MHz
I _{LEUART}	LEUART current	LEUART idle current, clock en- abled		140		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		6.1		µA/ MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32GG980.

4.1 Pinout

The *EFM32GG980* pinout is shown in Figure 4.1 (p. 54) and Table 4.1 (p. 54). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32GG980 Pinout (top view, not to scale)



Table 4.1. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other				
1	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	I2C0_SDA #0 LEU0_RX #4	PRS_CH0 #0 GPIO_EM4WU0				
2	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0				
3	PA2	LCD_SEG15	EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0				



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Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / out- put pin 15.
EBI_ALE		PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control in- put.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchroniza- tion pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn		PF8						External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as exter- nal optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF ca- pacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF ca- pacitor between LCD_BCAP_N and LCD_BCAP_P.



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Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
U0_TX	PF6	PE0	PA3					UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX		PF11	PB10	PE3				UART1 Receive input.
U1_TX		PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO)
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit.Also used as receive in- put in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit.Also used as receive in- put in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit.Also used as receive in- put in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and reg- ulator output

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32GG980* is shown in Table 4.3 (p. 66). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

65

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