Infineon Technologies - CYPD2103-20FNXIT Datasheet

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What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32kB)
Controller Series	-
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	9
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFBGA, WLCSP
Supplier Device Package	20-WLCSP (1.63x2.03)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd2103-20fnxit

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

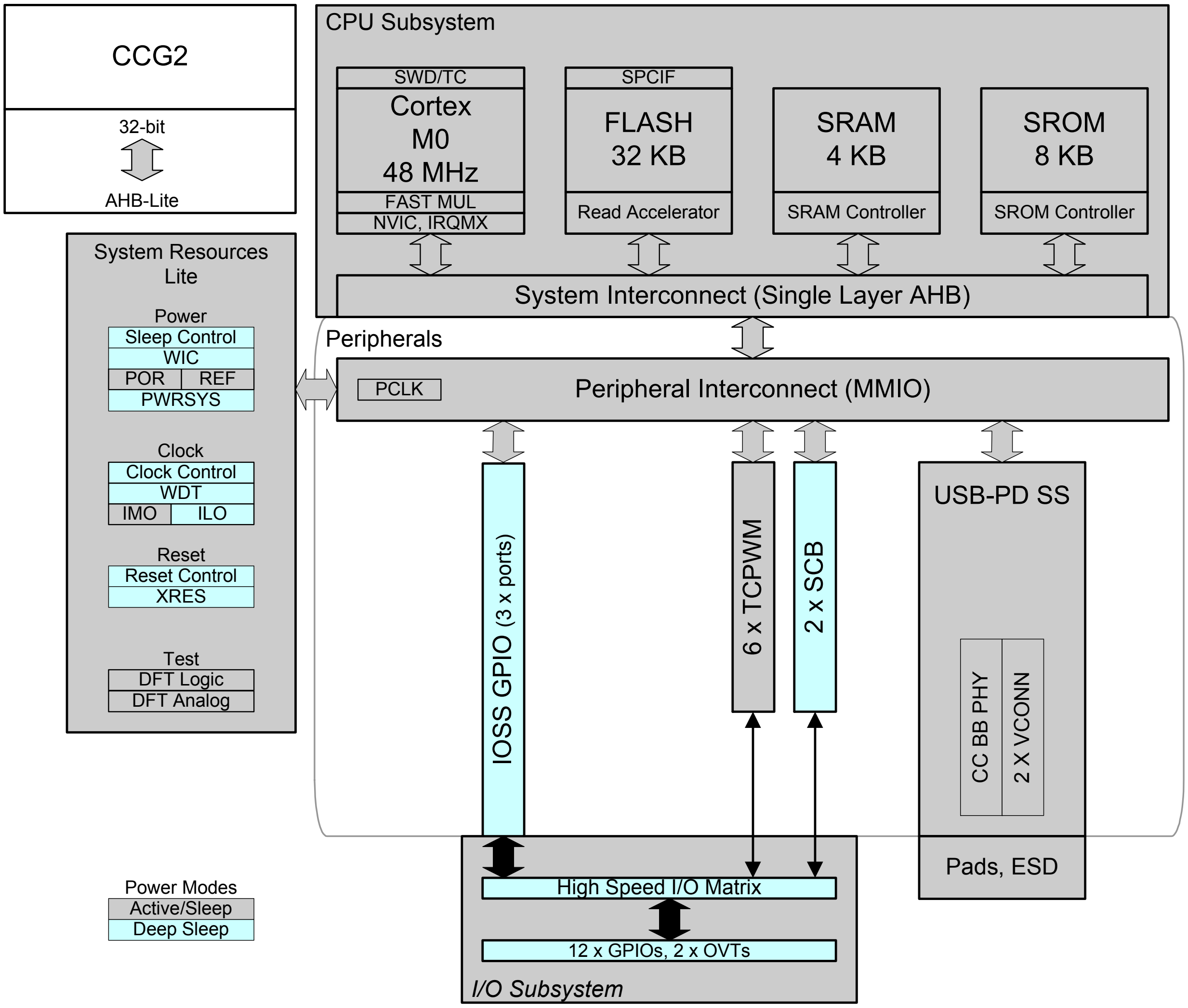
1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility

Figure 1. EZ-PD CCG2 Block Diagram



Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG2 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG2 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

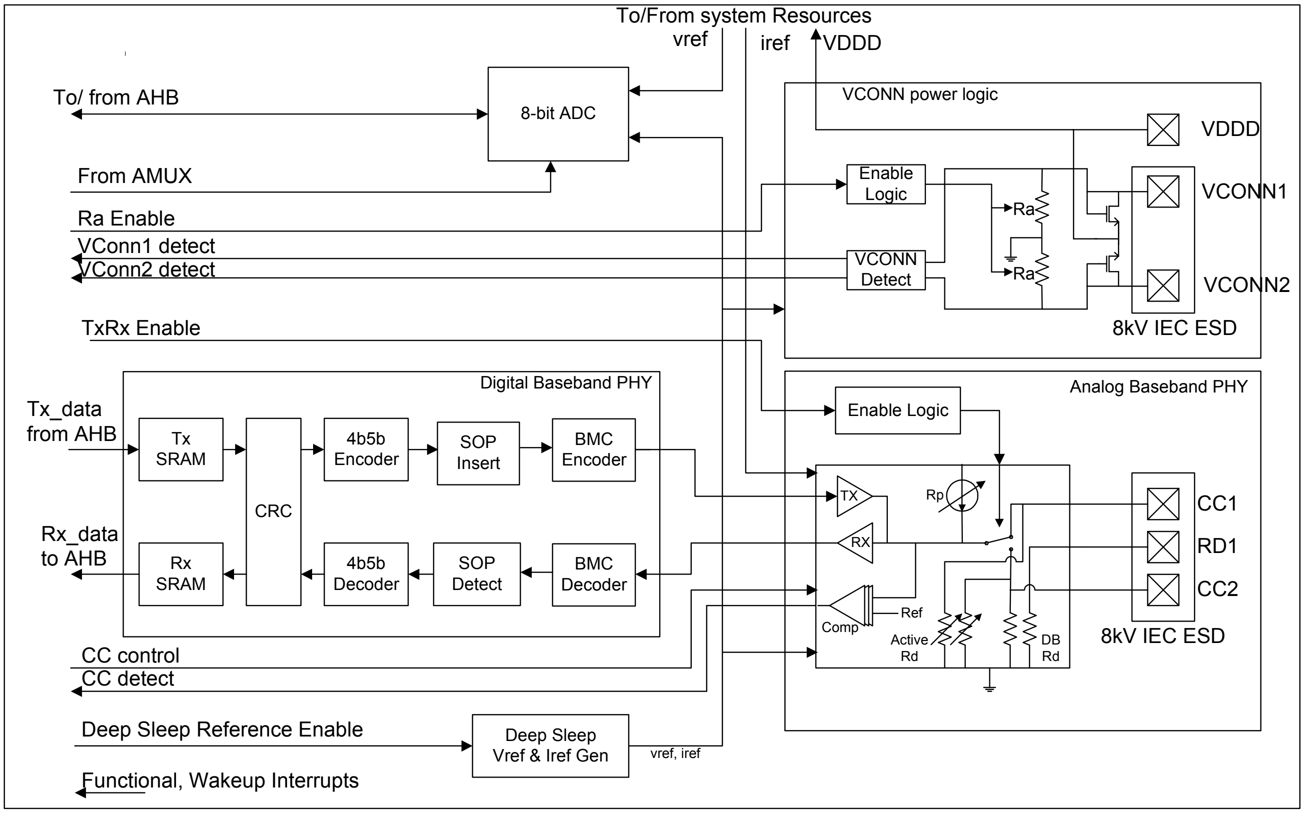
A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

EZ-PD CCG2 has a USB-PD subsystem consisting of a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V front end. This subsystem integrates the required termination resistors to identify the role of the EZ-PD CCG2 solution. R_A is used to identify EZ-PD CCG2 as an accessory or an electronically marked cable. R_D is used to identify EZ-PD CCG2 as a UFP in a hybrid cable or a dongle. When configured as a DFP, integrated current sources perform the role of R_P or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the Type-C spec. EZ-PD CCG2 responds to all USB-PD communication. The EZ-PD CCG2 USB-PD sub-system can be configured to respond to SOP, SOP', or SOP” messaging.

The USB-PD sub-system contains a 8-bit SAR (Successive Approximation Register) ADC for analog to digital conversions. The ADC includes a 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global Analog Multiplex Busses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use. The CC1, CC2 and RD1 pins are not available to connect to the mux busses.

Figure 2. USB-PD Subsystem



System Resources

Power System

The power system is described in detail in the section Power on page 9. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). EZ-PD CCG2 can operate from three different power sources over the range of 2.7 to 5.5 V and has three different power modes, transitions between which are managed by the power system. EZ-PD CCG2 provides Sleep and Deep Sleep low-power modes.

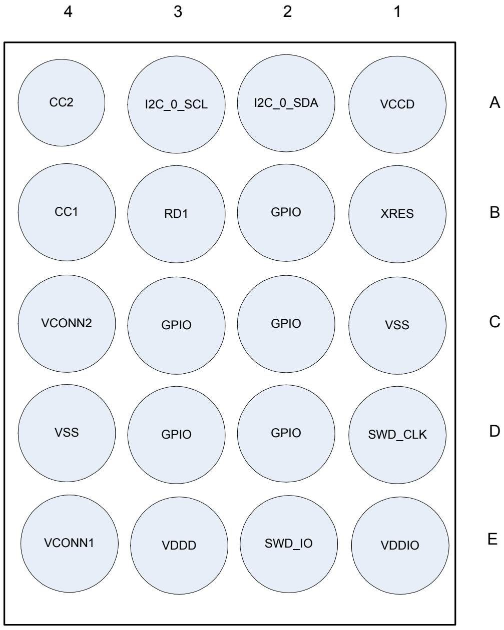
Clock System

The clock system for EZ-PD CCG2 consists of the Internal Main Oscillator (IMO) and the Internal Low-power Oscillator (ILO).

Pinouts

Group	Name	Pin Map 24-QFN	Ball Location 20-CSP	Pin Map 14-DFN	Description
USB Type-C Port	CC1	2	B4	3	USB PD connector detect/Configuration Channel 1
	CC2	1	A4	N/A	USB PD connector detect/Configuration Channel 2
	RD1	3	B3	N/A	Dedicated Rd resistor pin for CC1 Must be left open for cable applications and connected together with CC1 ball for UFP or DFP with dead battery applications
GPIOs and serial interfaces	GPIO	22	C3	N/A	GPIO / SPI_0_CLK / UART_0_ RX
	GPIO	18	D3	13	GPIO / SPI_0_MOSI / UART_0_TX
	GPIO	13	C2	10	GPIO / I2C_1_SDA / SPI_1_MISO / UART_1_RX
	GPIO	10	D2	N/A	GPIO / I2C_1_SCL / SPI_1_CLK / UART_1_TX
	GPIO	15	B2	11	GPIO / SPI_1_SEL / UART_1_RTS
	GPIO	14	N/A	N/A	GPIO
	GPIO	17	N/A	N/A	GPIO
	GPIO	21	N/A	N/A	GPIO
	GPIO	23	N/A	N/A	GPIO
	GPIO	24	N/A	N/A	GPIO
	I2C_0_SCL	20	A3	1	GPIO / I2C_0_SCL / SPI_0_MISO / UART_0_RTS
	I2C_0_SDA	19	A2	14	GPIO / I2C_0_SDA / SPI_0_SEL / UART_0_CTS
	SWD _IO	11	E2	8	SWD IO / GPIO / UART_1_CTS / SPI_1_MOSI
	SWD_CLK	12	D1	9	SWD clock / GPIO
RESET	XRES	16	B1	12	Reset input
POWER	VCONN1	5	E4	5	VCONN 1 input (4.0 V to 5.5 V)
	VCONN2	4	C4	4	VCONN 2 input (4.0 V to 5.5 V)
	VDDIO	8	E1	N/A	1.71-V to 5.5-V supply for I/Os
	VCCD	7	A1	6	1.8-V regulator output for filter capacitor
	VDDD	9	E3	7	VDDD supply input/output (2.7 V to 5.5 V)
	VDDD	6			VDDD supply input/output (2.7 V to 5.5 V)
	VSS	EPAD	N/A	EPAD	Ground supply
	VSS		D4	2	Ground supply
	VSS		C1		Ground supply

Figure 3. 20-ball WLCSP EZ-PD CCG2 Ball Map (Bottom (Balls Up) View)



	4	3	2	1
A	CC2	I2C_0_SCL	I2C_0_SDA	VCCD
B	CC1	RD1	GPIO	XRES
C	VCONN2	GPIO	GPIO	VSS
D	VSS	GPIO	GPIO	SWD_CLK
E	VCONN1	VDDD	SWD_IO	VDDIO

Figure 4. 14-pin DFN Pin Map (Top View)

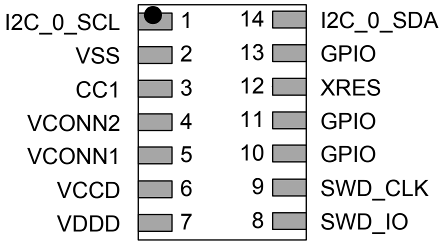


Figure 5. 24-Pin QFN Pin Map (Top View)

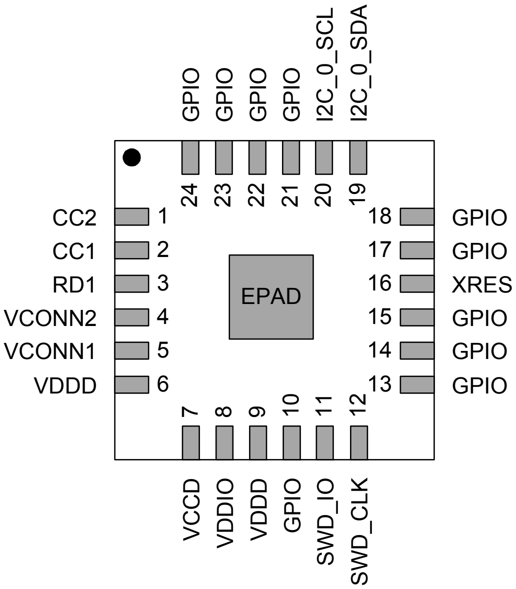


Figure 10 shows a Notebook DRP application diagram using a CCG2 device. The Type-C port can be used as a power provider or a power consumer. The CCG2 device communicates with the Embedded controller (EC) over I^2C. It also controls the Data Mux to route the High Speed signals either to the USB chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode). The SBU lines, SuperSpeed and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

Optional FETs are provided for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. A VBUS_DISCHARGE FET controlled by CCG2 device is used to quickly discharge VBUS after the Type-C connection is detached.

Figure 10. Dual Role Port (DRP) Application

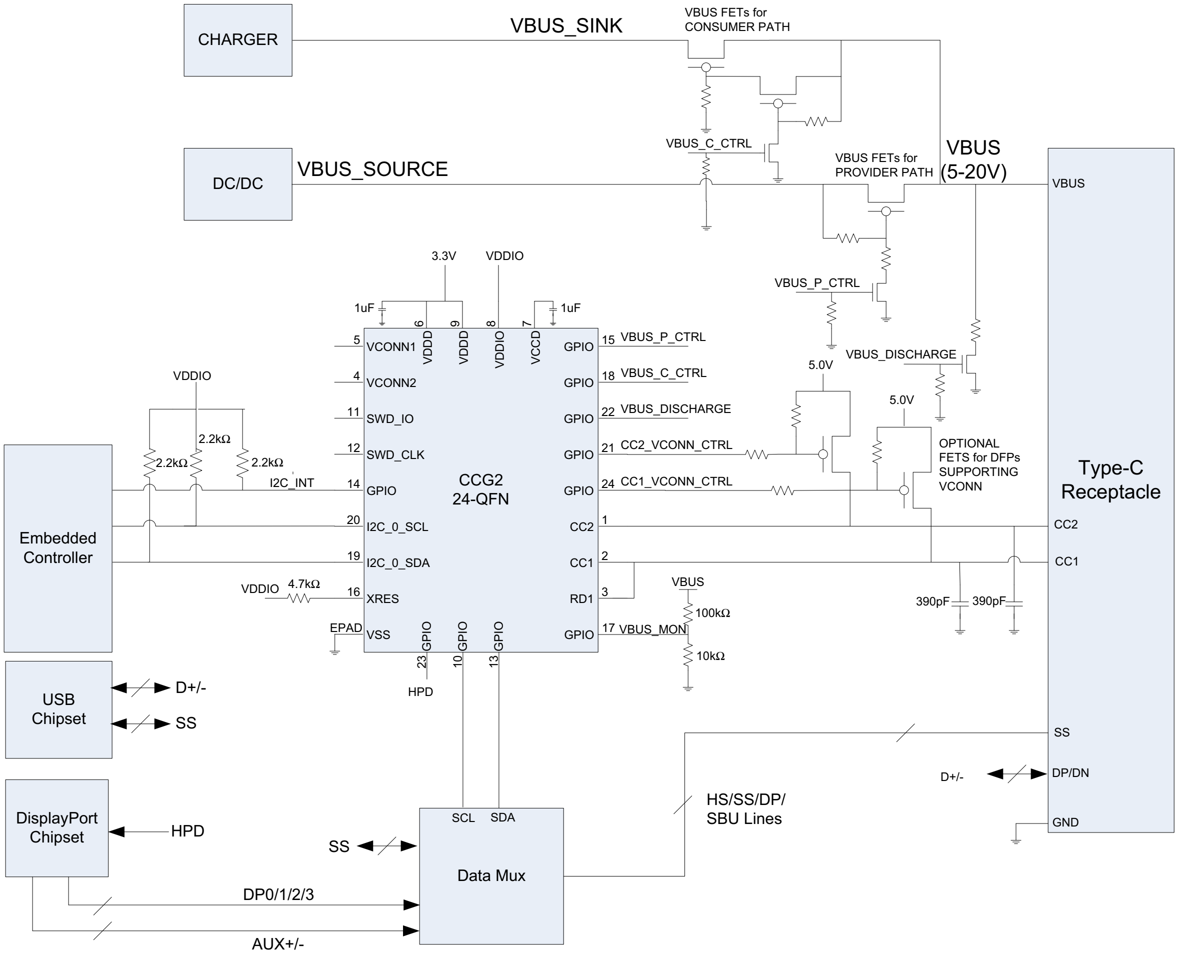


Figure 12 shows a USB Type-C to HDMI/DVI/VGA adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has HDMI/DVI/VGA interface. It enables users of any Notebook that implements USB-Type C to connect to other display types.

This application has a Type-C plug on one end and the legacy video (HDMI/DVI/VGA) receptacle on the other end. This application meets the requirements described in Section 4.3 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0. This application supports display output at a resolution of up to 4K Ultra HD (3840x2160) at 60 Hz. It also supports the USB Billboard Device Class, which is required by the USB PD specification for enumeration of any accessories that support Alternate Mode when connected to a host PC.

Figure 12. USB Type-C to HDMI/DVI/VGA Dongle Application Diagram

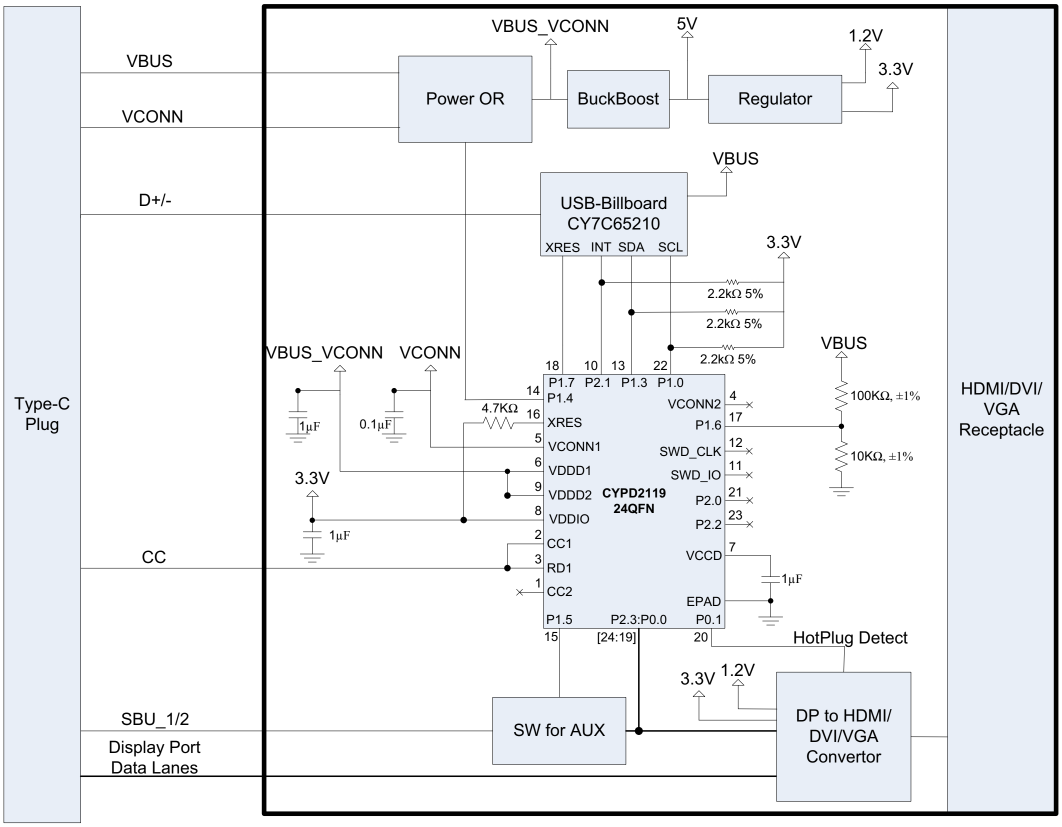


Figure 13 shows a USB Type-C to DisplayPort adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has a DisplayPort interface.

Figure 13 shows a Type-C plug on one end and a DP/mDP plug on the other end. The application meets the requirements described in Section 4.2 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0 (Scenarios 2a and 2b USB Type-C to DisplayPort Cables). It also supports the USB Billboard Device Class, which is required by the USB PD specification for enumeration of any accessories that support Alternate Mode when connected to a host PC.

Figure 13. USB Type-C to Display Port Application Diagram

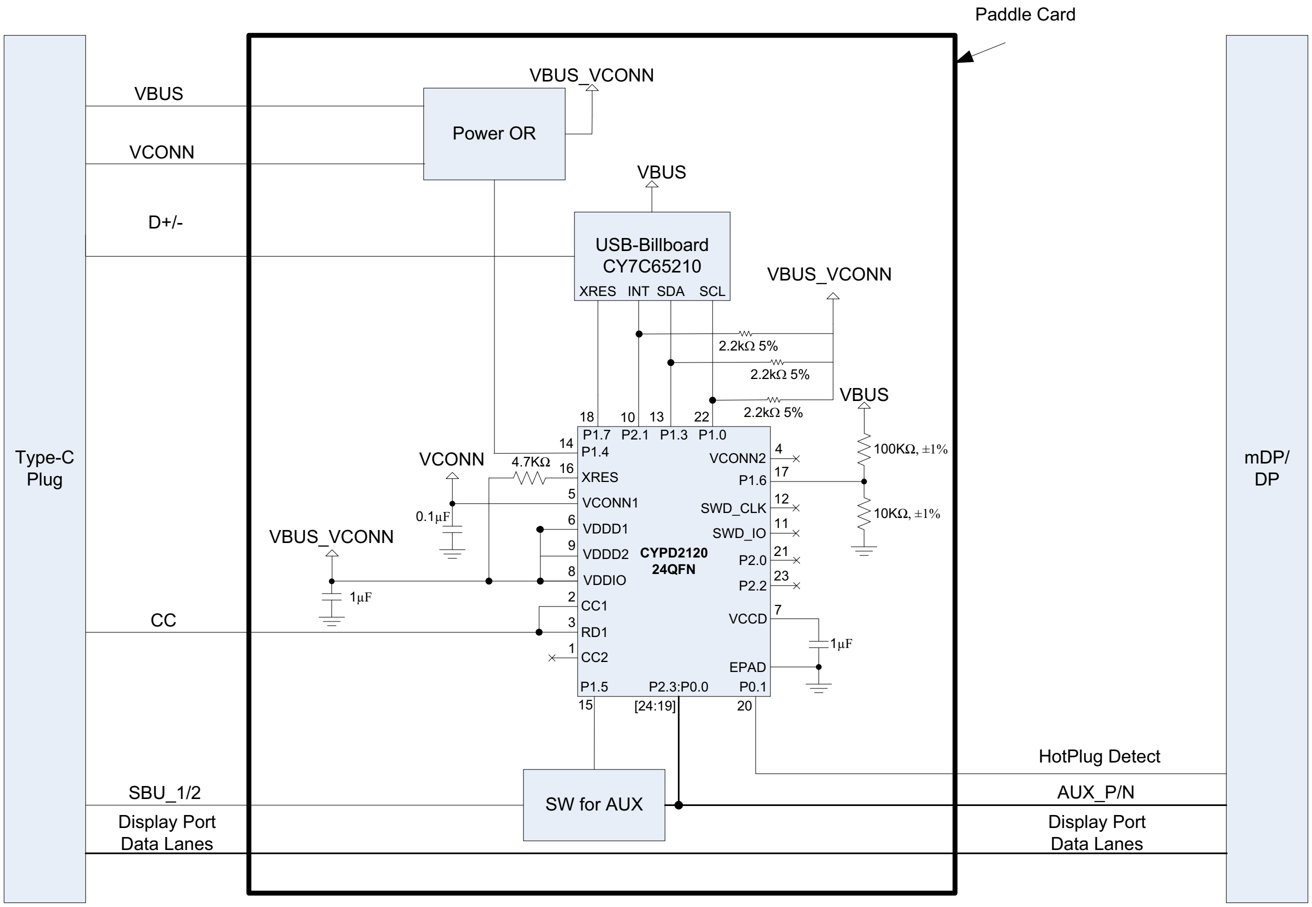
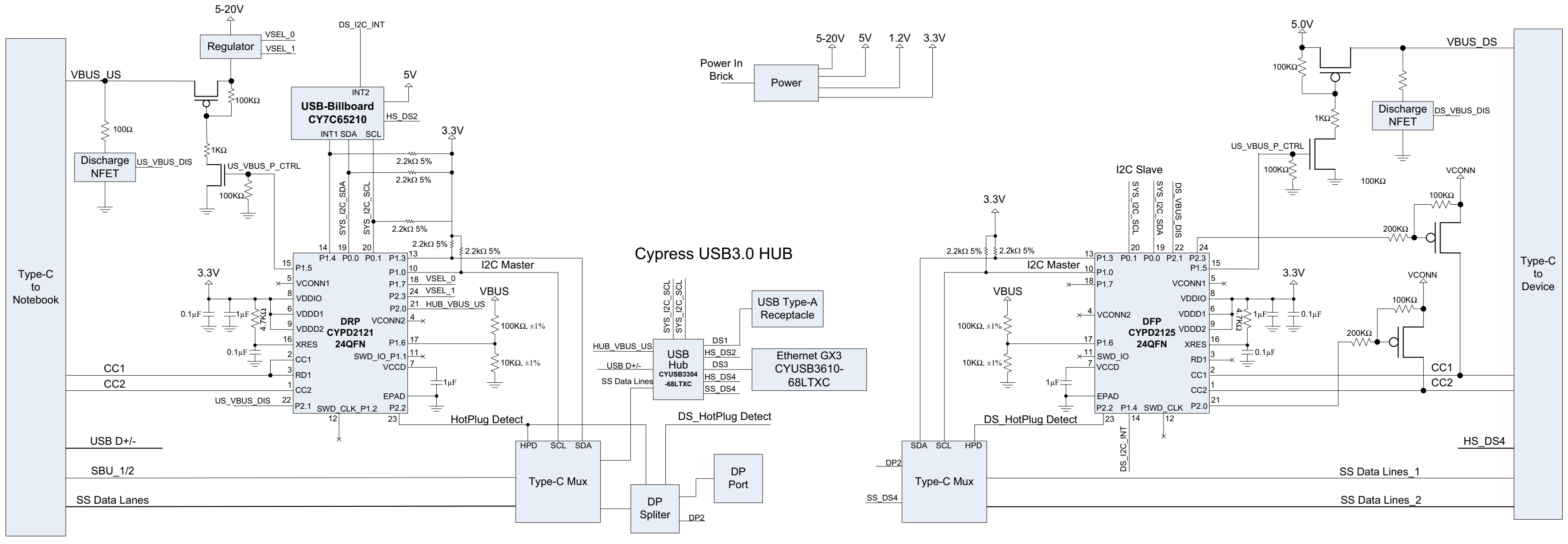


Figure 14 shows a CCG2 Monitor/Dock application diagram. It enables connectivity between a USB Type-C host system on the Upstream port and multiple Display/Data devices on the Downstream port. This application has a USB Type-C receptacle on the Upstream port, which supports data, power, and display. On the Downstream port, this application supports: USB Type-A, Gigabit Ethernet, DisplayPort, and USB Type-C receptacle.

The main features of this solution are:

- Powered from an external 24-V DC power adapter
- Provides up to 45 W (15 V at 3A) on the Upstream Type-C port and up to 15 W (5 V at 3A) on the Downstream USB Type-C port
- Provides simultaneous 4K display output with USB 3.1 Gen 1 on the USB Type-A port
- Four-lane display on the DisplayPort connector
- Multi-Stream support on DisplayPort and Downstream Type-C port
- USB 3.1 Gen 1 hub for USB port expansion
- Gigabit Ethernet using RJ45 connector
- Supports firmware upgrade of CCG2 controllers, HX3 Hub controller, and Billboard controller

Figure 14. CCG2 in Dock/Monitor Application Diagram



CCG2 connected on the Upstream Port

CCG2 connected on the Downstream Port

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{CONN1_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{CONN2_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	Absolute max
V_{CC_ABS}	Absolute max voltage for CC1 and CC2 pins	–	–	6	V	Absolute max
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VCONN1, and VCONN2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for pins CC1, CC2, VCONN1, and VCONN2

Note

1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	UFP Applications
SID.PWR#1_A	V_{DDD}	Power supply input voltage	3.0	–	5.5	V	DFP/DRP Applications
SID.PWR#23	V_{CONN1}	Power supply input voltage	4.0	–	5.5	V	–
SID.PWR#23_A	V_{CONN2}	Power supply input voltage	4.0	–	5.5	V	–
SID.PWR#13	V_{DDIO}	GPIO power supply	1.71	–	5.5	V	–
SID.PWR#24	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID.PWR#15	C_{EFC}	External regulator voltage bypass on V_{CCD}	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor on V_{DDD}	–	1	–	µF	X5R ceramic or better
SID.PWR#25		Power Supply Decoupling Capacitor on V_{CONN1} and V_{CONN2}	–	0.1	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 2.7 to 5.5 V. Typical values measured at V_{DD} = 3.3 V.							
SID.PWR#12	I_{DD12}	Supply current	–	7.5	–	mA	V_{CONN1} or V_{CONN2} = 5 V, T_A = 25 °C, CC I/O IN Transmit or Receive, R_A disconnected, no I/O sourcing current, CPU at 12 MHz
Sleep Mode, V_{DDD} = 2.7 to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup. WDT ON. IMO at 48 MHz	–	2.0	3.0	mA	V_{DDD} = 3.3 V, T_A = 25 °C, all blocks except CPU are ON, CC I/O ON, no I/O sourcing current
Deep Sleep Mode, V_{DDD} = 2.7 to 3.6 V (Regulator on)							
SID_DS_RA	$I_{DD\_DS\_RA}$	V_{CONN1} = 5.0, R_A termination disabled	–	100	–	µA	V_{CONN1}, V_{CONN2} = 5 V, T_A = 25 °C. R_A termination disabled on V_{CONN1} and V_{CONN2}, see SID.PD.7. VCONN leaker circuits turned off during deep sleep
SID34	I_{DD29}	V_{DDD} = 2.7 to 3.6 V. I^2C wakeup and WDT ON	–	50	–	µA	R_A switch disabled on V_{CONN1} and V_{CONN2}. V_{DDD} = 3.3 V, T_A = 25 °C
SID_DS	I_{DD_DS}	V_{DDD} = 2.7 to 3.6 V. CC wakeup ON	–	2.5	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P disabled
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	1	10	µA	–

Table 5. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF
SID71	T_{FALLF}	Fall time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF

XRES

Table 6. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	–	0.05 × V_{DDIO}	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 7. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	Fc	–	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	–	2/Fc	–	ns	For all Trigger Events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	–	2/Fc	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	–	1/Fc	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	–	1/Fc	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	–	1/Fc	–	ns	Minimum pulse width between quadrature-phase inputs

System Resources

Power-on-Reset (POR) with Brown Out

Table 17. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization

Table 18. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5	V	Guaranteed by characterization

SWD Interface

Table 19. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\ V \leq V_{DDIO} \leq 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$1.8\ V \leq V_{DDIO} \leq 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 20. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 21. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO}$	RMS jitter at 48 MHz	–	145	–	ps	Guaranteed by characterization
F_{IMO}	–	IMO frequency	24	–	48	MHz	–

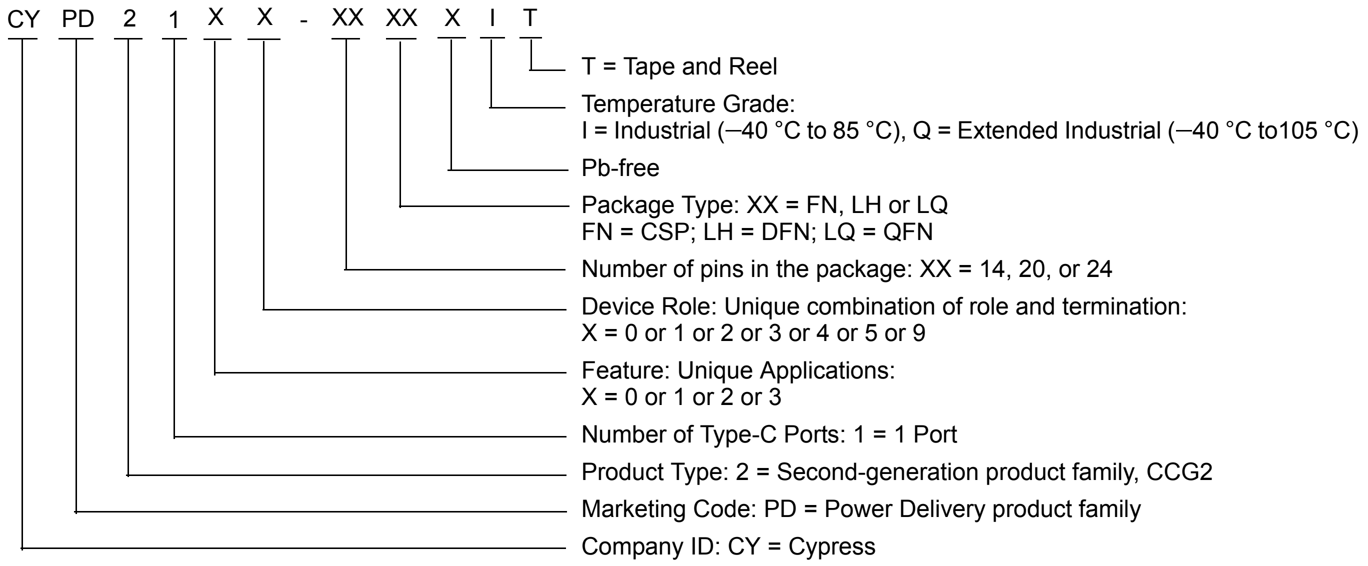
Ordering Information

The EZ-PD CCG2 part numbers and features are listed in Table 27.

Table 27. EZ-PD CCG2 Ordering Information

Part Number	Application	Type-C Ports	Termination Resistor	Role	Package
CYPD2103-20FNXIT	Cable	1	R_A[4]	Cable	20-ball CSP
CYPD2103-14LHXIT	Cable	1	R_A[4]	Cable	14-pin DFN
CYPD2104-20FNXIT	Accessory	1	R_D[5]	Accessory	20-ball CSP
CYPD2105-20FNXIT	Active Cable	1	R_A[4]	Active Cable	20-ball CSP
CYPD2119-24LQXIT	C-DP	1	R_D[5]	UFP	24-pin QFN
CYPD2120-24LQXIT	C-HDMI	1	R_D[5]	UFP	24-pin QFN
CYPD2121-24LQXIT	Dock/Monitor Upstream port	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2122-20FNXIT	Tablet	1	R_P[6], R_D[5]	DRP	20-ball CSP
CYPD2122-24LQXI	Notebook	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2122-24LQXIT	Notebook	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2125-24LQXIT	Dock/Monitor Downstream port	1	R_P[6]	DFP	24-pin QFN
CYPD2134-24LQXIT	DFP	1	R_P[6]	DFP	24-pin QFN
CYPD2134-24LQXQT	DFP	1	R_P[6]	DFP	24-pin QFN

Ordering Code Definitions



T = Tape and Reel

Temperature Grade:
I = Industrial (–40 °C to 85 °C), Q = Extended Industrial (–40 °C to105 °C)

Pb-free

Package Type: XX = FN, LH or LQ
FN = CSP; LH = DFN; LQ = QFN

Number of pins in the package: XX = 14, 20, or 24

Device Role: Unique combination of role and termination:
X = 0 or 1 or 2 or 3 or 4 or 5 or 9

Feature: Unique Applications:
X = 0 or 1 or 2 or 3

Number of Type-C Ports: 1 = 1 Port

Product Type: 2 = Second-generation product family, CCG2

Marketing Code: PD = Power Delivery product family

Company ID: CY = Cypress

Notes
4. Termination resistor denoting an EMCA.
5. Termination resistor denoting an accessory or upstream facing port.
6. Termination resistor denoting a downstream facing port.

Packaging

Table 28. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended Industrial			105	°C
T_J	Operating junction temperature	Industrial	–40	–	100	°C
		Extended Industrial			125	°C
T_{JA}	Package θ_{JA} (20-ball WLCSP)	–	–	66	–	°C/W
T_{JC}	Package θ_{JC} (20-ball WLCSP)	–	–	0.7	–	°C/W
T_{JA}	Package θ_{JA} (14-pin DFN)	–	–	31	–	°C/W
T_{JC}	Package θ_{JC} (14-pin DFN)	–	–	59	–	°C/W
T_{JA}	Package θ_{JA} (24-pin QFN)	–	–	22	–	°C/W
T_{JC}	Package θ_{JC} (24-pin QFN)	–	–	29	–	°C/W

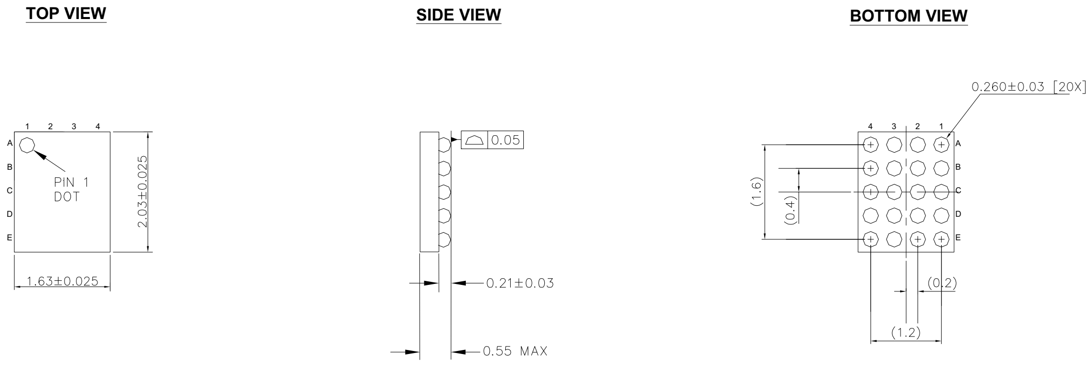
Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
20-ball WLCSP	260 °C	30 seconds
14-pin DFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds

Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
20-ball WLCSP	MSL 1
14-pin DFN	MSL 3
24-pin QFN	MSL 3

Figure 15. 20-ball WLCSP (1.63 × 2.03 × 0.55 mm) FN20B Package Outline, 001-95010

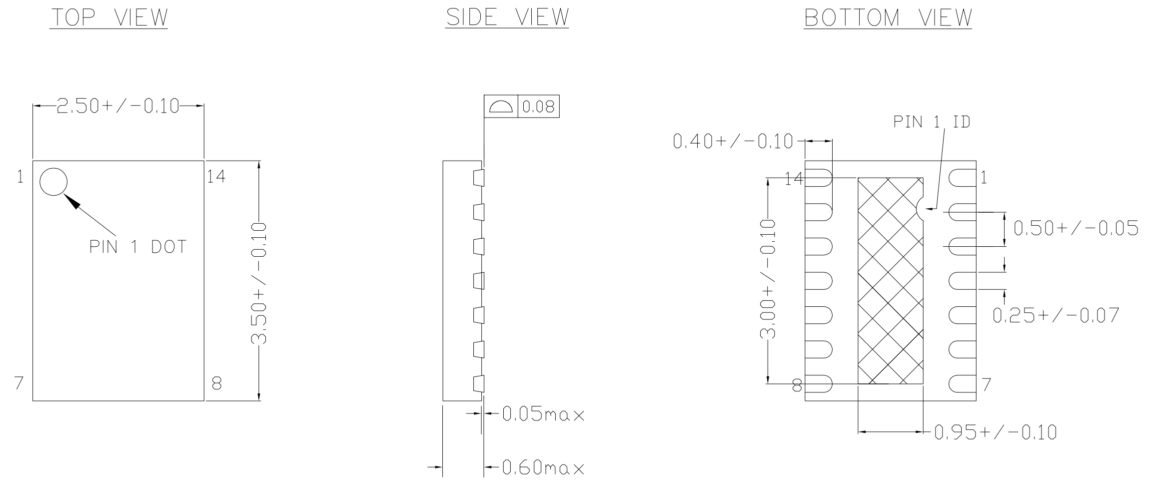


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-95010 *A

Figure 16. 14-pin DFN (2.5 × 3.5 × 0.6 mm), LH14A, 0.95 × 3.00 E-Pad (Sawn) Package Outline, 001-96312

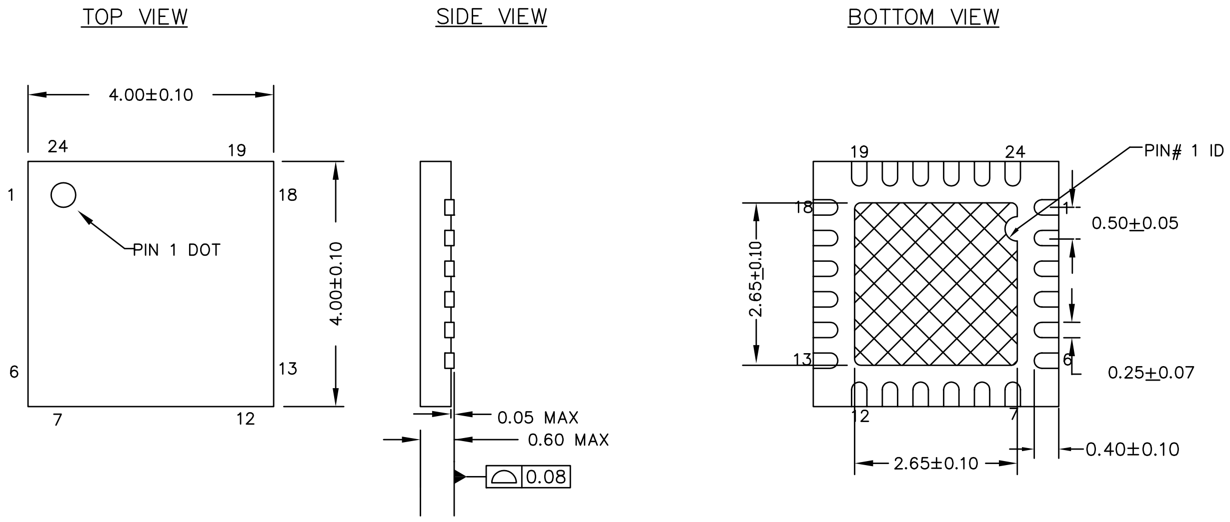


NOTES :

1. HATCH AREA IS SOLDERABLE EXPOSED METAL
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-96312 **

Figure 17. 24-Pin QFN (4 × 4 × 0.55 mm), LQ24A, 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937



NOTES :

1. ▨ HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Acronyms

Table 31. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG2	Cable Controller Generation 2
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
XRES	external reset I/O pin

References and Links To Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG3: USB Type-C Controller Datasheet
- CCG4: Two-Port USB Type-C Controller Datasheet

Document History Page

Description Title: EZ-PD™ CCG2 Datasheet USB Type-C Port Controller
Document Number: 001-93912

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	4680071	GAYA	03/07/2015	Release to web
*F	4718374	AKN	04/09/2015	Added 24-pin QFN pin and package information. Added DRP and DFP Application diagrams
*G	4774142	AKN	06/15/2015	Changed datasheet status from Preliminary to Final. Updated Logic Block Diagram. Changed number of GPIOs to 10 and added a note about the number of GPIOs varying depending on the package. Updated Power and Digital Peripherals section. Updated Application diagrams. Added SID.PWR#1_A parameter. Added CYPD2122-20FNXIT part in Ordering Information. Removed Errata.
*H	4979175	VGT	10/23/2015	Updated Figure 1 and Figure 5. Added VCC_ABS spec and updated the SID.ADC.4 parameter. Added “Guaranteed by characterization” note for the following specs: SID.GIO#16, SID.GIO#17, SID.XRES#3, SID 160 to SID 172A, SID 2226, SID 229, SID.ADC.1 to SID.ADC.5.
*I	5028128	VGT	12/04/2015	Updated Application Diagrams: Added Figure 12. Added Figure 13. Added Figure 14. Updated Ordering Information. Added part numbers CYPD2119-24LQXIT, CYPD2120-24LQXIT, CYPD2121-24LQXIT, CYPD2125-24LQXIT.
*J	5186972	VGT	03/28/2016	Updated temperature ranges in Features. Updated Table 28. Updated Ordering Information.
*K	5303957	VGT	06/13/2016	Added Available Firmware and Software Tools. Updated Figure 8: Per the USB PD3.0 spec, SOP” implementation is no longer valid for passive cables. Updated Figure 9, Figure 10, and Figure 11. Added descriptive notes for the application diagrams. Added References and Links To Applications Collaterals. Updated Ordering Information. Updated Cypress logo and copyright information.
*L	5387677	VGT	08/02/2016	Added CYPD2122-24LQXI part number in Ordering Information.

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