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Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

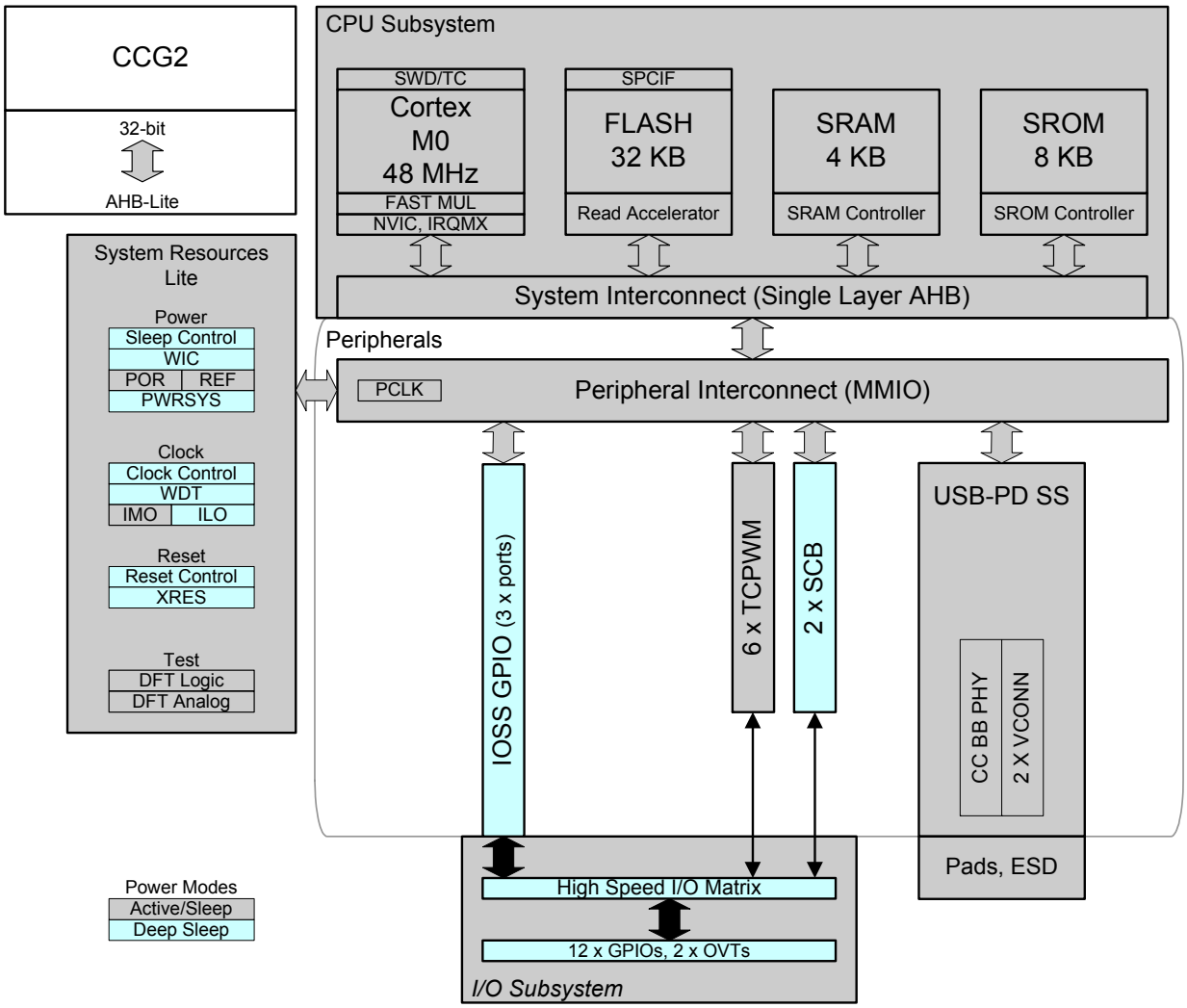
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32KB)
Controller Series	-
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	9
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFBGA, WLCSP
Supplier Device Package	20-WLCSP (1.63x2.03)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd2105-20fnxit

Contents

Figure 1. EZ-PD CCG2 Block Diagram



Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG2 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG2 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

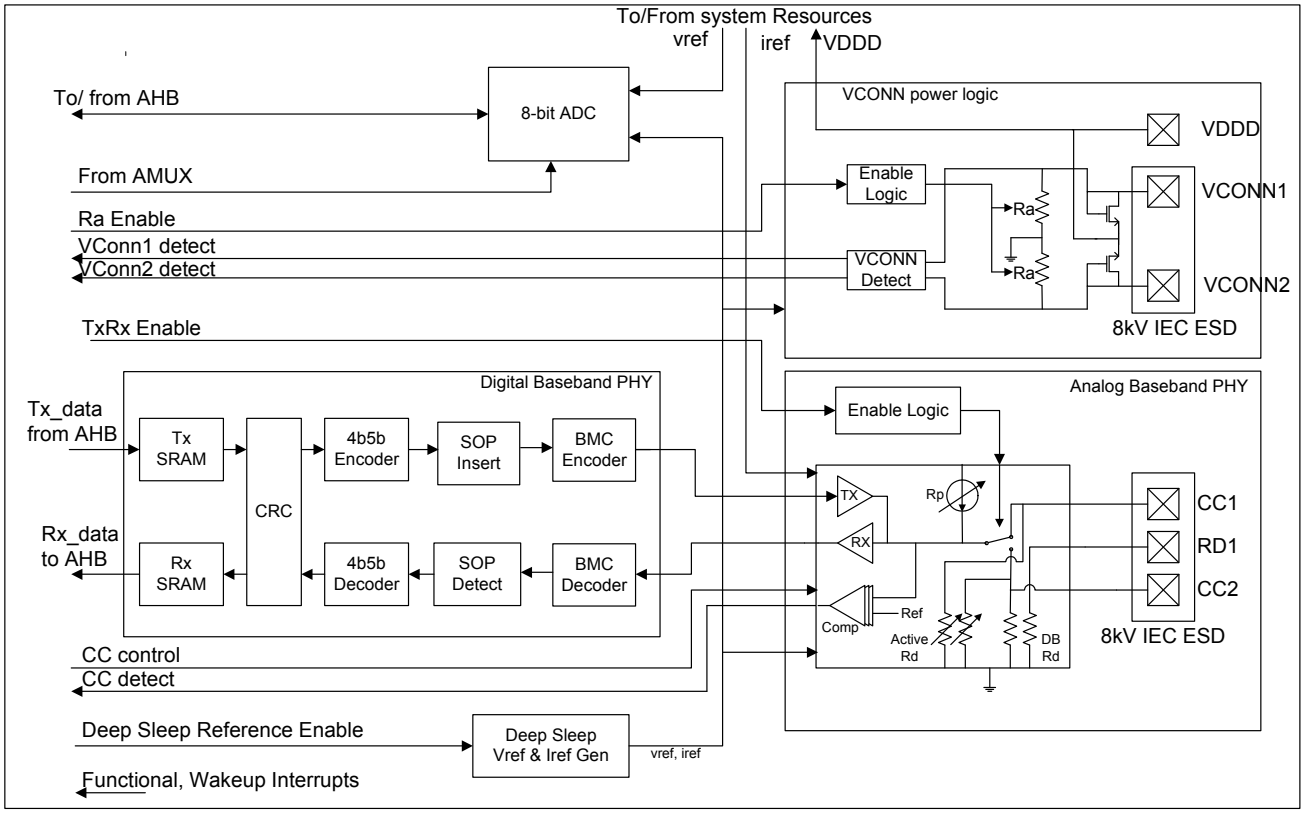
A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

EZ-PD CCG2 has a USB-PD subsystem consisting of a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V front end. This subsystem integrates the required termination resistors to identify the role of the EZ-PD CCG2 solution. R_A is used to identify EZ-PD CCG2 as an accessory or an electronically marked cable. R_D is used to identify EZ-PD CCG2 as a UFP in a hybrid cable or a dongle. When configured as a DFP, integrated current sources perform the role of R_P or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the Type-C spec. EZ-PD CCG2 responds to all USB-PD communication. The EZ-PD CCG2 USB-PD sub-system can be configured to respond to SOP, SOP', or SOP" messaging.

The USB-PD sub-system contains a 8-bit SAR (Successive Approximation Register) ADC for analog to digital conversions. The ADC includes a 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global Analog Multiplex Busses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use. The CC1, CC2 and RD1 pins are not available to connect to the mux busses.

Figure 2. USB-PD Subsystem



System Resources

Power System

The power system is described in detail in the section Power on page 9. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). EZ-PD CCG2 can operate from three different power sources over the range of 2.7 to 5.5 V and has three different power modes, transitions between which are managed by the power system. EZ-PD CCG2 provides Sleep and Deep Sleep low-power modes.

Clock System

The clock system for EZ-PD CCG2 consists of the Internal Main Oscillator (IMO) and the Internal Low-power Oscillator (ILO).

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG2 has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG2 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1 block of EZ-PD CCG2 is not completely compliant with the I^2C spec in the following respects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG2 has six TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG2 has up to 10 GPIOs in addition to the I^2C and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant. The number of available GPIOs vary with the package. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Figure 3. 20-ball WLCSP EZ-PD CCG2 Ball Map (Bottom (Balls Up) View)

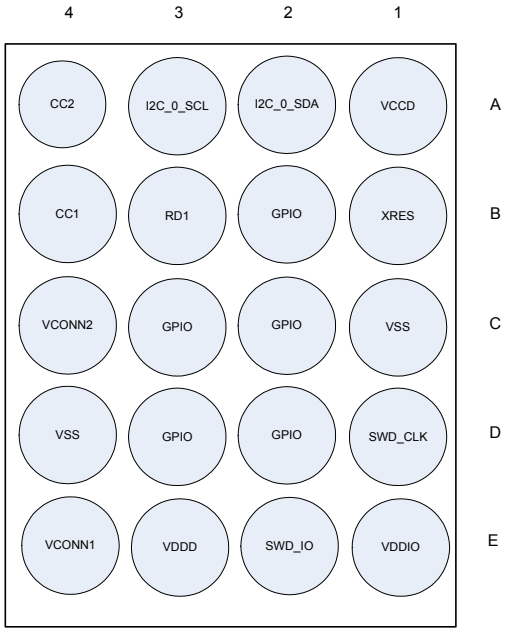


Figure 4. 14-pin DFN Pin Map (Top View)

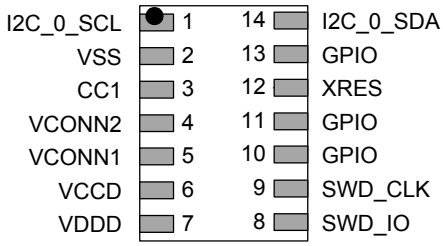
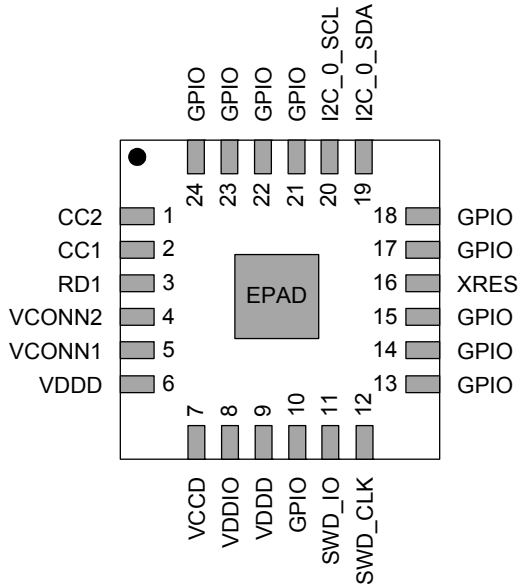


Figure 5. 24-Pin QFN Pin Map (Top View)



Power

The following power system diagram shows the set of power supply pins as implemented in EZ-PD CCG2.

EZ-PD CCG2 can operate from three different power sources. VCONN1 and VCONN2 pins can be used as connections to the VCONN pins on a Type-C plug of a cable or VCONN-powered accessory. Each of these inputs support operation over 4.0 to 5.5 V. An internal isolation between VCONN1 and VCONN2 pins is provided allowing them to be at different levels simultaneously. CCG2 can be used in EMCA applications with only one or both VCONN pins as power sources. This is illustrated later in the section on Applications. Besides being power inputs, each VCONN pin is also internally connected to a R_A termination resistor required for EMCA and VCONN-powered accessories.

EZ-PD CCG2 can also be operate from 2.7 to 5.5 V when operated from the VDDD supply pin. VCONN-powered accessory applications require that CCG2 work down to 2.7 V. In such applications, both the VDDD and VCONN pins should be connected to the VCONN pin of the Type-C plug in the accessory.

In UFP, DFP, and DRP applications, CCG2 can be operated from VDDD as the only supply input. In such applications, the VCONN pins are left open. In DFP applications, the lowest VDDD level that CCG2 can operate is 3.0 V due to the need to support disconnect detection thresholds of up to 2.7 V.

A separate I/O supply pin, VDDIO, allows the GPIOs to operate at levels from 1.71 to 5.5 V. The VDDIO pin can be equal to or less than the voltages connected to the VCONN1, VCONN2, and VDDD pins. The independent VDDIO supply is not available on the 14-DFN package. On this package, the VDDIO rail is internally connected to the VDDD rails.

The VCCD output of EZ-PD CCG2 must be bypassed to ground via an external capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

Bypass capacitors must be used from VDDD and VCONN pins to ground; typical practice for systems in this frequency range is to use a 0.1-µF capacitor. Note that these are simply rules of thumb and that for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of the power supply bypass capacitors is shown in Figure 6.

Figure 6. EZ-PD CCG2 Power and Bypass Scheme Example

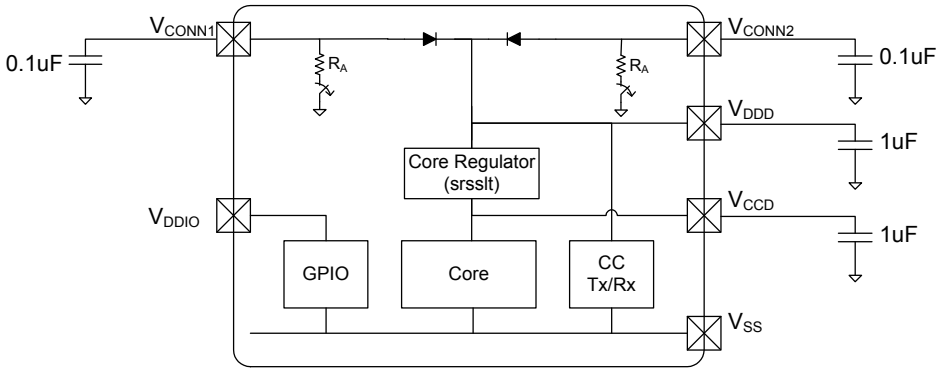


Figure 8. Passive EMCA Application – Single EZ-PD CCG2 Per Plug

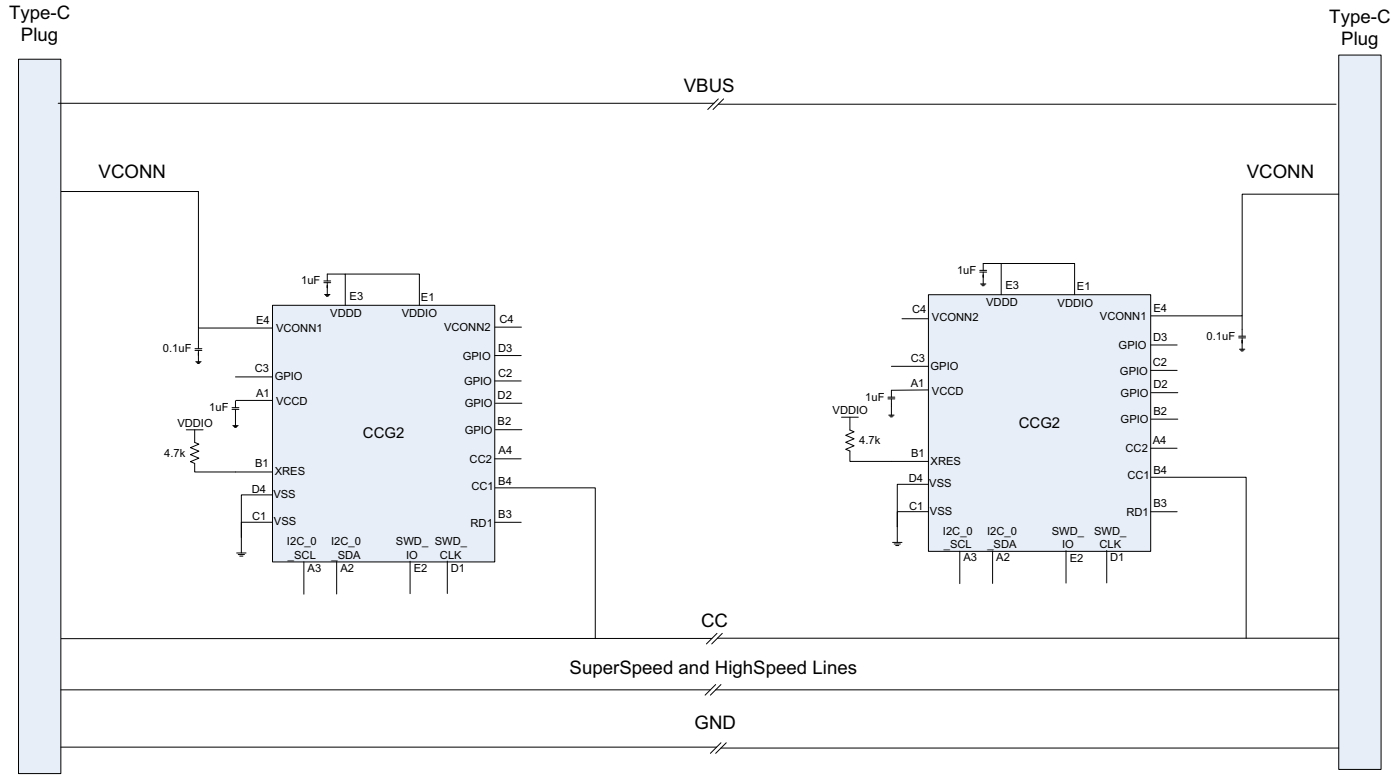


Figure 9 shows a CCG2 device being used in a UFP application (tablet with a Type-C port) only as a power consumer.

The Type-C receptacle brings in HighSpeed and SuperSpeed lines, which are connected directly to the applications processor. The VBUS line from the Type-C receptacle goes directly to the UFP (tablet) charger circuitry. The applications processor communicates over the I^2C signal with the CCG2 device, and the CC1 and CC2 lines from the Type-C receptacle are connected directly to the respective CC1/2 pins of the CCG2 device.

Figure 9. Upstream Facing Port (UFP) Application – Tablet with a Type-C Port

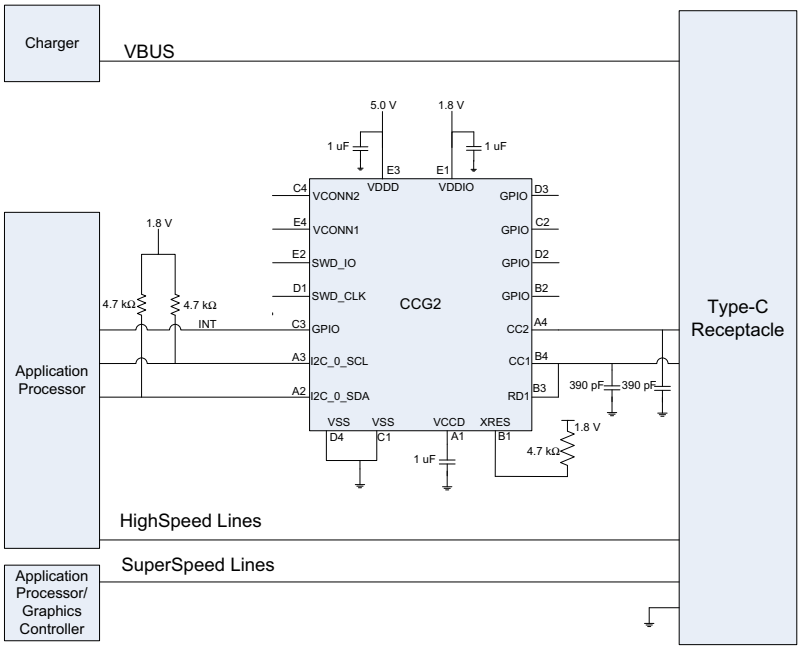


Figure 10 shows a Notebook DRP application diagram using a CCG2 device. The Type-C port can be used as a power provider or a power consumer. The CCG2 device communicates with the Embedded controller (EC) over I^2C. It also controls the Data Mux to route the High Speed signals either to the USB chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode). The SBU lines, SuperSpeed and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

Optional FETs are provided for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. A VBUS_DISCHARGE FET controlled by CCG2 device is used to quickly discharge VBUS after the Type-C connection is detached.

Figure 10. Dual Role Port (DRP) Application

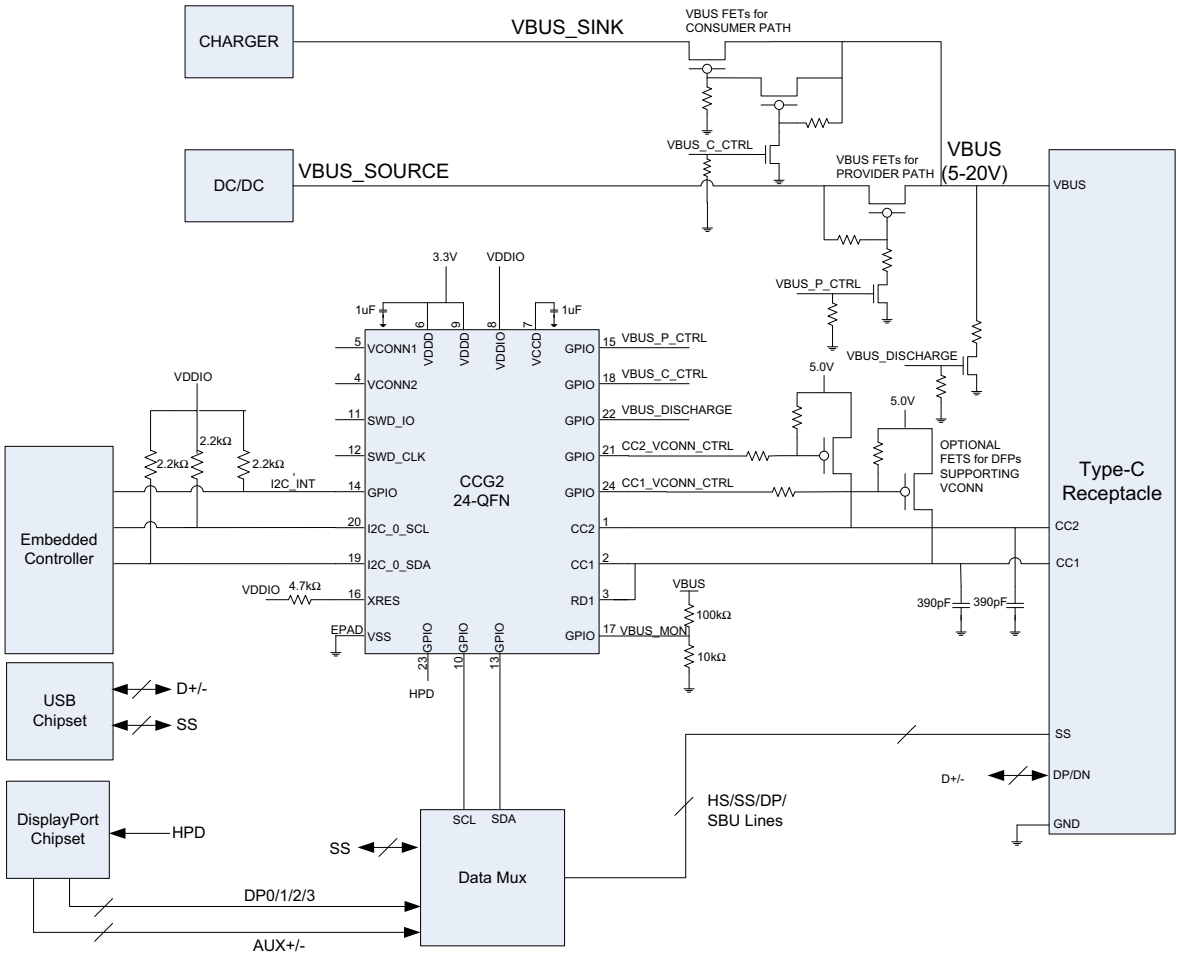
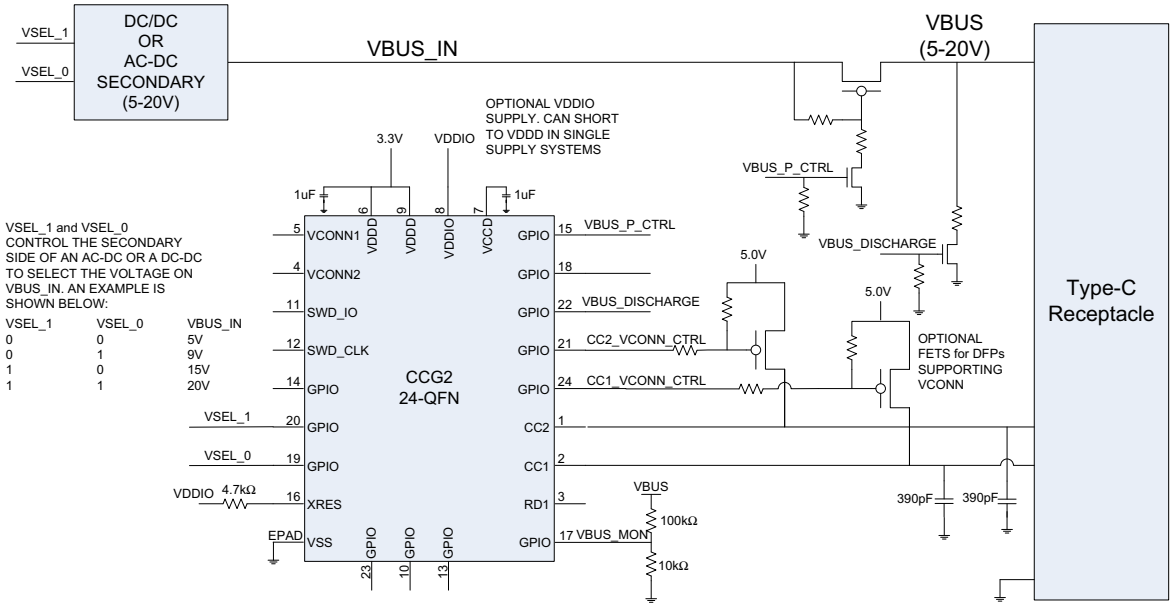


Figure 11 shows a CCG2 receptacle-based Power Adapter application in which the CCG2 device is used as a DFP. CCG2 integrates all termination resistors and uses GPIOs (VSEL_0 and VSEL_1) to indicate the negotiated power profile. The VBUS voltage on the Type-C port is monitored using internal ADC to detect undervoltage and overvoltage conditions on VBUS. To ensure quick discharge of VBUS when the power adapter cable is detached, a discharge path is also provided.

Figure 11. Downstream Facing Port (DFP) Application



Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{CONN1_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{CONN2_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	Absolute max
V_{CC_ABS}	Absolute max voltage for CC1 and CC2 pins	–	–	6	V	Absolute max
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VCONN1, and VCONN2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for pins CC1, CC2, VCONN1, and VCONN2

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 3. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU frequency	DC	–	48	MHz	3.0 V ≤ V_{DDD} ≤ 5.5 V
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	24-MHz IMO. Guaranteed by characterization
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	Guaranteed by characterization
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I2C / CC command”	–	5	25	ms	Guaranteed by characterization

I/O

Table 4. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH}[2]	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	V_{IH}[2]	LVTTL input, V_{DDIO} < 2.7 V	0.7× V_{DDIO}	–	–	V	–
SID.GIO#40	V_{IL}	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	V_{IH}[2]	LVTTL input, V_{DDIO} ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V_{IL}	LVTTL input, V_{DDIO} ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDIO}
SID.GIO#5	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#6	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDIO} = 3.0 V.Guaranteed by characterization
SID.GIO#17	C_{IN}	Input capacitance	–	–	7	pF	Guaranteed by characterization
SID.GIO#43	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DDIO} ≥ 2.7 V. Guaranteed by characterization.
SID.GPIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDIO}	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DDIO}/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	Guaranteed by characterization

Note
2. V_{IH} must not exceed V_{DDIO} + 0.2 V.

System Resources

Power-on-Reset (POR) with Brown Out

Table 17. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization

Table 18. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5	V	Guaranteed by characterization

SWD Interface

Table 19. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\ V \le V_{DDIO} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$1.8\ V \le V_{DDIO} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 20. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 21. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO}$	RMS jitter at 48 MHz	–	145	–	ps	Guaranteed by characterization
F_{IMO}	–	IMO frequency	24	–	48	MHz	–

Internal Low-Speed Oscillator

Table 22. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 23. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	ILO Frequency	20	40	80	kHz	–

Power Down

Table 24. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP Dead Battery CC termination on RD1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0 V and 0.6 V applied at RD1 or CC2
SID.PD.6	R_A	Power cable termination	0.8	1.0	1.2	kΩ	All supplies forced to 0 V and 0.2 V applied at V_{CONN1} or V_{CONN2}
SID.PD.7	Ra_OFF	Power cable termination - Disabled	0.4	0.75	–	MΩ	2.7 V applied at V_{CONN1} or V_{CONN2} with R_A disabled
SID.PD.8	Rleak_1	V_{CONN} leaker for 0.1-µF load	–	–	216	kΩ	Managed Active Cable (MAC) discharge
SID.PD.9	Rleak_2	V_{CONN} leaker for 0.5-µF load	–	–	41.2	kΩ	
SID.PD.10	Rleak_3	V_{CONN} leaker for 1.0-µF load	–	–	19.6	kΩ	
SID.PD.11	Rleak_4	V_{CONN} leaker for 2.0-µF load	–	–	9.8	kΩ	
SID.PD.12	Rleak_5	V_{CONN} leaker for 5.0-µF load	–	–	4.1	kΩ	
SID.PD.13	Rleak_6	V_{CONN} leaker for 10-µF load	–	–	2.0	kΩ	
SID.PD.14	Ileak	Leaker on V_{CONN1} and V_{CONN2} for discharge upon cable detach	150	–	–	µA	–

Analog-to-Digital Converter

Table 25. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	bits	Guaranteed by characterization
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	Guaranteed by characterization
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Guaranteed by characterization
SID.ADC.4	Gain Error	Gain error	–1	–	1	LSB	Guaranteed by characterization

Table 26. ADC AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	Guaranteed by characterization

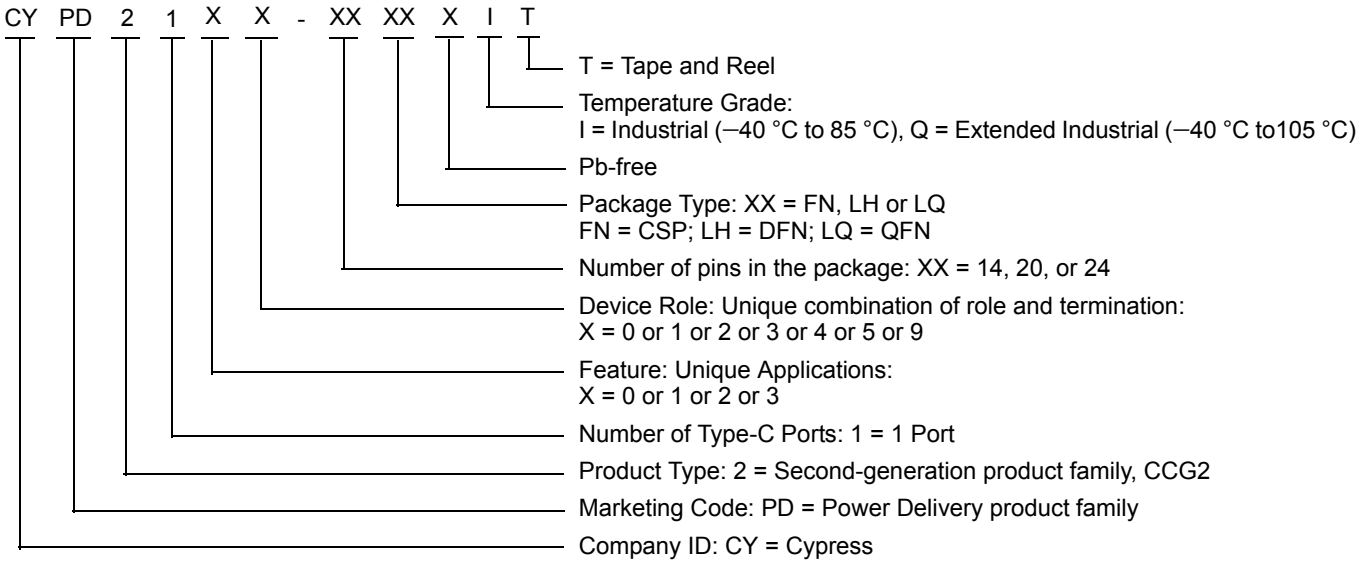
Ordering Information

The EZ-PD CCG2 part numbers and features are listed in Table 27.

Table 27. EZ-PD CCG2 Ordering Information

Part Number	Application	Type-C Ports	Termination Resistor	Role	Package
CYPD2103-20FNXIT	Cable	1	R_A[4]	Cable	20-ball CSP
CYPD2103-14LHXIT	Cable	1	R_A[4]	Cable	14-pin DFN
CYPD2104-20FNXIT	Accessory	1	R_D[5]	Accessory	20-ball CSP
CYPD2105-20FNXIT	Active Cable	1	R_A[4]	Active Cable	20-ball CSP
CYPD2119-24LQXIT	C-DP	1	R_D[5]	UFP	24-pin QFN
CYPD2120-24LQXIT	C-HDMI	1	R_D[5]	UFP	24-pin QFN
CYPD2121-24LQXIT	Dock/Monitor Upstream port	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2122-20FNXIT	Tablet	1	R_P[6], R_D[5]	DRP	20-ball CSP
CYPD2122-24LQXI	Notebook	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2122-24LQXIT	Notebook	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2125-24LQXIT	Dock/Monitor Downstream port	1	R_P[6]	DFP	24-pin QFN
CYPD2134-24LQXIT	DFP	1	R_P[6]	DFP	24-pin QFN
CYPD2134-24LQXQT	DFP	1	R_P[6]	DFP	24-pin QFN

Ordering Code Definitions



Notes
4. Termination resistor denoting an EMCA.
5. Termination resistor denoting an accessory or upstream facing port.
6. Termination resistor denoting a downstream facing port.

Packaging

Table 28. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended Industrial			105	°C
T_J	Operating junction temperature	Industrial	–40	–	100	°C
		Extended Industrial			125	°C
T_{JA}	Package θ_{JA} (20-ball WLCSP)	–	–	66	–	°C/W
T_{JC}	Package θ_{JC} (20-ball WLCSP)	–	–	0.7	–	°C/W
T_{JA}	Package θ_{JA} (14-pin DFN)	–	–	31	–	°C/W
T_{JC}	Package θ_{JC} (14-pin DFN)	–	–	59	–	°C/W
T_{JA}	Package θ_{JA} (24-pin QFN)	–	–	22	–	°C/W
T_{JC}	Package θ_{JC} (24-pin QFN)	–	–	29	–	°C/W

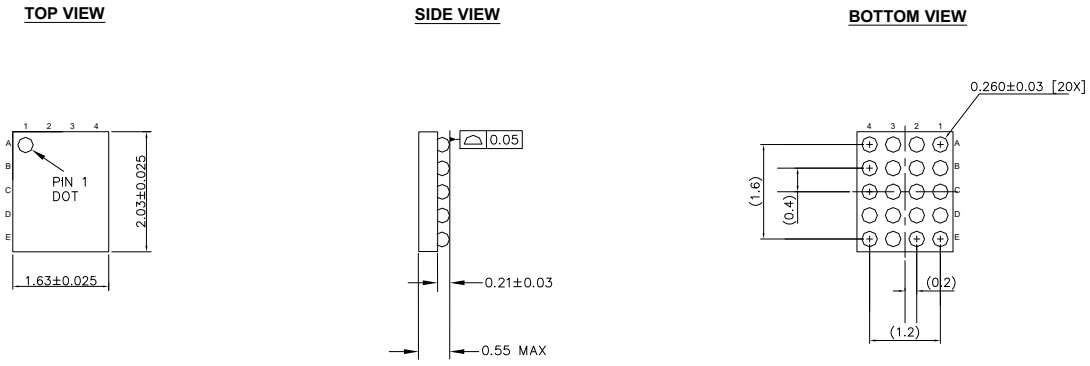
Table 29. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
20-ball WLCSP	260 °C	30 seconds
14-pin DFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds

Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
20-ball WLCSP	MSL 1
14-pin DFN	MSL 3
24-pin QFN	MSL 3

Figure 15. 20-ball WLCSP (1.63 × 2.03 × 0.55 mm) FN20B Package Outline, 001-95010



NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18

2. ALL DIMENSIONS ARE IN MILLIMETERS

001-95010 *A

Figure 16. 14-pin DFN (2.5 × 3.5 × 0.6 mm), LH14A, 0.95 × 3.00 E-Pad (Sawn) Package Outline, 001-96312

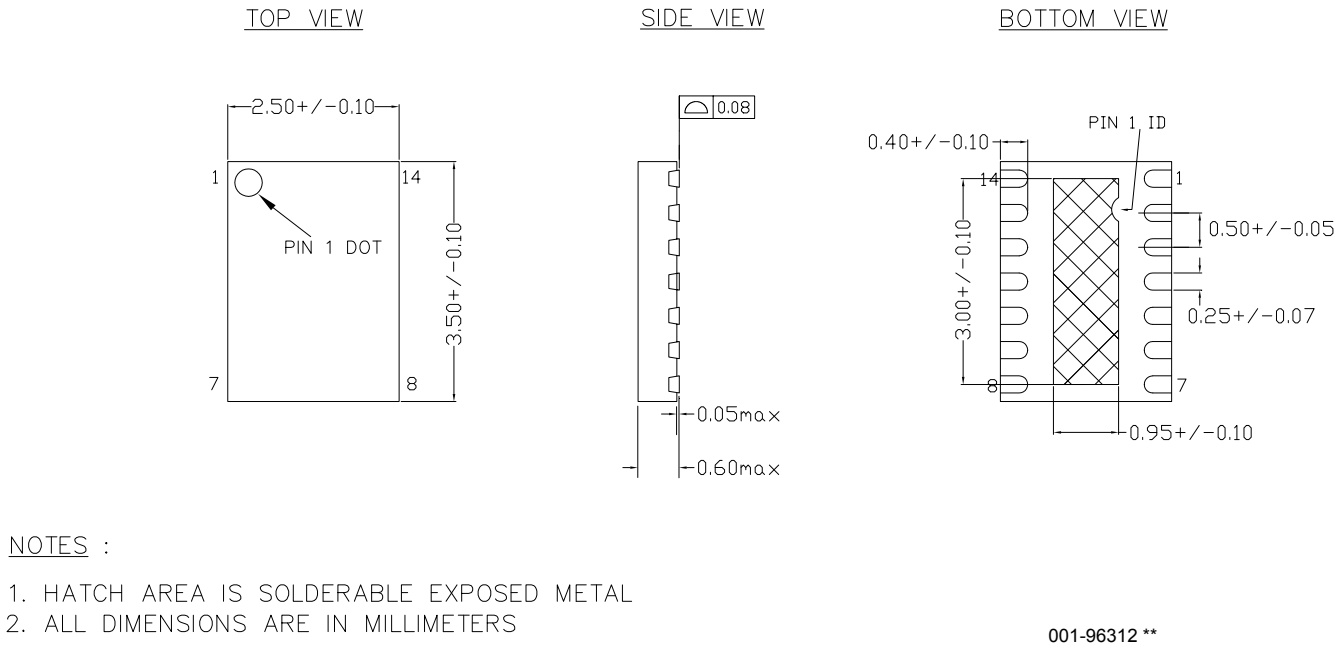
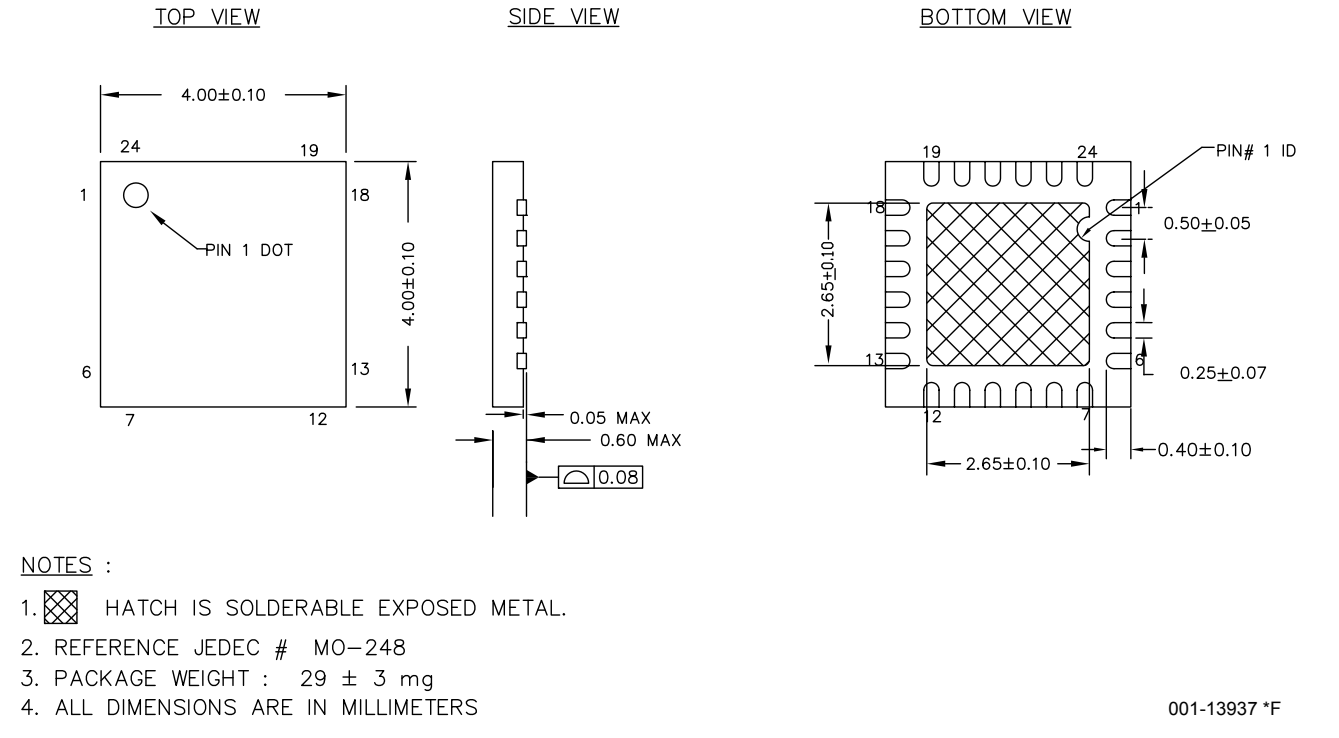


Figure 17. 24-Pin QFN (4 × 4 × 0.55 mm), LQ24A, 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937



Acronyms

Table 31. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG2	Cable Controller Generation 2
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
XRES	external reset I/O pin

References and Links To Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG3: USB Type-C Controller Datasheet
- CCG4: Two-Port USB Type-C Controller Datasheet

Document History Page

Description Title: EZ-PD™ CCG2 Datasheet USB Type-C Port Controller Document Number: 001-93912				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	4680071	GAYA	03/07/2015	Release to web
*F	4718374	AKN	04/09/2015	Added 24-pin QFN pin and package information. Added DRP and DFP Application diagrams
*G	4774142	AKN	06/15/2015	Changed datasheet status from Preliminary to Final. Updated Logic Block Diagram. Changed number of GPIOs to 10 and added a note about the number of GPIOs varying depending on the package. Updated Power and Digital Peripherals section. Updated Application diagrams. Added SID.PWR#1_A parameter. Added CYPD2122-20FNXIT part in Ordering Information. Removed Errata.
*H	4979175	VGT	10/23/2015	Updated Figure 1 and Figure 5. Added VCC_ABS spec and updated the SID.ADC.4 parameter. Added “Guaranteed by characterization” note for the following specs: SID.GIO#16, SID.GIO#17, SID.XRES#3, SID 160 to SID 172A, SID 2226, SID 229, SID.ADC.1 to SID.ADC.5.
*I	5028128	VGT	12/04/2015	Updated Application Diagrams: Added Figure 12. Added Figure 13. Added Figure 14. Updated Ordering Information. Added part numbers CYPD2119-24LQXIT, CYPD2120-24LQXIT, CYPD2121-24LQXIT, CYPD2125-24LQXIT.
*J	5186972	VGT	03/28/2016	Updated temperature ranges in Features. Updated Table 28. Updated Ordering Information.
*K	5303957	VGT	06/13/2016	Added Available Firmware and Software Tools. Updated Figure 8: Per the USB PD3.0 spec, SOP” implementation is no longer valid for passive cables. Updated Figure 9, Figure 10, and Figure 11. Added descriptive notes for the application diagrams. Added References and Links To Applications Collaterals. Updated Ordering Information. Updated Cypress logo and copyright information.
*L	5387677	VGT	08/02/2016	Added CYPD2122-24LQXI part number in Ordering Information.