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Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (32KB)
Controller Series	-
RAM Size	4K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	9
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFBGA, WLCSP
Supplier Device Package	20-WLCSP (1.63x2.03)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd2122-20fnxit

Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

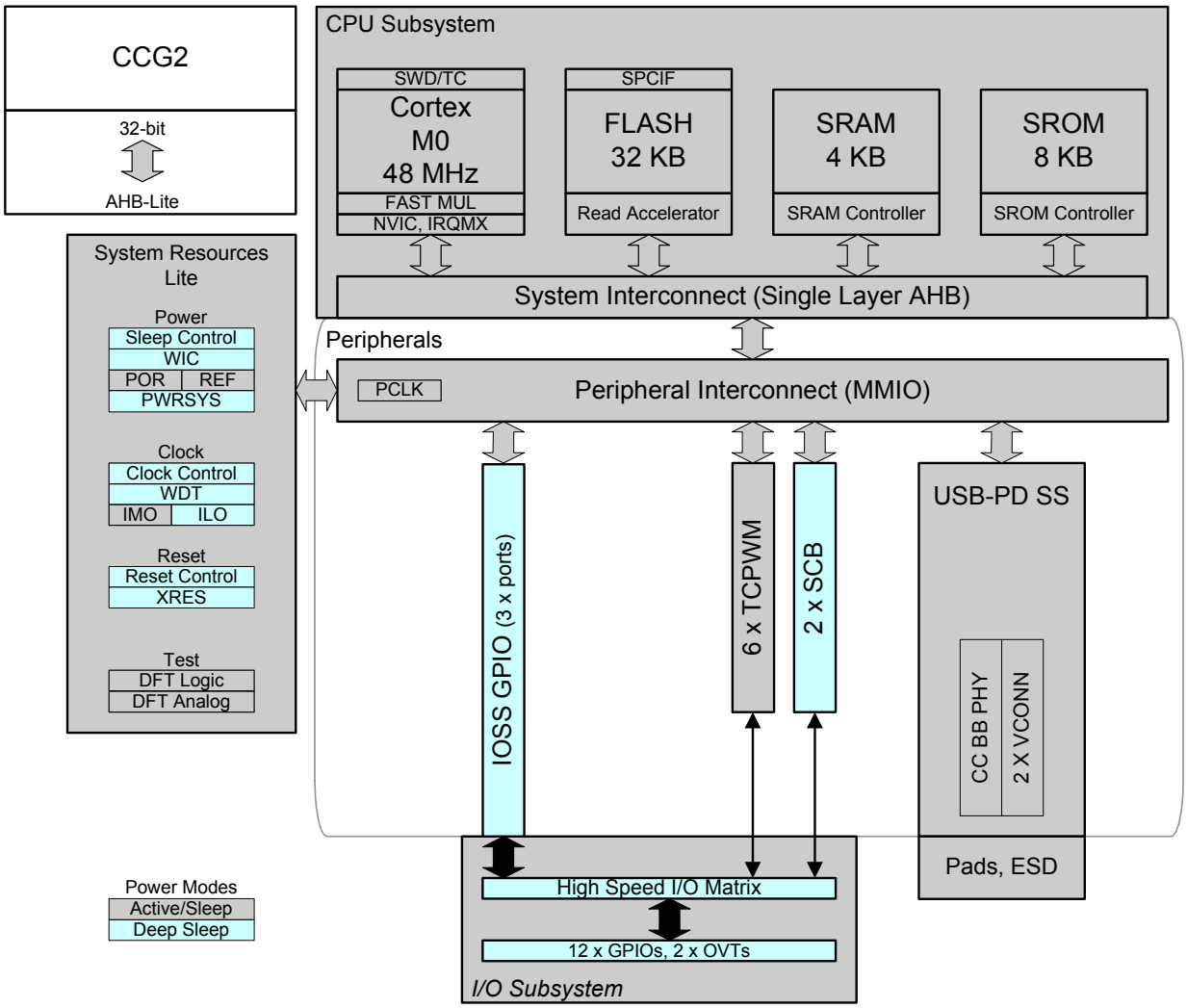
You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility

Contents

Functional Overview **4**
CPU and Memory Subsystem 4
USB-PD Subsystem (SS) 5
System Resources 5
Peripherals 6
GPIO 6
Pinouts **7**
Power **9**
Application Diagrams **10**
Electrical Specifications **17**
Absolute Maximum Ratings 17
Device Level Specifications 18
Digital Peripherals 20
Memory 22
System Resources 23
Ordering Information **26**
Ordering Code Definitions 26
Packaging **27**
Acronyms **29**
Document Conventions **30**
Units of Measure 30
References and Links To Applications Collaterals 31
Document History Page **32**
Sales, Solutions, and Legal Information **33**
Worldwide Sales and Design Support 33
Products 33
PSoC® Solutions 33
Cypress Developer Community 33
Technical Support 33

Figure 1. EZ-PD CCG2 Block Diagram



Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG2 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG2 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG2 has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG2 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1 block of EZ-PD CCG2 is not completely compliant with the I^2C spec in the following respects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG2 has six TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG2 has up to 10 GPIOs in addition to the I^2C and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant. The number of available GPIOs vary with the package. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

Group	Name	Pin Map 24-QFN	Ball Location 20-CSP	Pin Map 14-DFN	Description
USB Type-C Port	CC1	2	B4	3	USB PD connector detect/Configuration Channel 1
	CC2	1	A4	N/A	USB PD connector detect/Configuration Channel 2
	RD1	3	B3	N/A	Dedicated Rd resistor pin for CC1 Must be left open for cable applications and connected together with CC1 ball for UFP or DFP with dead battery applications
GPIOs and serial interfaces	GPIO	22	C3	N/A	GPIO / SPI_0_CLK / UART_0_ RX
	GPIO	18	D3	13	GPIO / SPI_0_MOSI / UART_0_TX
	GPIO	13	C2	10	GPIO / I2C_1_SDA / SPI_1_MISO / UART_1_RX
	GPIO	10	D2	N/A	GPIO / I2C_1_SCL / SPI_1_CLK / UART_1_TX
	GPIO	15	B2	11	GPIO / SPI_1_SEL / UART_1_RTS
	GPIO	14	N/A	N/A	GPIO
	GPIO	17	N/A	N/A	GPIO
	GPIO	21	N/A	N/A	GPIO
	GPIO	23	N/A	N/A	GPIO
	GPIO	24	N/A	N/A	GPIO
	I2C_0_SCL	20	A3	1	GPIO / I2C_0_SCL / SPI_0_MISO / UART_0_RTS
	I2C_0_SDA	19	A2	14	GPIO / I2C_0_SDA / SPI_0_SEL / UART_0_CTS
	SWD _IO	11	E2	8	SWD IO / GPIO / UART_1_CTS / SPI_1_MOSI
	SWD_CLK	12	D1	9	SWD clock / GPIO
RESET	XRES	16	B1	12	Reset input
POWER	VCONN1	5	E4	5	VCONN 1 input (4.0 V to 5.5 V)
	VCONN2	4	C4	4	VCONN 2 input (4.0 V to 5.5 V)
	VDDIO	8	E1	N/A	1.71-V to 5.5-V supply for I/Os
	VCCD	7	A1	6	1.8-V regulator output for filter capacitor
	VDDD	9	E3	7	VDDD supply input/output (2.7 V to 5.5 V)
	VDDD	6			VDDD supply input/output (2.7 V to 5.5 V)
	VSS	EPAD	N/A	EPAD	Ground supply
	VSS		D4	2	Ground supply
	VSS		C1		Ground supply

Figure 3. 20-ball WLCSP EZ-PD CCG2 Ball Map (Bottom (Balls Up) View)

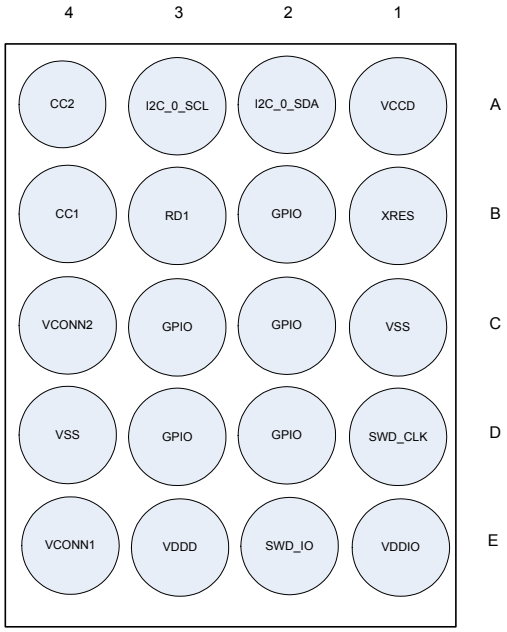


Figure 4. 14-pin DFN Pin Map (Top View)

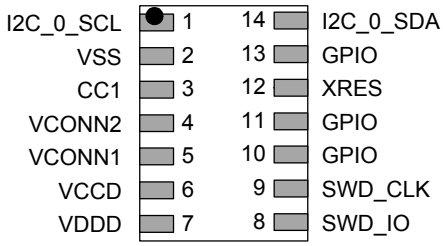


Figure 5. 24-Pin QFN Pin Map (Top View)

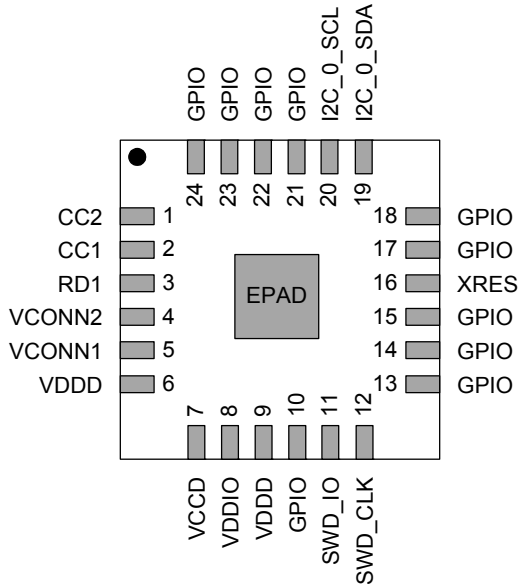


Figure 10 shows a Notebook DRP application diagram using a CCG2 device. The Type-C port can be used as a power provider or a power consumer. The CCG2 device communicates with the Embedded controller (EC) over I^2C. It also controls the Data Mux to route the High Speed signals either to the USB chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode). The SBU lines, SuperSpeed and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

Optional FETs are provided for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. A VBUS_DISCHARGE FET controlled by CCG2 device is used to quickly discharge VBUS after the Type-C connection is detached.

Figure 10. Dual Role Port (DRP) Application

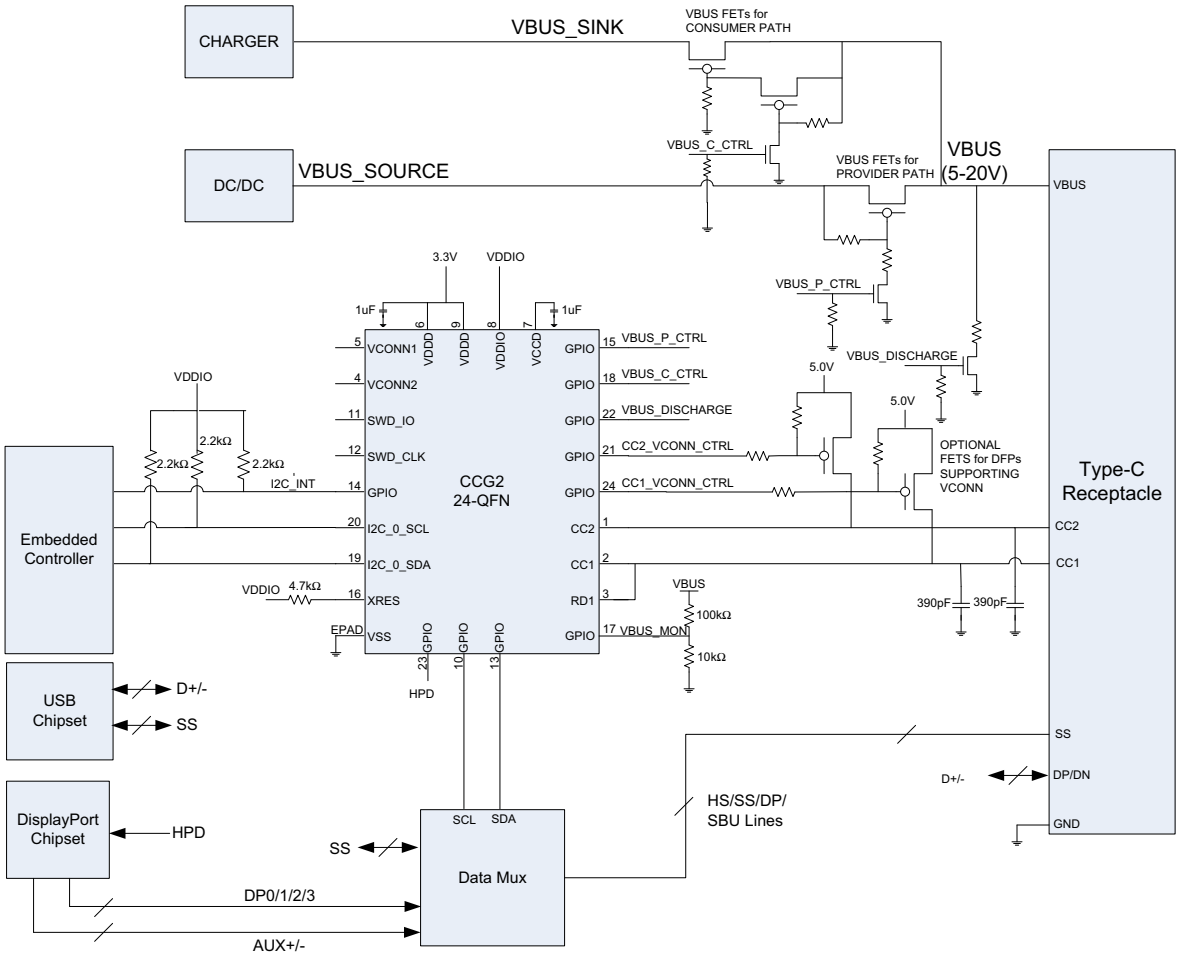


Figure 12 shows a USB Type-C to HDMI/DVI/VGA adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has HDMI/DVI/VGA interface. It enables users of any Notebook that implements USB-Type C to connect to other display types.

This application has a Type-C plug on one end and the legacy video (HDMI/DVI/VGA) receptacle on the other end. This application meets the requirements described in Section 4.3 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0. This application supports display output at a resolution of up to 4K Ultra HD (3840x2160) at 60 Hz. It also supports the USB Billboard Device Class, which is required by the USB PD specification for enumeration of any accessories that support Alternate Mode when connected to a host PC.

Figure 12. USB Type-C to HDMI/DVI/VGA Dongle Application Diagram

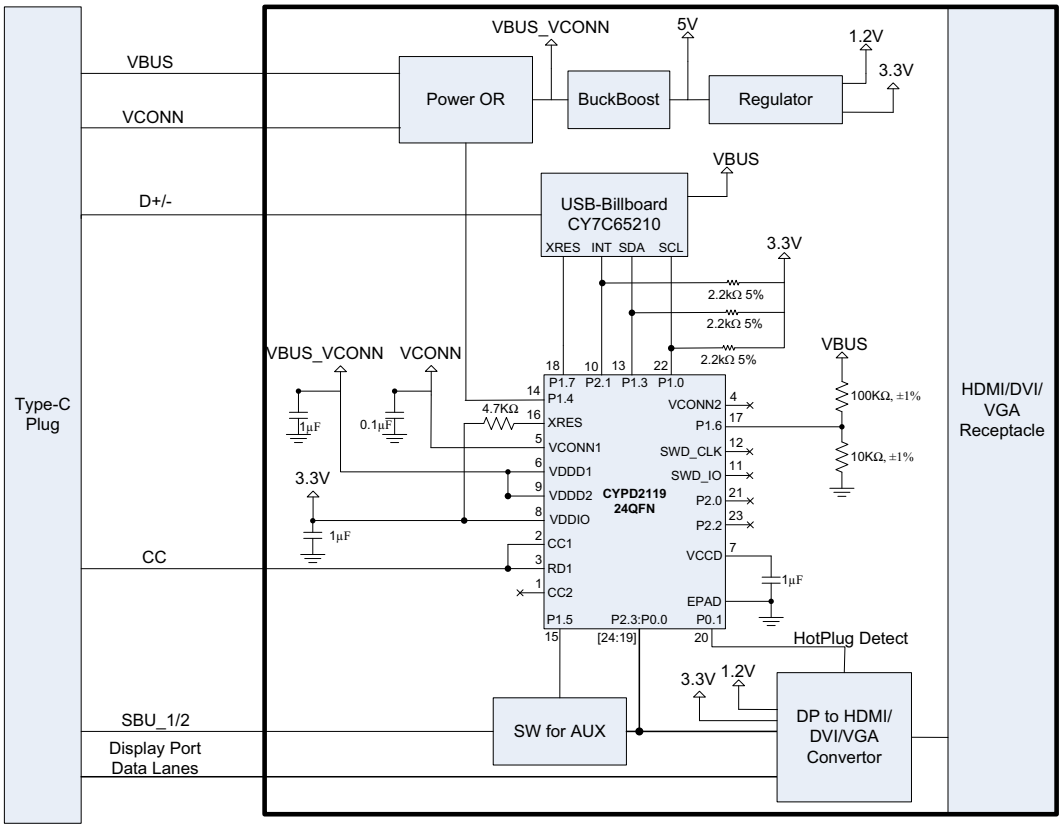
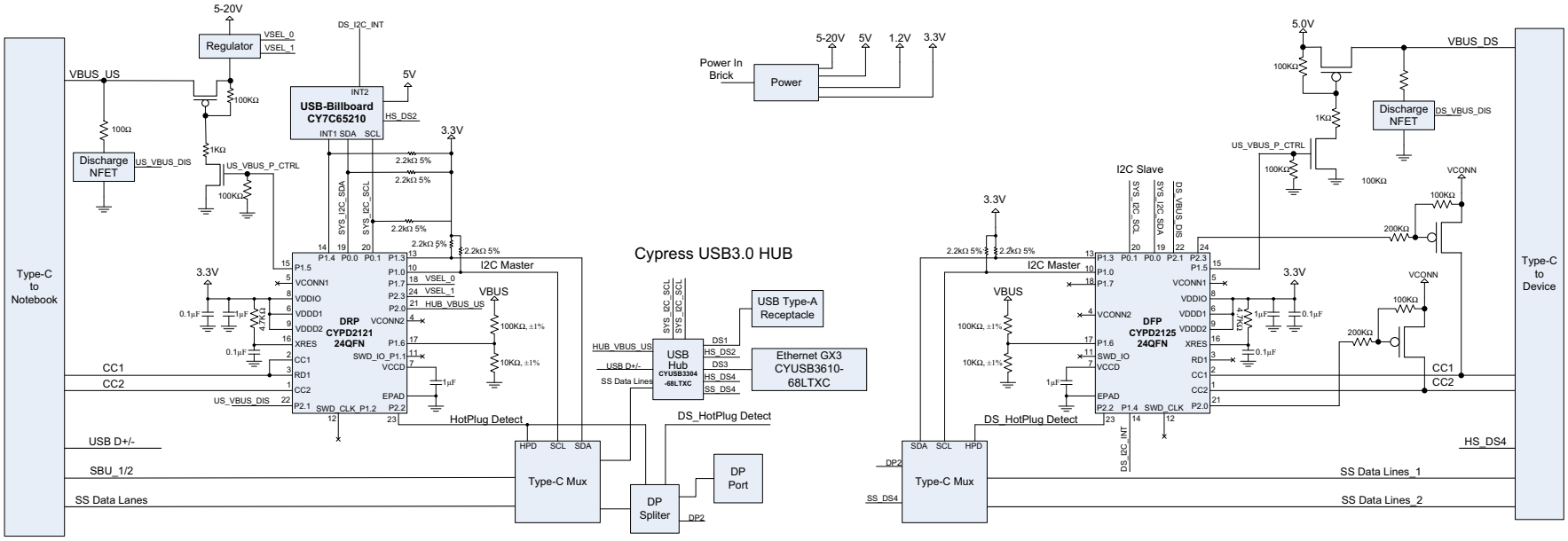


Figure 14 shows a CCG2 Monitor/Dock application diagram. It enables connectivity between a USB Type-C host system on the Upstream port and multiple Display/Data devices on the Downstream port. This application has a USB Type-C receptacle on the Upstream port, which supports data, power, and display. On the Downstream port, this application supports: USB Type-A, Gigabit Ethernet, DisplayPort, and USB Type-C receptacle.

The main features of this solution are:

- Powered from an external 24-V DC power adapter
- Provides up to 45 W (15 V at 3A) on the Upstream Type-C port and up to 15 W (5 V at 3A) on the Downstream USB Type-C port
- Provides simultaneous 4K display output with USB 3.1 Gen 1 on the USB Type-A port
- Four-lane display on the DisplayPort connector
- Multi-Stream support on DisplayPort and Downstream Type-C port
- USB 3.1 Gen 1 hub for USB port expansion
- Gigabit Ethernet using RJ45 connector
- Supports firmware upgrade of CCG2 controllers, HX3 Hub controller, and Billboard controller

Figure 14. CCG2 in Dock/Monitor Application Diagram



CCG2 connected on the Upstream Port

CCG2 connected on the Downstream Port

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{CONN1_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{CONN2_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	Absolute max
V_{CC_ABS}	Absolute max voltage for CC1 and CC2 pins	–	–	6	V	Absolute max
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VCONN1, and VCONN2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for pins CC1, CC2, VCONN1, and VCONN2

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	UFP Applications
SID.PWR#1_A	V_{DDD}	Power supply input voltage	3.0	–	5.5	V	DFP/DRP Applications
SID.PWR#23	V_{CONN1}	Power supply input voltage	4.0	–	5.5	V	–
SID.PWR#23_A	V_{CONN2}	Power supply input voltage	4.0	–	5.5	V	–
SID.PWR#13	V_{DDIO}	GPIO power supply	1.71	–	5.5	V	–
SID.PWR#24	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID.PWR#15	C_{EFC}	External regulator voltage bypass on V_{CCD}	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor on V_{DDD}	–	1	–	µF	X5R ceramic or better
SID.PWR#25		Power Supply Decoupling Capacitor on V_{CONN1} and V_{CONN2}	–	0.1	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 2.7 to 5.5 V. Typical values measured at V_{DD} = 3.3 V.							
SID.PWR#12	I_{DD12}	Supply current	–	7.5	–	mA	V_{CONN1} or V_{CONN2} = 5 V, T_A = 25 °C, CC I/O IN Transmit or Receive, R_A disconnected, no I/O sourcing current, CPU at 12 MHz
Sleep Mode, V_{DDD} = 2.7 to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup. WDT ON. IMO at 48 MHz	–	2.0	3.0	mA	V_{DDD} = 3.3 V, T_A = 25 °C, all blocks except CPU are ON, CC I/O ON, no I/O sourcing current
Deep Sleep Mode, V_{DDD} = 2.7 to 3.6 V (Regulator on)							
SID_DS_RA	$I_{DD\_DS\_RA}$	V_{CONN1} = 5.0, R_A termination disabled	–	100	–	µA	V_{CONN1}, V_{CONN2} = 5 V, T_A = 25 °C. R_A termination disabled on V_{CONN1} and V_{CONN2}, see SID.PD.7. VCONN leaker circuits turned off during deep sleep
SID34	I_{DD29}	V_{DDD} = 2.7 to 3.6 V. I^2C wakeup and WDT ON	–	50	–	µA	R_A switch disabled on V_{CONN1} and V_{CONN2}. V_{DDD} = 3.3 V, T_A = 25 °C
SID_DS	I_{DD_DS}	V_{DDD} = 2.7 to 3.6 V. CC wakeup ON	–	2.5	–	µA	Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P disabled
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	1	10	µA	–

Table 5. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF
SID71	T_{FALLF}	Fall time	2	–	12	ns	3.3-V V_{DDIO}, Cload = 25 pF

XRES

Table 6. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	–	0.05 × V_{DDIO}	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 7. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	Fc	–	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	–	2/Fc	–	ns	For all Trigger Events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	–	2/Fc	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	–	1/Fc	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	–	1/Fc	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	–	1/Fc	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 8. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kbps	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kbps	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 9. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 10. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	125	µA	Guaranteed by characterization
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	Guaranteed by characterization

Table 11. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	Guaranteed by characterization

Table 12. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	Guaranteed by characterization
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	Guaranteed by characterization
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	Guaranteed by characterization

Table 13. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	Guaranteed by characterization

Internal Low-Speed Oscillator

Table 22. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 23. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	ILO Frequency	20	40	80	kHz	–

Power Down

Table 24. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP Dead Battery CC termination on RD1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0 V and 0.6 V applied at RD1 or CC2
SID.PD.6	R_A	Power cable termination	0.8	1.0	1.2	kΩ	All supplies forced to 0 V and 0.2 V applied at V_{CONN1} or V_{CONN2}
SID.PD.7	Ra_OFF	Power cable termination - Disabled	0.4	0.75	–	MΩ	2.7 V applied at V_{CONN1} or V_{CONN2} with R_A disabled
SID.PD.8	Rleak_1	V_{CONN} leaker for 0.1-µF load	–	–	216	kΩ	Managed Active Cable (MAC) discharge
SID.PD.9	Rleak_2	V_{CONN} leaker for 0.5-µF load	–	–	41.2	kΩ	
SID.PD.10	Rleak_3	V_{CONN} leaker for 1.0-µF load	–	–	19.6	kΩ	
SID.PD.11	Rleak_4	V_{CONN} leaker for 2.0-µF load	–	–	9.8	kΩ	
SID.PD.12	Rleak_5	V_{CONN} leaker for 5.0-µF load	–	–	4.1	kΩ	
SID.PD.13	Rleak_6	V_{CONN} leaker for 10-µF load	–	–	2.0	kΩ	
SID.PD.14	Ileak	Leaker on V_{CONN1} and V_{CONN2} for discharge upon cable detach	150	–	–	µA	–

Analog-to-Digital Converter

Table 25. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	bits	Guaranteed by characterization
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	Guaranteed by characterization
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Guaranteed by characterization
SID.ADC.4	Gain Error	Gain error	–1	–	1	LSB	Guaranteed by characterization

Table 26. ADC AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	Guaranteed by characterization

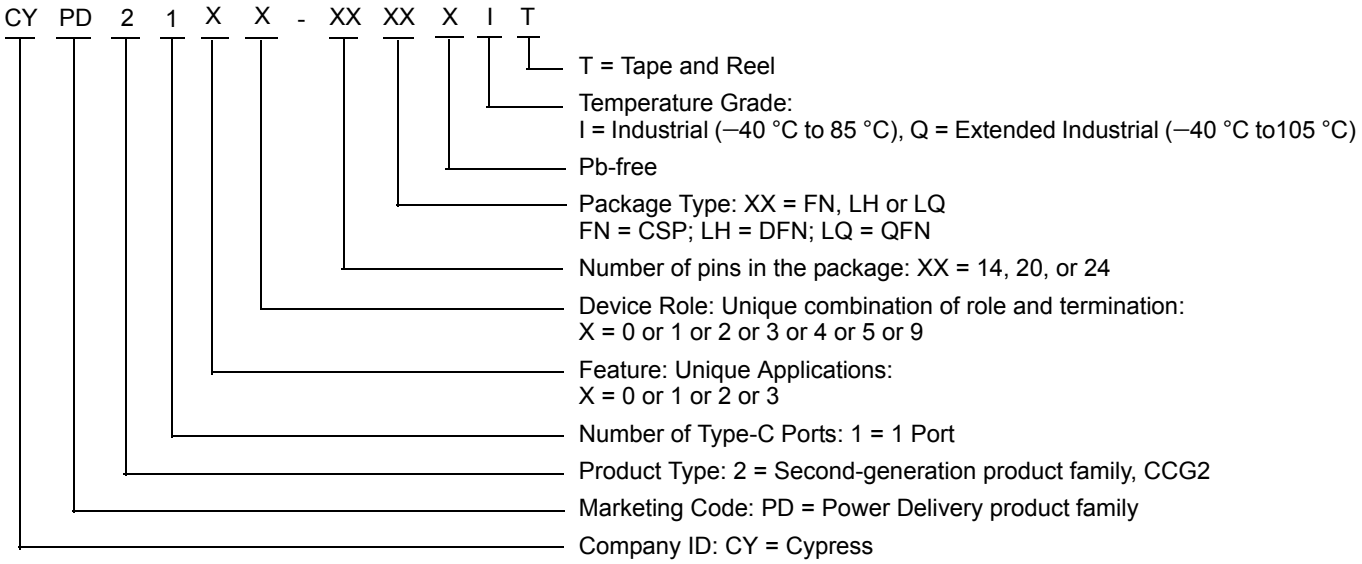
Ordering Information

The EZ-PD CCG2 part numbers and features are listed in Table 27.

Table 27. EZ-PD CCG2 Ordering Information

Part Number	Application	Type-C Ports	Termination Resistor	Role	Package
CYPD2103-20FNXIT	Cable	1	R_A[4]	Cable	20-ball CSP
CYPD2103-14LHXIT	Cable	1	R_A[4]	Cable	14-pin DFN
CYPD2104-20FNXIT	Accessory	1	R_D[5]	Accessory	20-ball CSP
CYPD2105-20FNXIT	Active Cable	1	R_A[4]	Active Cable	20-ball CSP
CYPD2119-24LQXIT	C-DP	1	R_D[5]	UFP	24-pin QFN
CYPD2120-24LQXIT	C-HDMI	1	R_D[5]	UFP	24-pin QFN
CYPD2121-24LQXIT	Dock/Monitor Upstream port	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2122-20FNXIT	Tablet	1	R_P[6], R_D[5]	DRP	20-ball CSP
CYPD2122-24LQXI	Notebook	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2122-24LQXIT	Notebook	1	R_P[6], R_D[5]	DRP	24-pin QFN
CYPD2125-24LQXIT	Dock/Monitor Downstream port	1	R_P[6]	DFP	24-pin QFN
CYPD2134-24LQXIT	DFP	1	R_P[6]	DFP	24-pin QFN
CYPD2134-24LQXQT	DFP	1	R_P[6]	DFP	24-pin QFN

Ordering Code Definitions



Notes
4. Termination resistor denoting an EMCA.
5. Termination resistor denoting an accessory or upstream facing port.
6. Termination resistor denoting a downstream facing port.

Figure 16. 14-pin DFN (2.5 × 3.5 × 0.6 mm), LH14A, 0.95 × 3.00 E-Pad (Sawn) Package Outline, 001-96312

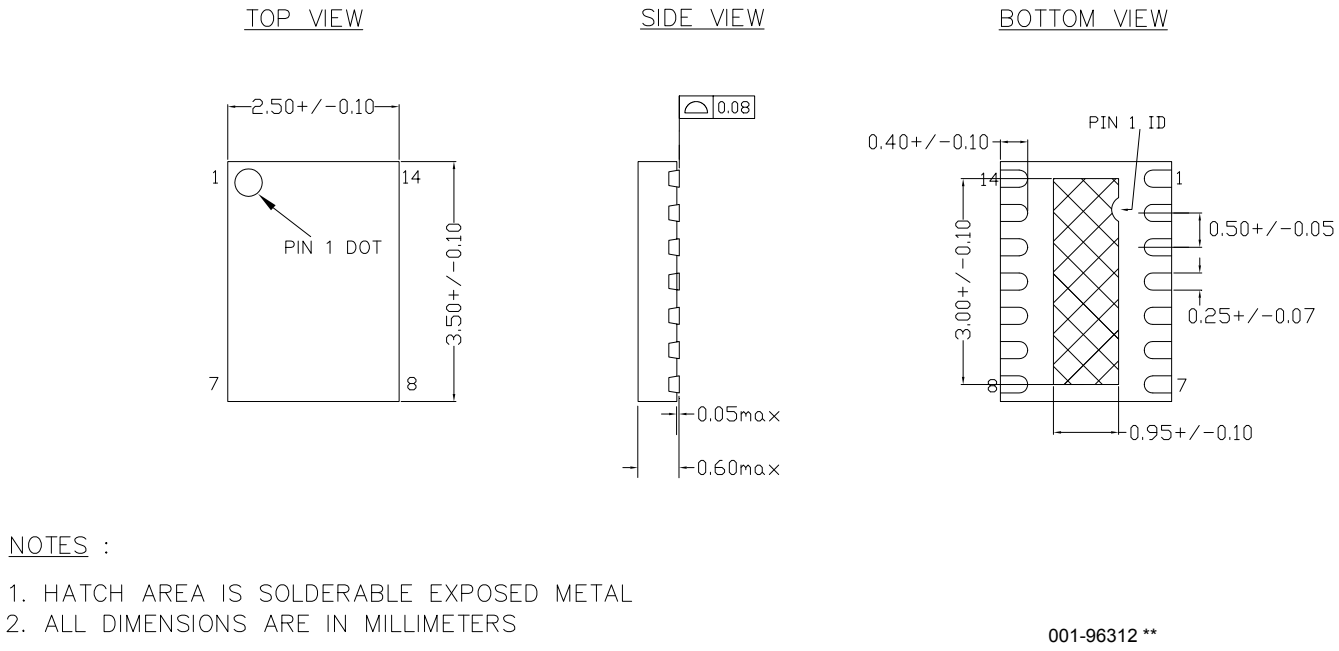
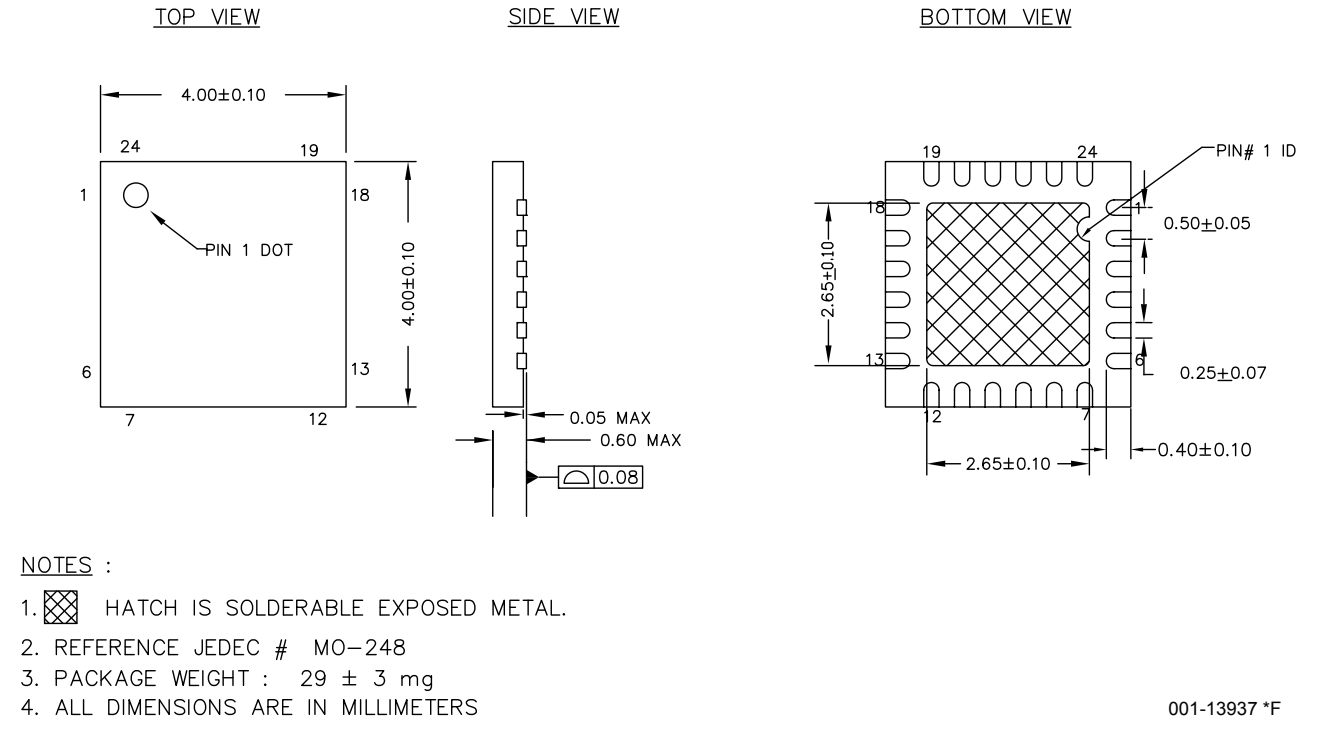


Figure 17. 24-Pin QFN (4 × 4 × 0.55 mm), LQ24A, 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937



Acronyms

Table 31. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG2	Cable Controller Generation 2
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt

Table 31. Acronyms Used in this Document *(continued)*

Acronym	Description
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
XRES	external reset I/O pin

Document History Page

Description Title: EZ-PD™ CCG2 Datasheet USB Type-C Port Controller Document Number: 001-93912				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	4680071	GAYA	03/07/2015	Release to web
*F	4718374	AKN	04/09/2015	Added 24-pin QFN pin and package information. Added DRP and DFP Application diagrams
*G	4774142	AKN	06/15/2015	Changed datasheet status from Preliminary to Final. Updated Logic Block Diagram. Changed number of GPIOs to 10 and added a note about the number of GPIOs varying depending on the package. Updated Power and Digital Peripherals section. Updated Application diagrams. Added SID.PWR#1_A parameter. Added CYPD2122-20FNXIT part in Ordering Information. Removed Errata.
*H	4979175	VGT	10/23/2015	Updated Figure 1 and Figure 5. Added VCC_ABS spec and updated the SID.ADC.4 parameter. Added “Guaranteed by characterization” note for the following specs: SID.GIO#16, SID.GIO#17, SID.XRES#3, SID 160 to SID 172A, SID 2226, SID 229, SID.ADC.1 to SID.ADC.5.
*I	5028128	VGT	12/04/2015	Updated Application Diagrams: Added Figure 12. Added Figure 13. Added Figure 14. Updated Ordering Information. Added part numbers CYPD2119-24LQXIT, CYPD2120-24LQXIT, CYPD2121-24LQXIT, CYPD2125-24LQXIT.
*J	5186972	VGT	03/28/2016	Updated temperature ranges in Features. Updated Table 28. Updated Ordering Information.
*K	5303957	VGT	06/13/2016	Added Available Firmware and Software Tools. Updated Figure 8: Per the USB PD3.0 spec, SOP” implementation is no longer valid for passive cables. Updated Figure 9, Figure 10, and Figure 11. Added descriptive notes for the application diagrams. Added References and Links To Applications Collaterals. Updated Ordering Information. Updated Cypress logo and copyright information.
*L	5387677	VGT	08/02/2016	Added CYPD2122-24LQXI part number in Ordering Information.

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