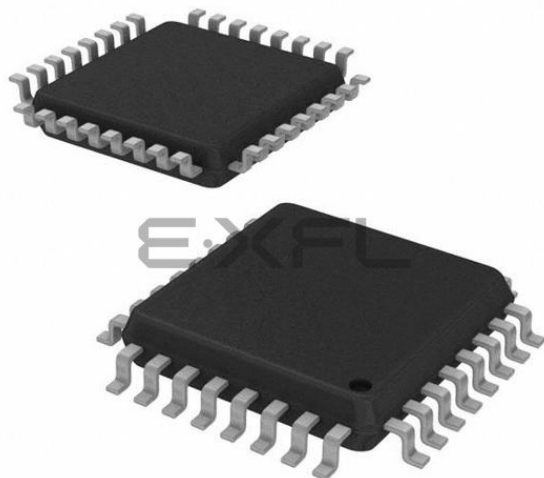




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbus, SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gr16avfje



Revision History

Chapter 11 Low-Voltage Inhibit (LVI)

11.1	Introduction	111
11.2	Features	111
11.3	Functional Description	111
11.3.1	Polled LVI Operation	112
11.3.2	Forced Reset Operation	112
11.3.3	Voltage Hysteresis Protection	113
11.3.4	LVI Trip Selection	113
11.4	LVI Status Register	113
11.5	LVI Interrupts	113
11.6	Low-Power Modes	113
11.6.1	Wait Mode	114
11.6.2	Stop Mode	114

Chapter 12 Input/Output (I/O) Ports

12.1	Introduction	115
12.2	Port A	118
12.2.1	Port A Data Register	118
12.2.2	Data Direction Register A	118
12.2.3	Port A Input Pullup Enable Register	120
12.3	Port B	120
12.3.1	Port B Data Register	120
12.3.2	Data Direction Register B	121
12.4	Port C	122
12.4.1	Port C Data Register	122
12.4.2	Data Direction Register C	122
12.4.3	Port C Input Pullup Enable Register	124
12.5	Port D	124
12.5.1	Port D Data Register	124
12.5.2	Data Direction Register D	125
12.5.3	Port D Input Pullup Enable Register	127
12.6	Port E	127
12.6.1	Port E Data Register	127
12.6.2	Data Direction Register E	128

Chapter 13 Resets and Interrupts

13.1	Introduction	131
13.2	Resets	131
13.2.1	Effects	131
13.2.2	External Reset	131
13.2.3	Internal Reset	131
13.2.3.1	Power-On Reset (POR)	131
13.2.3.2	Computer Operating Properly (COP) Reset	132

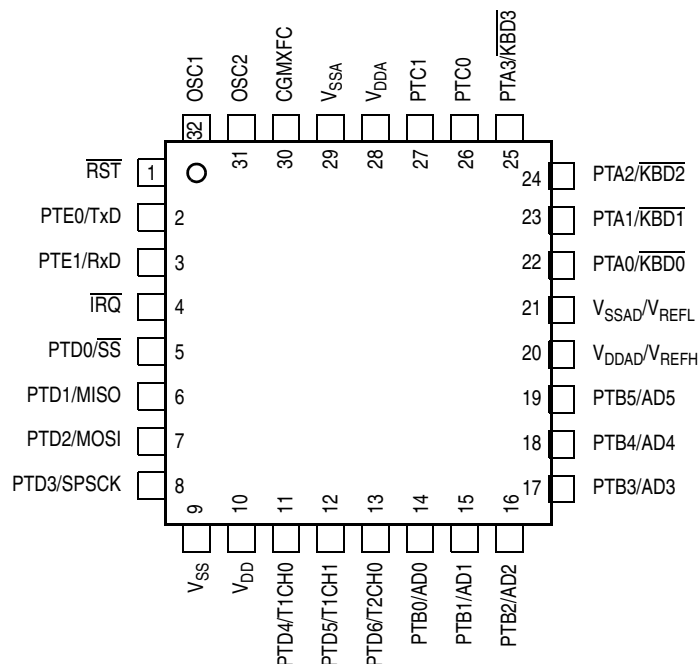


Figure 1-2. 32-Pin LQFP Pin Assignments

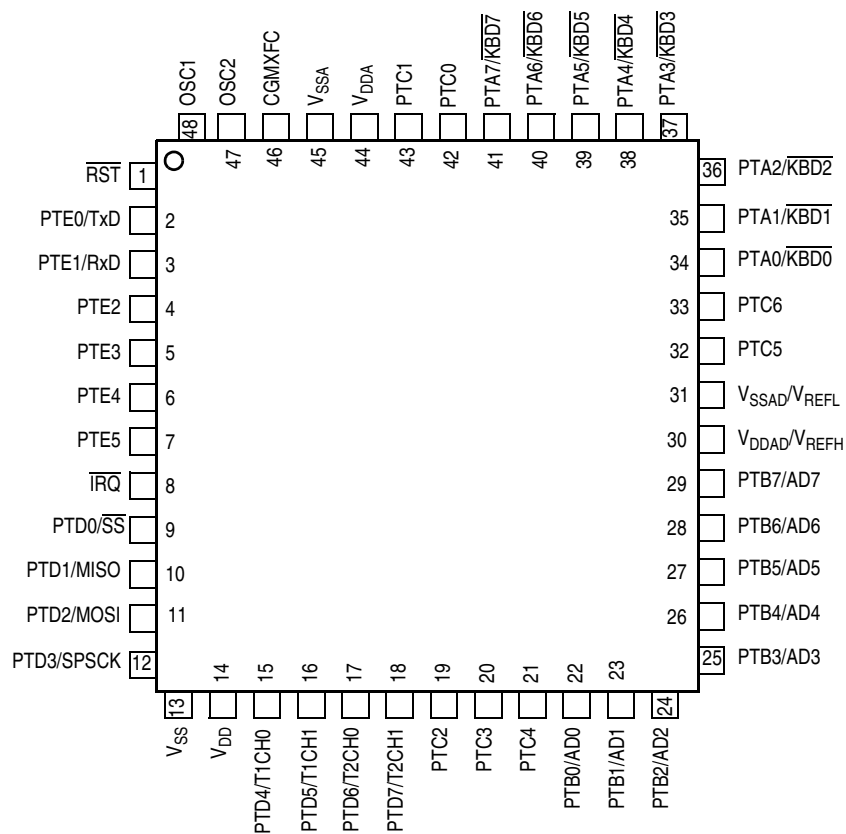


Figure 1-3. 48-Pin LQFP Pin Assignments

Memory

\$0000		\$FE03	BREAK FLAG CONTROL REGISTER (SBFCR)
↓		\$FE04	INTERRUPT STATUS REGISTER 1 (INT1)
\$003F		\$FE05	INTERRUPT STATUS REGISTER 2 (INT2)
\$0040		\$FE06	INTERRUPT STATUS REGISTER 3 (INT3)
↓		\$FE07	RESERVED
\$043F		\$FE08	FLASH CONTROL REGISTER (FLCR)
\$0440		\$FE09	BREAK ADDRESS REGISTER HIGH (BRKH)
↓		\$FE0A	BREAK ADDRESS REGISTER LOW (BRKL)
\$04FF		\$FE0B	BREAK STATUS AND CONTROL REGISTER (BRKSCR)
\$0500		\$FE0C	LVI STATUS REGISTER (LVISR)
↓		\$FE0D	
\$057F		↓	UNIMPLEMENTED 3 BYTES
\$0580		\$FE0F	
↓		\$FE10	UNIMPLEMENTED 16 BYTES
\$1BFF		↓	RESERVED FOR COMPATIBILITY WITH MONITOR CODE FOR A-FAMILY PART
\$1C00		\$FE1F	
↓		\$FE20	
\$1D95		↓	MONITOR ROM 350 BYTES
\$1D96		\$FF7D	
↓		\$FF7E	FLASH BLOCK PROTECT REGISTER (FLBPR)
\$BFFF		\$FF7F	
\$C000		↓	UNIMPLEMENTED 93 BYTES
↓		\$FFDB	
\$FDFF		\$FFDC	
\$FE00	BREAK STATUS REGISTER (SBSR)	↓	FLASH VECTORS 36 BYTES
\$FE01	SIM RESET STATUS REGISTER (SRSR)	\$FFFF ⁽¹⁾	
\$FE02	RESERVED		

1. \$FFF6–\$FFFD used for eight security bytes

Figure 2-1. Memory Map

Memory

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0024	Timer 1 Counter Modulo Register Low (T1MODL) See page 227.	Read: Write: Reset:	Bit 7	6	5	4	3	2	1	Bit 0
\$0025	Timer 1 Channel 0 Status and Control Register (T1SC0) See page 230.	Read: Write: Reset:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
\$0026	Timer 1 Channel 0 Register High (T1CH0H) See page 230.	Read: Write: Reset:	Bit 15	14	13	12	11	10	9	Bit 8
\$0027	Timer 1 Channel 0 Register Low (T1CH0L) See page 230.	Read: Write: Reset:	Bit 7	6	5	4	3	2	1	Bit 0
\$0028	Timer 1 Channel 1 Status and Control Register (T1SC1) See page 230.	Read: Write: Reset:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
\$0029	Timer 1 Channel 1 Register High (T1CH1H) See page 230.	Read: Write: Reset:	Bit 15	14	13	12	11	10	9	Bit 8
\$002A	Timer 1 Channel 1 Register Low (T1CH1L) See page 230.	Read: Write: Reset:	Bit 7	6	5	4	3	2	1	Bit 0
\$002B	Timer 2 Status and Control Register (T2SC) See page 227.	Read: Write: Reset:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
\$002C	Timer 2 Counter Register High (T2CNTH) See page 226.	Read: Write: Reset:	Bit 15	14	13	12	11	10	9	Bit 8
\$002D	Timer 2 Counter Register Low (T2CNTL) See page 226.	Read: Write: Reset:	Bit 7	6	5	4	3	2	1	Bit 0
\$002E	Timer 2 Counter Modulo Register High (T2MODH) See page 227.	Read: Write: Reset:	Bit 15	14	13	12	11	10	9	Bit 8
\$002F	Timer 2 Counter Modulo Register Low (T2MODL) See page 227.	Read: Write: Reset:	Bit 7	6	5	4	3	2	1	Bit 0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 7)

Chapter 3

Analog-to-Digital Converter (ADC)

3.1 Introduction

This section describes the 10-bit analog-to-digital converter (ADC).

3.2 Features

Features of the ADC module include:

- Eight channels with multiplexed input
- Linear successive approximation with monotonicity
- 10-bit resolution
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock
- Left or right justified result
- Left justified sign data mode

3.3 Functional Description

The ADC provides eight pins for sampling external sources at pins PTB7/KBD7–PTB0/KBD0. An analog multiplexer allows the single ADC converter to select one of eight ADC channels as ADC voltage in (V_{ADIN}). V_{ADIN} is converted by the successive approximation register-based analog-to-digital converter. When the conversion is completed, ADC places the result in the ADC data register and sets a flag or generates an interrupt. See Figure 3-2.

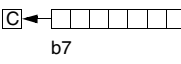
3.3.1 ADC Port I/O Pins

PTB7/AD7–PTB0/AD0 are general-purpose I/O (input/output) pins that share with the ADC channels. The channel select bits define which ADC channel/port pin will be used as the input signal. The ADC overrides the port I/O logic by forcing that pin as input to the ADC. The remaining ADC channels/port pins are controlled by the port I/O logic and can be used as general-purpose I/O. Writes to the port register or data direction register (DDR) will not have any affect on the port pin that is selected by the ADC. A read of a port pin in use by the ADC will return a 0.

7.7 Instruction Set Summary

Table 7-1 provides a summary of the M68HC08 instruction set.

Table 7-1. Instruction Set Summary (Sheet 1 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #opr ADC opr ADC opr ADC opr,X ADC opr,X ADC ,X ADC opr,SP ADC opr,SP	Add with Carry	$A \leftarrow (A) + (M) + (C)$	†	†	–	†	†	†	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #opr ADD opr ADD opr ADD opr,X ADD opr,X ADD ,X ADD opr,SP ADD opr,SP	Add without Carry	$A \leftarrow (A) + (M)$	†	†	–	†	†	†	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #opr	Add Immediate Value (Signed) to SP	$SP \leftarrow (SP) + (16 \ll M)$	–	–	–	–	–	–	IMM	A7	ii	2
AIX #opr	Add Immediate Value (Signed) to H:X	$H:X \leftarrow (H:X) + (16 \ll M)$	–	–	–	–	–	–	IMM	AF	ii	2
AND #opr AND opr AND opr AND opr,X AND opr,X AND ,X AND opr,SP AND opr,SP	Logical AND	$A \leftarrow (A) \& (M)$	0	–	–	†	†	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL opr ASLA ASLX ASL opr,X ASL ,X ASL opr,SP	Arithmetic Shift Left (Same as LSL)		†	–	–	†	†	†	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff ff	4 1 1 4 3 5
ASR opr ASRA ASRX ASR opr,X ASR opr,X ASR opr,SP	Arithmetic Shift Right		†	–	–	†	†	†	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff ff	4 1 1 4 3 5
BCC rel	Branch if Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? (C) = 0$	–	–	–	–	–	–	REL	24	rr	3
BCLR n, opr	Clear Bit n in M	$M_n \leftarrow 0$	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BCS rel	Branch if Carry Bit Set (Same as BLO)	$PC \leftarrow (PC) + 2 + rel ? (C) = 1$	–	–	–	–	–	–	REL	25	rr	3
BEQ rel	Branch if Equal	$PC \leftarrow (PC) + 2 + rel ? (Z) = 1$	–	–	–	–	–	–	REL	27	rr	3
BGE opr	Branch if Greater Than or Equal To (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (N \oplus V) = 0$	–	–	–	–	–	–	REL	90	rr	3
BGT opr	Branch if Greater Than (Signed Operands)	$PC \leftarrow (PC) + 2 + rel ? (Z) \mid (N \oplus V) = 0$	–	–	–	–	–	–	REL	92	rr	3
BHCC rel	Branch if Half Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? (H) = 0$	–	–	–	–	–	–	REL	28	rr	3
BHCS rel	Branch if Half Carry Bit Set	$PC \leftarrow (PC) + 2 + rel ? (H) = 1$	–	–	–	–	–	–	REL	29	rr	3
BHI rel	Branch if Higher	$PC \leftarrow (PC) + 2 + rel ? (C) \mid (Z) = 0$	–	–	–	–	–	–	REL	22	rr	3

Low-Power Modes

- Timebase module (TBM) interrupt — A TBM interrupt loads the program counter with the contents of locations \$FFDC and \$FFDD when the timebase counter has rolled over. This allows the TBM to generate a periodic wakeup from stop mode.

Upon exit from stop mode, the system clocks begin running after an oscillator stabilization delay. A 12-bit stop recovery counter inhibits the system clocks for 4096 CGMXCLK cycles after the reset or external interrupt.

The short stop recovery bit, SSREC, in the CONFIG1 register controls the oscillator stabilization delay during stop recovery. Setting SSREC reduces stop recovery time from 4096 CGMXCLK cycles to 32 CGMXCLK cycles.

NOTE

Use the full stop recovery time (SSREC = 0) in applications that use an external crystal.

11.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR} . This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF} . V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS} .

11.3.4 LVI Trip Selection

The LVI5OR3 bit in the configuration register selects whether the LVI is configured for 5-V or 3-V protection.

NOTE

The microcontroller is guaranteed to operate at a minimum supply voltage. The trip point (V_{TRIPF} [5 V] or V_{TRIPF} [3 V]) may be lower than this. See Chapter 20 Electrical Specifications for the actual trip point voltages.

11.4 LVI Status Register

The LVI status register (LVISR) indicates if the V_{DD} voltage was detected below the V_{TRIPF} level.

Address:	\$FE0C							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0
	= Unimplemented							

Figure 11-3. LVI Status Register (LVISR)

LVIOUT — LVI Output Bit

This read-only flag becomes set when the V_{DD} voltage falls below the V_{TRIPF} trip voltage (see Table 11-1). Reset clears the LVIOUT bit.

Table 11-1. LVIOUT Bit Indication

V_{DD}	LVIOUT
$V_{DD} > V_{TRIPR}$	0
$V_{DD} < V_{TRIPF}$	1
$V_{TRIPF} < V_{DD} < V_{TRIPR}$	Previous value

11.5 LVI Interrupts

The LVI module does not generate interrupt requests.

11.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby modes.

Chapter 12

Input/Output (I/O) Ports

12.1 Introduction

Bidirectional input-output (I/O) pins form five parallel ports. All I/O pins are programmable as inputs or outputs. All individual bits within port A, port C, and port D are software configurable with pullup devices if configured as input port bits. The pullup devices are automatically and dynamically disabled when a port bit is switched to output mode.

NOTE

Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS} . Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.

Not all port pins are bonded out in all packages. Care sure be taken to make any unbonded port pins an output to prevent them from being floating inputs.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0000	Port A Data Register (PTA) See page 118.	Read:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
\$0001	Port B Data Register (PTB) See page 120.	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
\$0002	Port C Data Register (PTC) See page 122.	Read:	1	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
		Write:								
		Reset:	Unaffected by reset							
\$0003	Port D Data Register (PTD) See page 124.	Read:	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
		Write:								
		Reset:	Unaffected by reset							
\$0004	Data Direction Register A (DDRA) See page 118.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			= Unimplemented							

Figure 12-1. I/O Port Register Summary

Input/Output (I/O) Ports

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0005	Data Direction Register B (DDRB) See page 121.	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0006	Data Direction Register C (DDRC) See page 122.	Read:	0	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0007	Data Direction Register D (DDRD) See page 125.	Read:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0008	Port E Data Register (PTE) See page 127.	Read:	0	0	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0
		Write:								
		Reset:	Unaffected by reset							
\$000C	Data Direction Register E (DDRE) See page 128.	Read:	0	0	DDRE5	DDRE4	DDRE3	DDRE2	DDRE1	DDRE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000D	Port A Input Pullup Enable Register (PTAPUE) See page 120.	Read:	PTAPUE7	PTAPUE6	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000E	Port C Input Pullup Enable Register (PTCPUE) See page 124.	Read:	0	PTCPUE6	PTCPUE5	PTCPUE4	PTCPUE3	PTCPUE2	PTCPUE1	PTCPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000F	Port D Input Pullup Enable Register (PTDPUE) See page 127.	Read:	PTDPUE7	PTDPUE6	PTDPUE5	PTDPUE4	PTDPUE3	PTDPUE2	PTDPUE1	PTDPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

Figure 12-1. I/O Port Register Summary (Continued)

Figure 12-15 shows the port D I/O logic.

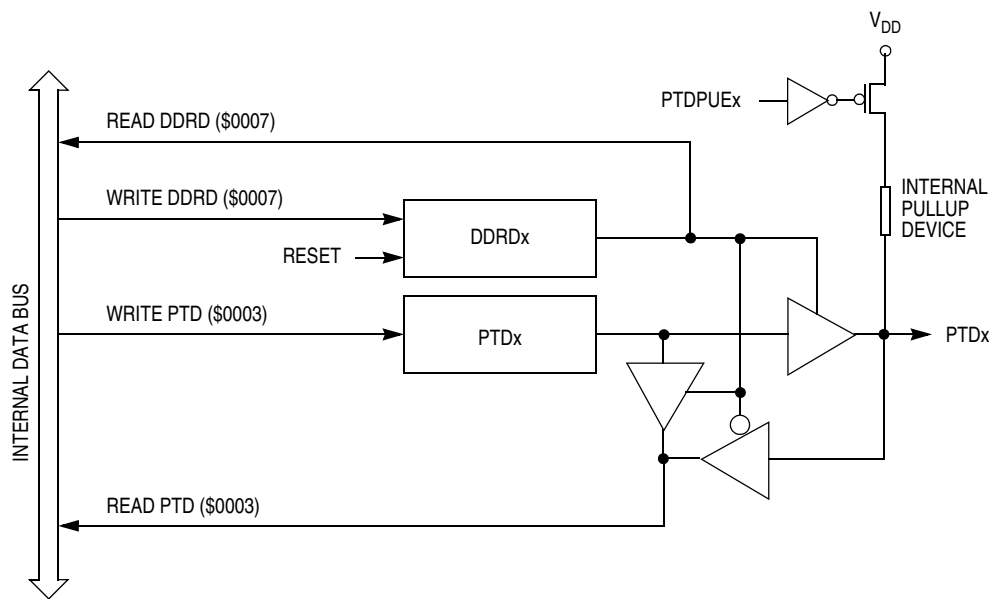


Figure 12-15. Port D I/O Circuit

When bit $DDRDx$ is a 1, reading address \$0003 reads the $PTDx$ data latch. When bit $DDRDx$ is a 0, reading address \$0003 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 12-5 summarizes the operation of the port D pins.

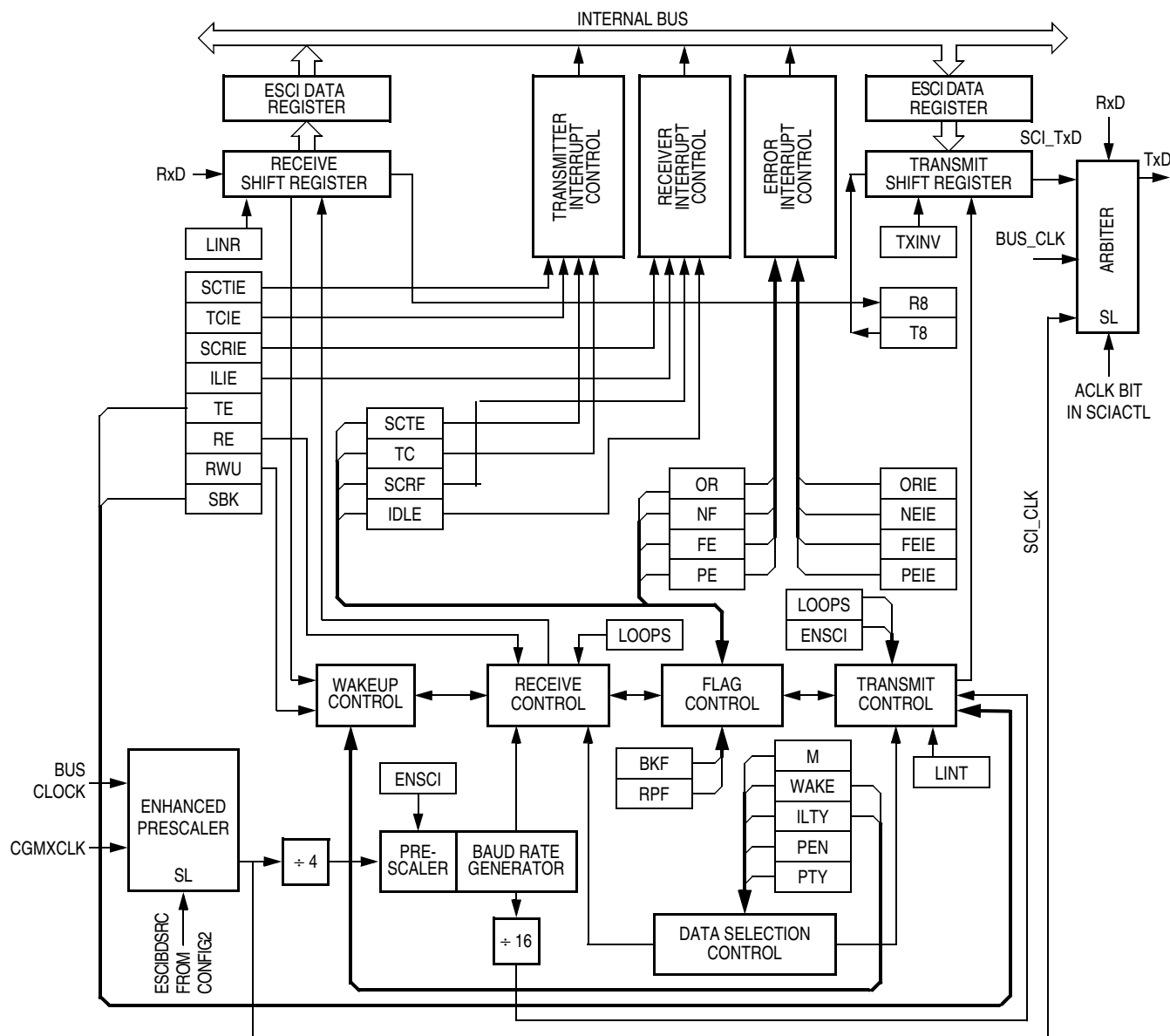
Table 12-5. Port D Pin Functions

PTDPUE Bit	DDRD Bit	PTD Bit	I/O Pin Mode	Accesses to DDRD	Accesses to PTD	
				Read/Write	Read	Write
1	0	X ⁽¹⁾	Input, V_{DD} ⁽²⁾	DDRD7–DDRD0	Pin	PTD7–PTD0 ⁽³⁾
0	0	X	Input, Hi-Z ⁽⁴⁾	DDRD7–DDRD0	Pin	PTD7–PTD0 ⁽³⁾
X	1	X	Output	DDRD7–DDRD0	PTD7–PTD0	PTD7–PTD0

1. X = Don't care
2. I/O pin pulled up to V_{DD} by internal pullup device.
3. Writing affects data register, but does not affect input.
4. Hi-Z = High impedance

14.4 Functional Description

Figure 14-2 shows the structure of the ESCI module. The ESCI allows full-duplex, asynchronous, NRZ serial communication between the MCU and remote devices, including other MCUs. The transmitter and receiver of the ESCI operate independently, although they use the same baud rate generator. During normal operation, the CPU monitors the status of the ESCI, writes the data to be transmitted, and processes received data.



SL = 1 -> SCI_CLK = BUSCLK
SL = 0 -> SCI_CLK = CGMXCLK (4x BUSCLK)

Figure 14-2. ESCI Module Block Diagram

14.4.1 Data Format

The SCI uses the standard non-return-to-zero mark/space data format illustrated in Figure 14-4.

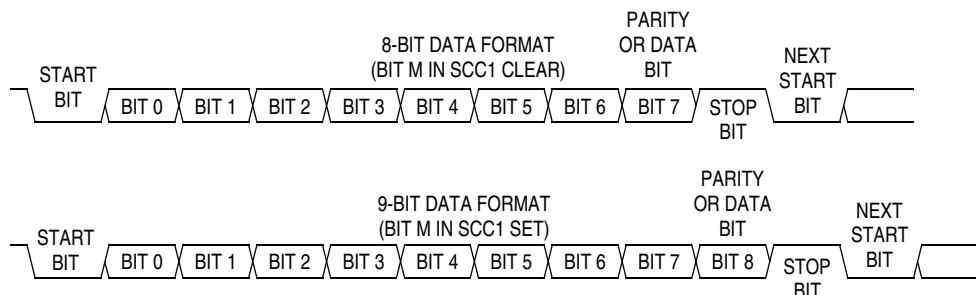


Figure 14-4. SCI Data Formats

14.4.2 Transmitter

Figure 14-5 shows the structure of the SCI transmitter and the registers are summarized in Figure 14-3. The baud rate clock source for the ESCI can be selected via the configuration bit, ESCIBDSRC.

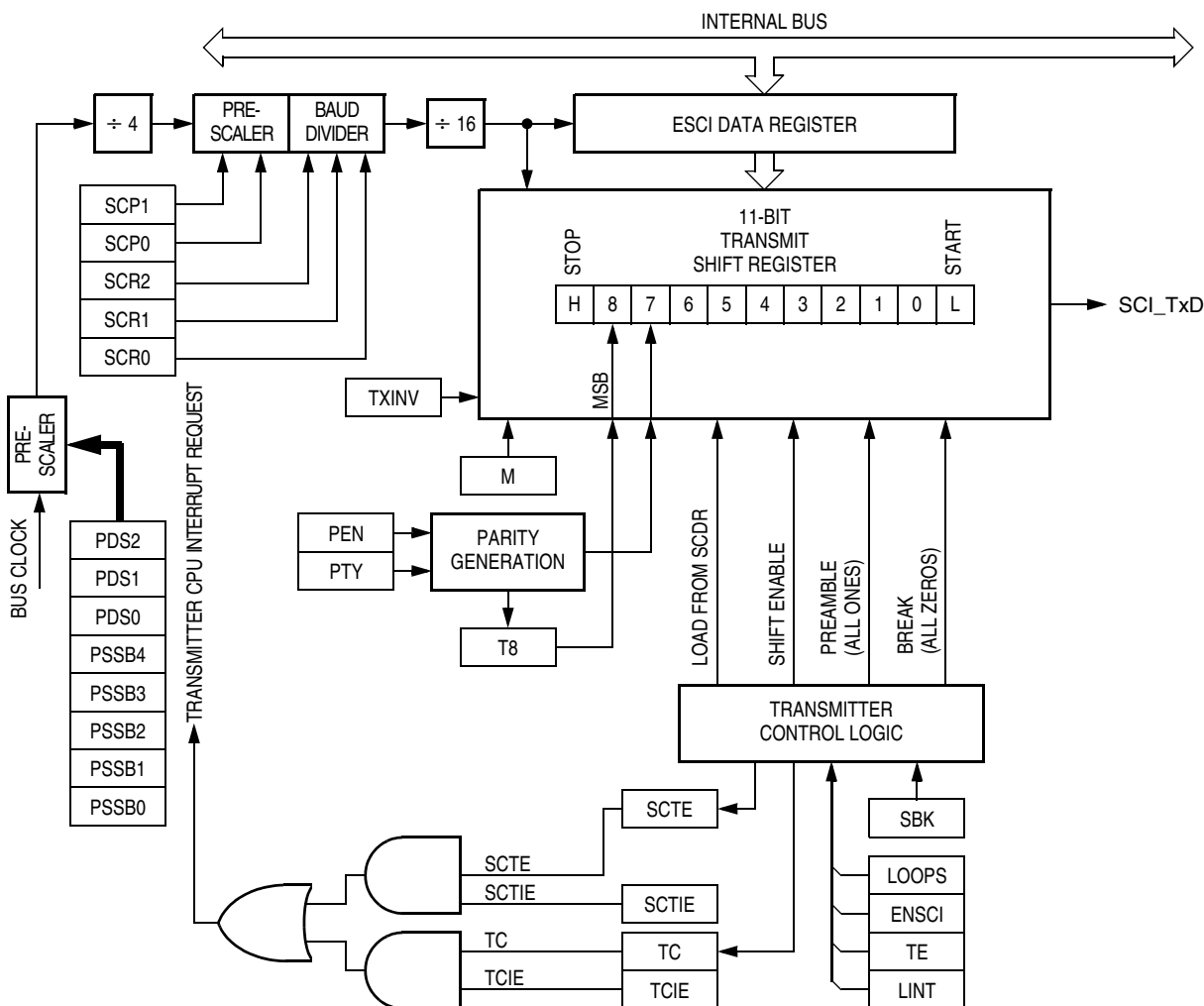


Figure 14-5. ESCI Transmitter

PDS2–PDS0 — Prescaler Divisor Select Bits

These read/write bits select the prescaler divisor as shown in Table 14-10. Reset clears PDS2–PDS0.

NOTE

The setting of '000' will bypass not only this prescaler but also the prescaler divisor fine adjust (PDFA). It is not recommended to bypass the prescaler while ENSCI is set, because the switching is not glitch free.

Table 14-10. ESCI Prescaler Division Ratio

PS[2:1:0]	Prescaler Divisor (PD)
0 0 0	Bypass this prescaler
0 0 1	2
0 1 0	3
0 1 1	4
1 0 0	5
1 0 1	6
1 1 0	7
1 1 1	8

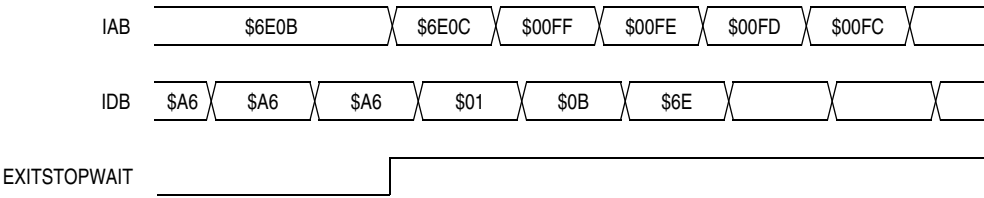
PSSB4–PSSB0 — Clock Insertion Select Bits

These read/write bits select the number of clocks inserted in each 32 output cycle frame to achieve more timing resolution on the **average** prescaler frequency as shown in Table 14-11. Reset clears PSSB4–PSSB0.

Table 14-11. ESCI Prescaler Divisor Fine Adjust

PSSB[4:3:2:1:0]	Prescaler Divisor Fine Adjust (PDFA)
0 0 0 0 0	0/32 = 0
0 0 0 0 1	1/32 = 0.03125
0 0 0 1 0	2/32 = 0.0625
0 0 0 1 1	3/32 = 0.09375
0 0 1 0 0	4/32 = 0.125
0 0 1 0 1	5/32 = 0.15625
0 0 1 1 0	6/32 = 0.1875
0 0 1 1 1	7/32 = 0.21875
0 1 0 0 0	8/32 = 0.25
0 1 0 0 1	9/32 = 0.28125
0 1 0 1 0	10/32 = 0.3125
0 1 0 1 1	11/32 = 0.34375
0 1 1 0 0	12/32 = 0.375
0 1 1 0 1	13/32 = 0.40625
0 1 1 1 0	14/32 = 0.4375
0 1 1 1 1	15/32 = 0.46875

Continued on next page



Note: EXITSTOPWAIT = $\overline{\text{RST}}$ pin or CPU interrupt

Figure 15-16. Wait Recovery from Interrupt

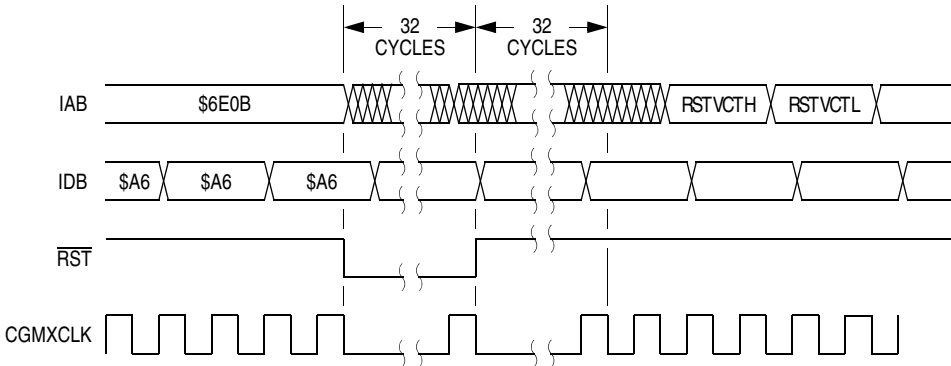


Figure 15-17. Wait Recovery from Internal Reset

15.6.2 Stop Mode

In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset causes an exit from stop mode.

The SIM disables the clock generator module outputs (CGMOUT and CGMXCLK) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the CONFIG1 register. If SSREC is set, stop recovery is reduced from the normal delay of 4096 CGMXCLK cycles down to 32. This is ideal for applications using canned oscillators that do not require long startup times from stop mode.

NOTE

External crystal applications should use the full stop recovery time by clearing the SSREC bit unless the OSCENINSTOP bit is set in CONFIG2.

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. Figure 15-18 shows stop mode entry timing. Figure 15-19 shows stop mode recovery time from interrupt.

NOTE

To minimize stop current, all pins configured as inputs should be driven to a 1 or 0.

16.6 Error Conditions

The following flags signal SPI error conditions:

- Overflow (OVRF) — Failing to read the SPI data register before the next full byte enters the shift register sets the OVRF bit. The new byte does not transfer to the receive data register, and the unread byte still can be read. OVRF is in the SPI status and control register.
- Mode fault error (MODF) — The MODF bit indicates that the voltage on the slave select pin ($\overline{SS}$) is inconsistent with the mode of the SPI. MODF is in the SPI status and control register.

16.6.1 Overflow Error

The overflow flag (OVRF) becomes set if the receive data register still has unread data from a previous transmission when the capture strobe of bit 1 of the next transmission occurs. The bit 1 capture strobe occurs in the middle of SPSCK cycle 7 (see Figure 16-5 and Figure 16-7.) If an overflow occurs, all data received after the overflow and before the OVRF bit is cleared does not transfer to the receive data register and does not set the SPI receiver full bit (SPRF). The unread data that transferred to the receive data register before the overflow occurred can still be read. Therefore, an overflow error always indicates the loss of data. Clear the overflow flag by reading the SPI status and control register and then reading the SPI data register.

OVRF generates a receiver/error CPU interrupt request if the error interrupt enable bit (ERRIE) is also set. The SPRF, MODF, and OVRF interrupts share the same CPU interrupt vector (see Figure 16-12.) It is not possible to enable MODF or OVRF individually to generate a receiver/error CPU interrupt request. However, leaving MODFEN low prevents MODF from being set.

If the CPU SPRF interrupt is enabled and the OVRF interrupt is not, watch for an overflow condition. Figure 16-10 shows how it is possible to miss an overflow. The first part of Figure 16-10 shows how it is possible to read the SPSCR and SPDR to clear the SPRF without problems. However, as illustrated by the second transmission example, the OVRF bit can be set in between the time that SPSCR and SPDR are read.

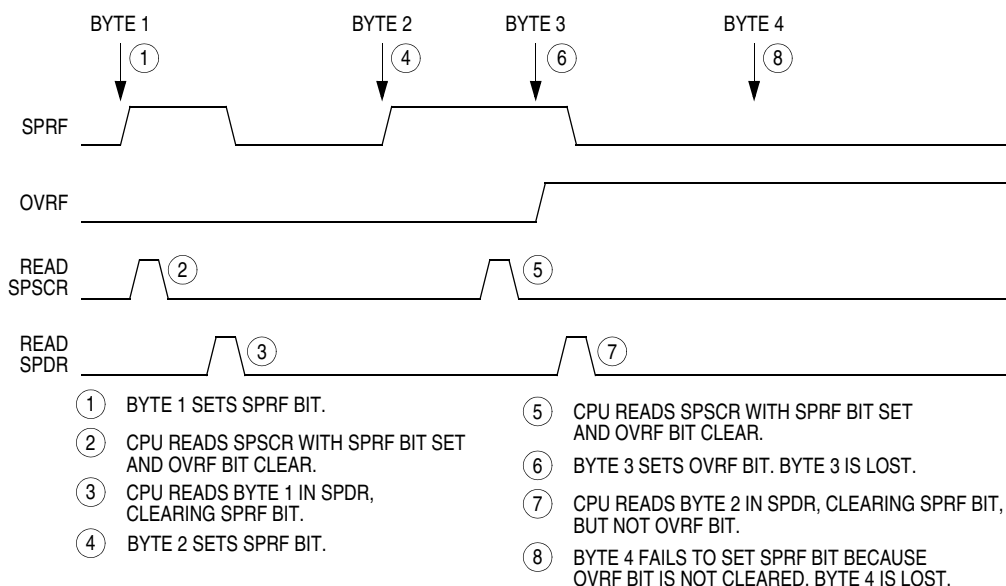


Figure 16-10. Missed Read of Overflow Condition

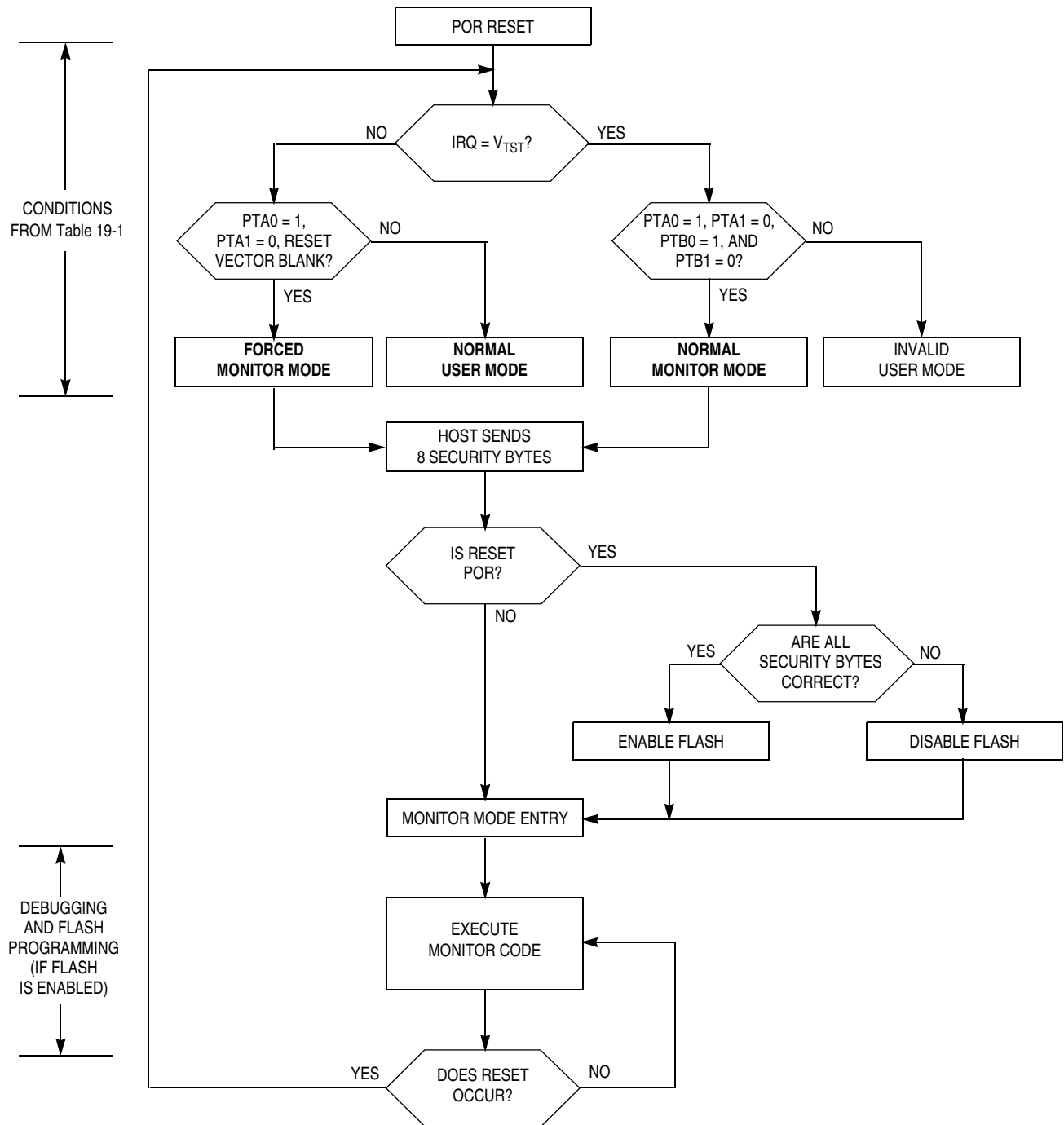


Figure 19-9. Simplified Monitor Mode Entry Flowchart

Chapter 20

Electrical Specifications

20.1 Introduction

This section contains electrical and timing specifications.

20.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to 20.5 5-Vdc Electrical Characteristics and 20.6 3.3-Vdc Electrical Characteristics for guaranteed operating conditions.

Characteristic ⁽¹⁾	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to + 6.0	V
Input voltage	V_{In}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Maximum current per pin excluding those specified below	I	± 15	mA
Maximum current for pins PTC0–PTC4	$I_{PTC0-PTC4}$	± 25	mA
Maximum current into V_{DD}	I_{MVDD}	150	mA
Maximum current out of V_{SS}	I_{MVSS}	150	mA
Storage temperature	T_{stg}	-55 to +150	°C

1. Voltages referenced to V_{SS}

NOTE

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \leq (V_{In} \text{ or } V_{Out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).