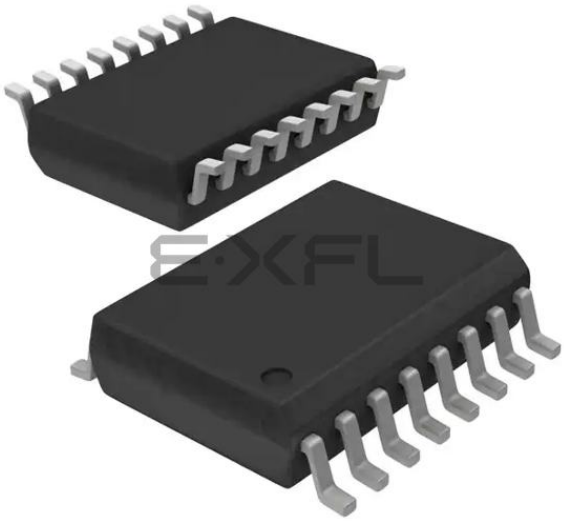

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	9
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t00cm6

Table of Contents

1 INTRODUCTION

The ST6200C, 01C and 03C devices are low cost members of the ST62xx 8-bit HCMOS family of microcontrollers, which is targeted at low to medium complexity applications. All ST62xx devices are based on a building block approach: a common core is surrounded by a number of on-chip peripherals.

The ST62E01C is the erasable EPROM version of the ST62T00C, T01 and T03C devices, which may be used during the development phase for the ST62T00C, T01 and T03C target devices, as well as the respective ST6200C, 01C and 03C ROM devices.

OTP and EPROM devices are functionally identical. OTP devices offer all the advantages of user programmability at low cost, which make them the ideal choice in a wide range of applications where frequent code changes, multiple code versions or last minute programmability are required.

The ROM based versions offer the same functionality, selecting the options defined in the programmable option bytes of the OTP/EPROM versions in the ROM option list (See Section 11.6 on page 92).

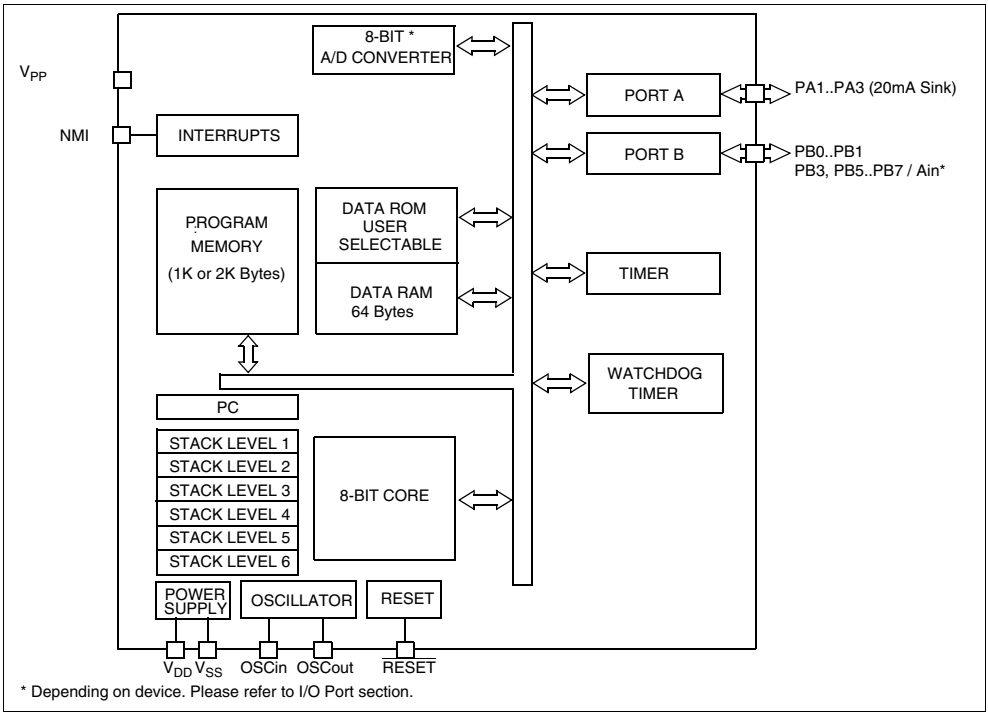
The ST62P00C, P01C and P03C are the **F**actory **A**dvanced **S**ervice **T**echnique ROM (FASTROM) versions of ST62T00C, T01 and T03C OTP devices.

They offer the same functionality as OTP devices, but they do not have to be programmed by the customer (See Section 11 on page 86).

These compact low-cost devices feature a Timer comprising an 8-bit counter with a 7-bit programmable prescaler, an 8-bit A/D Converter with 4 analog inputs (depending on device, see device summary on page 1) and a Digital Watchdog timer, making them well suited for a wide range of automotive, appliance and industrial applications.

For easy reference, all parametric data are located in Section 10 on page 58.

Figure 1. Block Diagram



* Depending on device. Please refer to I/O Port section.

MEMORY MAP (Cont'd)

3.1.2 Program Space

Program Space comprises the instructions to be executed, the data required for immediate addressing mode instructions, the reserved factory test area and the user vectors. Program Space is addressed via the 12-bit Program Counter register (PC register). Thus, the MCU is capable of addressing 4K bytes of memory directly.

3.1.3 Readout Protection

The Program Memory in in OTP, EPROM or ROM devices can be protected against external readout of memory by setting the Readout Protection bit in the option byte (Section 3.3 on page 15).

In the EPROM parts, Readout Protection option can be desactivated only by U.V. erasure that also results in the whole EPROM context being erased.

Note: Once the Readout Protection is activated, it is no longer possible, even for STMicroelectronics, to gain access to the OTP or ROM contents. Returned parts can therefore not be accepted if the Readout Protection bit is set.

3.1.4 Data Space

Data Space accommodates all the data necessary for processing the user program. This space comprises the RAM resource, the processor core and peripheral registers, as well as read-only data such as constants and look-up tables in OTP/EPROM.

3.1.4.1 Data ROM

All read-only data is physically stored in program memory, which also accommodates the Program Space. The program memory consequently contains the program code to be executed, as well as the constants and look-up tables required by the application.

The Data Space locations in which the different constants and look-up tables are addressed by the processor core may be thought of as a 64-byte window through which it is possible to access the read-only data stored in OTP/EPROM.

3.1.4.2 Data RAM

The data space includes the user RAM area, the accumulator (A), the indirect registers (X), (Y), the short direct registers (V), (W), the I/O port registers, the peripheral data and control registers, the interrupt option register and the Data ROM Window register (DRWR register).

3.1.5 Stack Space

Stack space consists of six 12-bit registers which are used to stack subroutine and interrupt return addresses, as well as the current program counter contents.

5 CLOCKS, SUPPLY AND RESET

5.1 CLOCK SYSTEM

The main oscillator of the MCU can be driven by any of these clock sources:

– external clock signal

– external AT-cut parallel-resonant crystal

– external ceramic resonator

– external RC network (R_{NET}).

In addition, an on-chip Low Frequency Auxiliary Oscillator (LFAO) is available as a back-up clock system or to reduce power consumption.

An optional Oscillator Safeguard (OSG) filters spikes from the oscillator lines, and switches to the LFAO backup oscillator in the event of main oscillator failure. It also automatically limits the internal clock frequency (f_{INT}) as a function of V_{DD}, in order to guarantee correct operation. These functions are illustrated in Figure 10, and Figure 11.

Table 5 illustrates various possible oscillator configurations using an external crystal or ceramic resonator, an external clock input, an external resistor (R_{NET}), or the lowest cost solution using only the LFAO.

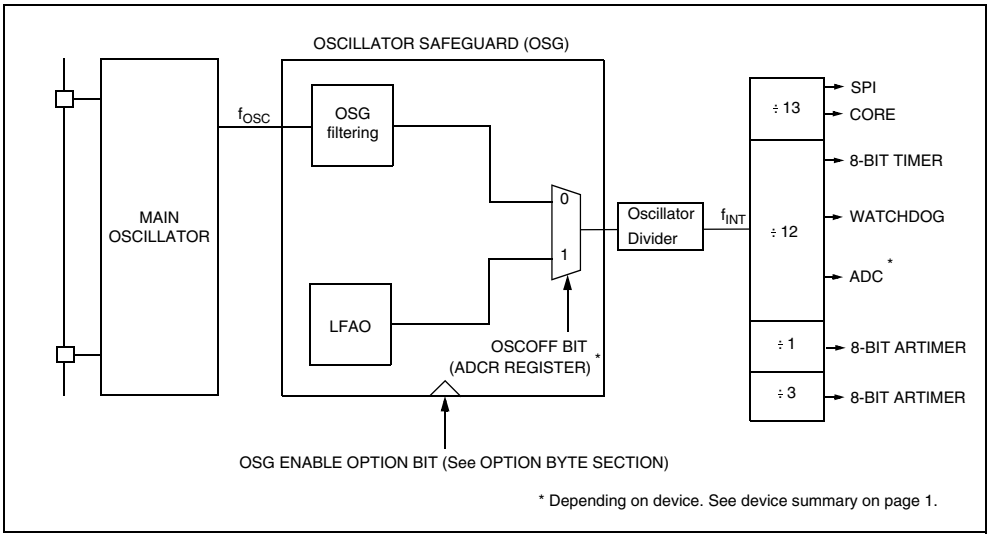
For more details on configuring the clock options, refer to the Option Bytes section of this document.

The internal MCU clock frequency (f_{INT}) is divided by 12 to drive the Timer, the Watchdog timer and the A/D converter, by 13 to drive the CPU core and the SPI and by 1 or 3 to drive the ARTIMER, as shown in Figure 9.

With an 8 MHz oscillator, the fastest CPU cycle is therefore 1.625µs.

A CPU cycle is the smallest unit of time needed to execute any operation (for instance, to increment the Program Counter). An instruction may require two, four, or five CPU cycles for execution.

Figure 9. Clock Circuit Block Diagram



5.4 INTERRUPTS

The ST6 core may be interrupted by four maskable interrupt sources, in addition to a Non Maskable Interrupt (NMI) source. The interrupt processing flowchart is shown in Figure 18.

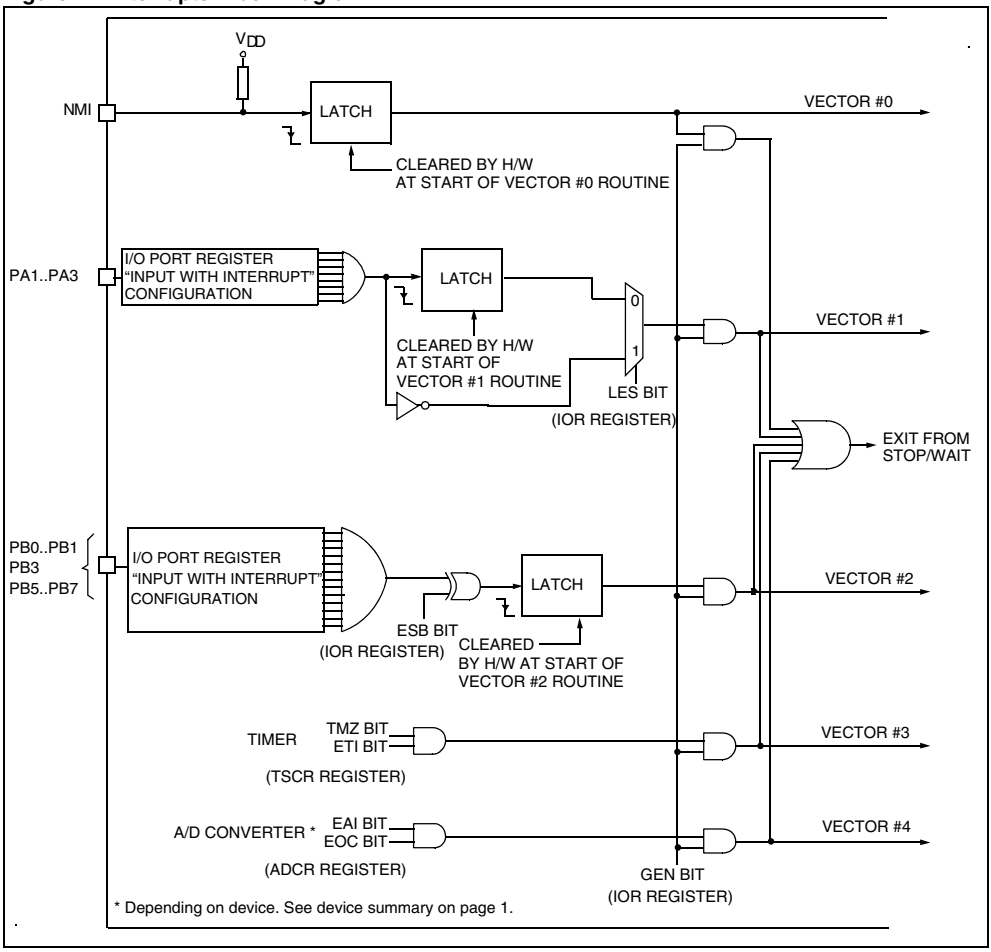
Maskable interrupts must be enabled by setting the GEN bit in the IOR register. However, even if they are disabled (GEN bit = 0), interrupt events are latched and may be processed as soon as the GEN bit is set.

Each source is associated with a specific Interrupt Vector, located in Program space (see Table 7). In the vector location, the user must write a Jump instruction to the associated interrupt service routine.

When an interrupt source generates an interrupt request, the PC register is loaded with the address of the interrupt vector, which then causes a Jump to the relevant interrupt service routine, thus servicing the interrupt.

Interrupt are triggered by events either on external pins, or from the on-chip peripherals. Several events can be ORed on the same interrupt vector. On-chip peripherals have flag registers to determine which event triggered the interrupt.

Figure 17. Interrupts Block Diagram



7 I/O PORTS

7.1 INTRODUCTION

Each I/O port contains up to 8 pins. Each pin can be programmed independently as digital input (with or without pull-up and interrupt generation), digital output (open drain, push-pull) or analog input (when available).

The I/O pins can be used in either standard or alternate function mode.

Standard I/O mode is used for:

– Transfer of data through digital inputs and outputs (on specific pins):

– External interrupt generation

Alternate function mode is used for:

– Alternate signal input/output for the on-chip peripherals

The generic I/O block diagram is shown in Figure 23.

7.2 FUNCTIONAL DESCRIPTION

Each port is associated with 3 registers located in Data space:

– Data Register (DR)

– Data Direction Register (DDR)

– Option Register (OR)

Each I/O pin may be programmed using the corresponding register bits in the DDR, DR and OR registers: bit x corresponding to pin x of the port. Table 8 illustrates the various port configurations which can be selected by user software.

During MCU initialization, all I/O registers are cleared and the input mode with pull-up and no interrupt generation is selected for all the pins, thus avoiding pin conflicts.

7.2.1 Digital Input Modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Different input modes can be selected by software through the DR and OR registers, see Table 8.

External Interrupt Function

All input lines can be individually connected by software to the interrupt system by programming the OR and DR registers accordingly. The interrupt trigger modes (falling edge, rising edge and low level) can be configured by software for each port as described in the Interrupt section.

7.2.2 Analog Inputs

Some pins can be configured as analog inputs by programming the OR and DR registers accordingly, see Table 8. These analog inputs are connected to the on-chip 8-bit Analog to Digital Converter.

Caution: ONLY ONE pin should be programmed as an analog input at any time, since by selecting more than one input simultaneously their pins will be effectively shorted.

7.2.3 Output Modes

The output configuration is selected by setting the corresponding DDR register bit. In this case, writing to the DR register applies this digital value to the I/O pin through the latch. Then, reading the DR register returns the previously stored value.

Two different output modes can be selected by software through the OR register: push-pull and open-drain.

DR register value and output pin status:

DR	Push-pull	Open-drain
0	V_{SS}	V_{SS}
1	V_{DD}	Floating

Note: The open drain setting is not a true open drain. This means it has the same structure as the push-pull setting but the P-buffer is deactivated. To avoid damaging the device, please respect the V_{OUT} absolute maximum rating described in the Electrical Characteristics section.

7.2.4 Alternate Functions

When an on-chip peripheral is configured to use a pin, the alternate function (timer input/output...) is not systematically selected but has to be configured through the DDR, OR and DR registers. Refer to the chapter describing the peripheral for more details.

WATCHDOG TIMER (Cont'd)

These instructions test the C bit and reset the MCU (i.e. disable the Watchdog) if the bit is set (i.e. if the Watchdog is active), thus disabling the Watchdog.

For more information on the use of the watchdog, please read application note AN1015.

Note: This note applies only when the watchdog is used as a standard timer. It is recommended to read the counter twice, as it may sometimes return an invalid value if the read is performed while the counter is decremented (counter bits in transient state). To validate the return value, both values read must be equal. The counter decrements every 384 µs at 8 MHz f_{OSC}.

8.1.5 Low Power Modes

Mode	Description
WAIT	No effect on Watchdog.
STOP	Behaviour depends on the EXTCNTL option in the Option bytes: **1. Watchdog disabled:** The MCU will enter Stop mode if a STOP instruction is executed. **2. Watchdog enabled and EXTCNTL option disabled:** If a STOP instruction is encountered, it is interpreted as a WAIT. **3. Watchdog and EXTCNTL option enabled:** If a STOP instruction is encountered when the NMI pin is low, it is interpreted as a WAIT. If, however, the STOP instruction is encountered when the NMI pin is high, the Watchdog counter is frozen and the CPU enters STOP mode. When the MCU exits STOP mode (i.e. when an interrupt is generated), the Watchdog resumes its activity.

8.1.6 Interrupts

None.

8.2 8-BIT TIMER

8.2.1 Introduction

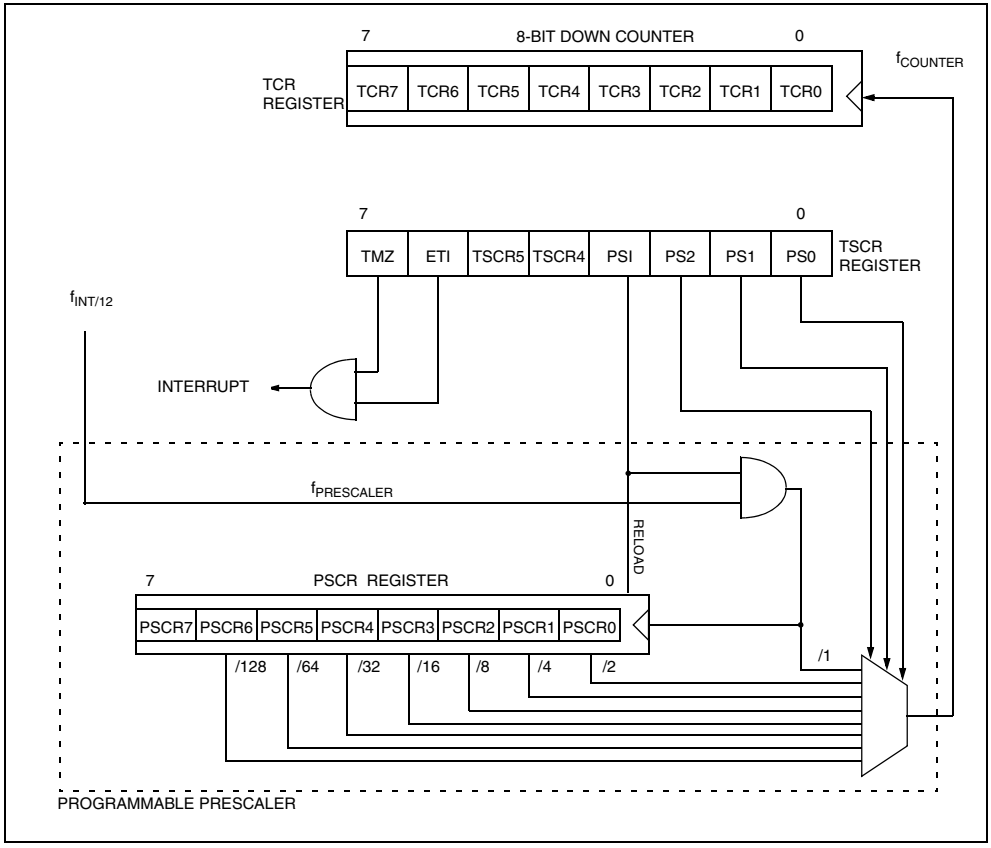
The 8-Bit Timer on-chip peripheral is a free running downcounter based on an 8-bit downcounter with a 7-bit programmable prescaler, giving a maximum count of 2^{15}.

8.2.2 Main Features

- Time-out downcounting mode with up to 15-bit accuracy
- Interrupt capability on counter underflow

The timer can be used in WAIT mode to wake up the MCU.

Figure 27. Timer Block Diagram



8.3 A/D CONVERTER (ADC)

8.3.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 8-bit, successive approximation converter. This peripheral has multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from different sources.

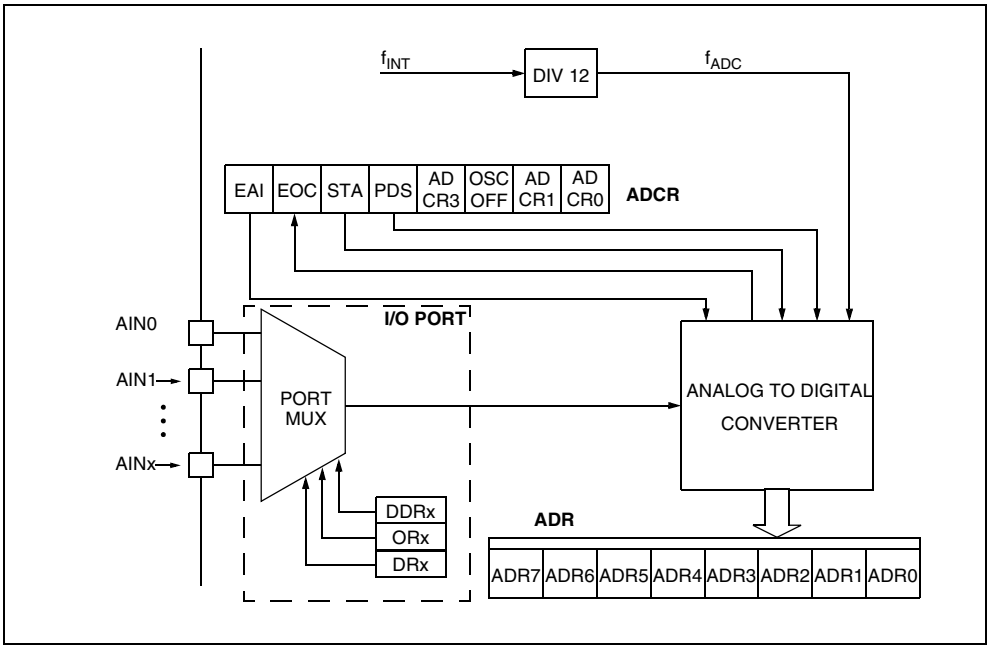
The result of the conversion is stored in a 8-bit Data Register. The A/D converter is controlled through a Control Register.

8.3.2 Main Features

- 8-bit conversion
- Multiplexed analog input channels
- Linear successive approximation
- Data register (DR) which contains the results
- End of Conversion flag
- On/Off bit (to reduce consumption)
- Typical conversion time 70 µs (with an 8 MHz crystal)

The block diagram is shown in Figure 28.

Figure 28. ADC Block Diagram



Note: ADC not present on some devices. See device summary on page 1.

Opcode Map Summary (Continued)

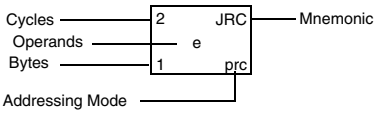
LOW / HI	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW / HI
0 **0000**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b.d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 prc	4 LD a,(y) 1 ind	**0** **0000**
1 **0001**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b.d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 prc	4 LD a,rr 2 dir	**1** **0001**
2 **0010**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b.d	2 JRZ e 1 pcr	4 COM a	2 JRC e 1 prc	4 CP a,(y) 1 ind	**2** **0010**
3 **0011**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b.d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 prc	4 CP a,rr 2 dir	**3** **0011**
4 **0100**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b.d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 prc	4 ADD a,(y) 1 ind	**4** **0100**
5 **0101**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b.d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 prc	4 ADD a,rr 2 dir	**5** **0101**
6 **0110**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b.d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 prc	4 INC (y) 1 ind	**6** **0110**
7 **0111**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b.d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 prc	4 INC rr 2 dir	**7** **0111**
8 **1000**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b.d	2 JRZ e 1 pcr	# 1 prc	2 JRC e 1 prc	4 LD (y),a 1 ind	**8** **1000**
9 **1001**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b.d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 prc	4 LD rr,a 2 dir	**9** **1001**
A **1010**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b.d	2 JRZ e 1 pcr	4 RCL a 1 inh	2 JRC e 1 prc	4 AND a,(y) 1 ind	**A** **1010**
B **1011**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b.d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 prc	4 AND a,rr 2 dir	**B** **1011**
C **1100**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b.d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 prc	4 SUB a,(y) 1 ind	**C** **1100**
D **1101**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b.d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 prc	4 SUB a,rr 2 dir	**D** **1101**
E **1110**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b.d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 prc	4 DEC (y) 1 ind	**E** **1110**
F **1111**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b.d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 prc	4 DEC rr 2 dir	**F** **1111**

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5-bit Displacement
b	3-bit Address
rr	1-byte Data space address
nn	1-byte immediate data
abc	12-bit address
ee	8-bit Displacement



10 ELECTRICAL CHARACTERISTICS

10.1 PARAMETER CONDITIONS

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

10.1.2 Typical Values

Unless otherwise specified, typical data are based on T_A=25°C, V_{DD}=5V (for the 4.5V≤V_{DD}≤6.0V voltage range) and V_{DD}=3.3V (for the 3V≤V_{DD}≤3.6V voltage range). They are given only as design guidelines and are not tested.

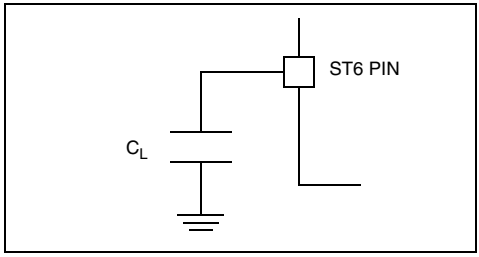
10.1.3 Typical Curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading Capacitor

The loading conditions used for pin parameter measurement is shown in Figure 30.

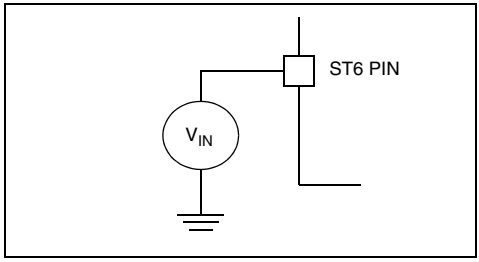
Figure 30. Pin Loading Conditions



10.1.5 Pin Input Voltage

The input voltage measurement on a pin of the device is described in Figure 31.

Figure 31. Pin Input Voltage



SUPPLY CURRENT CHARACTERISTICS (Cont'd)

Figure 38. Typical I_{DD} in WAIT vs f_{CPU} and Temperature for OTP devices with option bytes not programmed

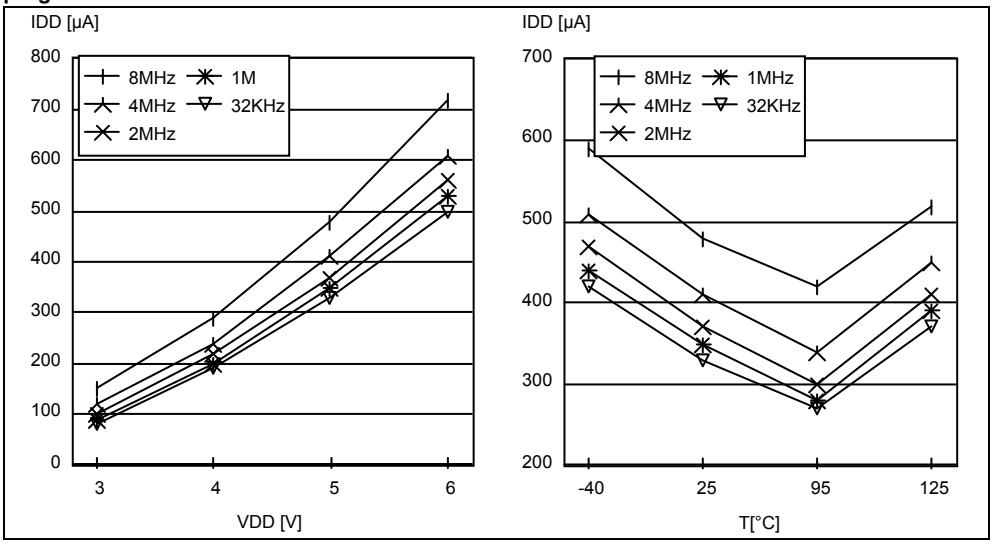
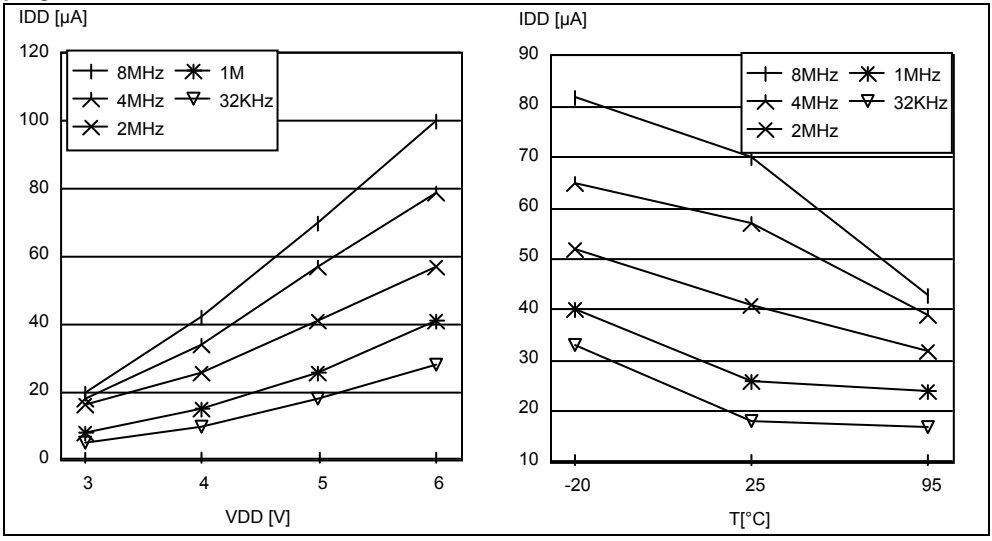


Figure 39. Typical I_{DD} in WAIT vs f_{CPU} and Temperature for OTP devices with option bytes programmed to 00H



10.5 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

10.5.1 General Timings

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	4	5	t_{CPU}
		f_{CPU}=8 MHz	3.25	6.5	8.125	µs
$t_{v(IT)}$	Interrupt reaction time [2] $t_{v(IT)} = \Delta t_{c(INST)} + 6$		6		11	t_{CPU}
		f_{CPU}=8 MHz	9.75		17.875	µs

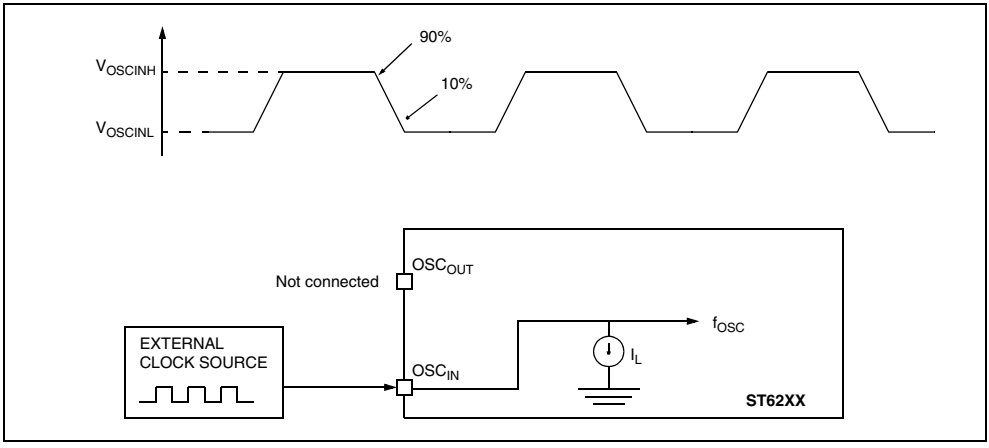
10.5.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSCINH}	OSC_{IN} input pin high level voltage	See Figure 43	$0.7xV_{DD}$		V_{DD}	V
V_{OSCINL}	OSC_{IN} input pin low level voltage		V_{SS}		$0.3xV_{DD}$	
I_L	OSCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			± 2	µA

Notes:

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

Figure 43. Typical Application with an External Clock Source



CLOCK AND TIMING CHARACTERISTICS (Cont'd)

10.5.4 RC Oscillator

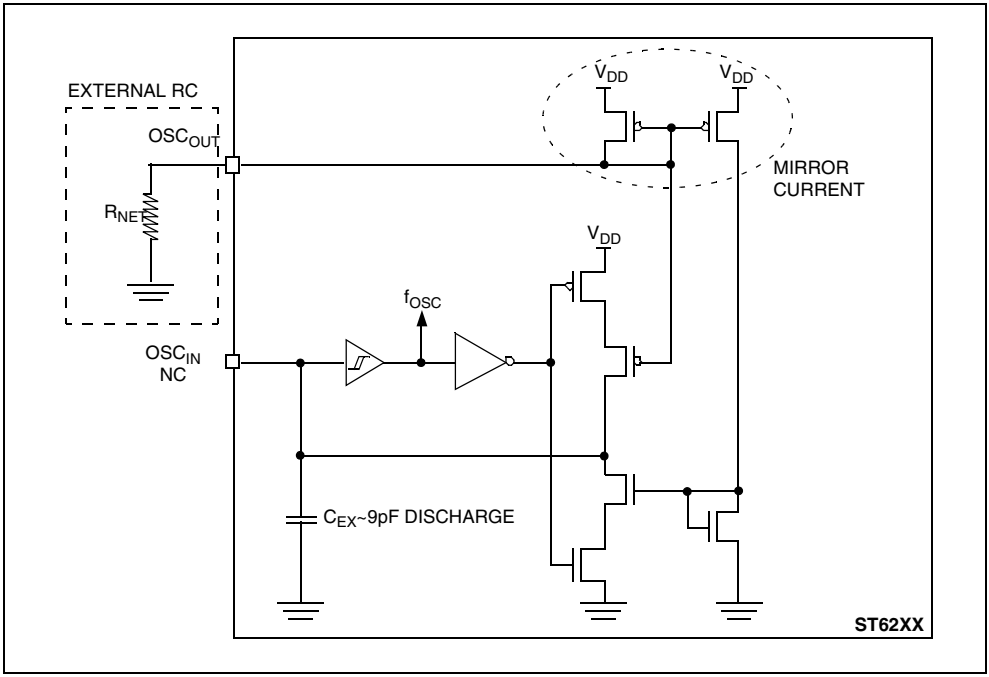
The ST6 internal clock can be supplied with an external RC oscillator. Depending on the R_{NET} value, the accuracy of the frequency is about 20%, so it may not be suitable for some applications.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{OSC}	RC oscillator frequency [1]	4.5V≤V_{DD}≤6.0V	R_{NET}=22 kΩ	7.2	8.6	10	MHz
			R_{NET}=47 kΩ	5.1	5.7	6.5	
			R_{NET}=100 kΩ	3.2	3.4	3.8	
			R_{NET}=220 kΩ	1.8	1.9	2	
			R_{NET}=470 kΩ	0.9	0.95	1.1	
		3V≤V_{DD}≤3.6V	R_{NET}=22 kΩ	3.7	4.3	4.9	
			R_{NET}=47 kΩ	2.8	3	3.3	
			R_{NET}=100 kΩ	1.8	1.9	2	
			R_{NET}=220 kΩ	1	1.1	1.2	
			R_{NET}=470 kΩ	0.5	0.55	0.6	
R_{NET}	RC Oscillator external resistor [2]		see Figure 46 & Figure 47	22		870	kΩ

Notes:

1. Data based on characterization results, not tested in production. These measurements were done with the OSCin pin unconnected (only soldered on the PCB).
2. R_{NET} must have a positive temperature coefficient (ppm/°C), carbon resistors should therefore not be used.

Figure 45. Typical Application with RC Oscillator



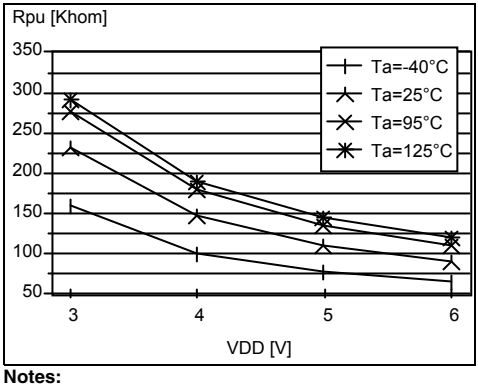
10.8 I/O PORT PIN CHARACTERISTICS

10.8.1 General Characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IL}	Input low level voltage [2]					$0.3xV_{DD}$	V
V_{IH}	Input high level voltage [2]			$0.7xV_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis [3]	V_{DD}=5V		200	400		mV
		V_{DD}=3.3V		200	400		
I_L	Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ (no pull-up configured)			0.1	1	µA
R_{PU}	Weak pull-up equivalent resistor [4]	$V_{IN}=V_{SS}$	V_{DD}=5V	40	110	350	kΩ
			V_{DD}=3.3V	80	230	700	
C_{IN}	I/O input pin capacitance				5	10	pF
C_{OUT}	I/O output pin capacitance				5	10	pF
$t_{f(IO)out}$	Output high to low level fall time [5]	C_L=50pF Between 10% and 90%			30		ns
$t_{r(IO)out}$	Output low to high level rise time [5]				35		
$t_{w(IT)in}$	External interrupt pulse time [6]			1			t_{CPU}

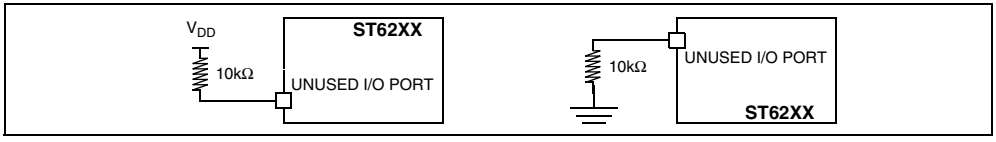
Figure 55. Typical R_{PU} vs. V_{DD} with $V_{IN} = V_{SS}$



Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=5V.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The R_{PU} pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, not tested in production.
5. Data based on characterization results, not tested in production.
6. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 56. Two typical Applications with unused I/O Pin



I/O PORT PIN CHARACTERISTICS (Cont'd)

10.8.2 Output Driving Current

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL} 1)	Output low level voltage for a standard I/O pin (see Figure 57 and Figure 60)	V_{DD}=5V	I_{IO}=+10µA, $T_A \leq 125°C$		0.1	V
			I_{IO}=+3mA, $T_A \leq 125°C$		0.8	
			I_{IO}=+5mA, $T_A \leq 85°C$		0.8	
			I_{IO}=+10mA, $T_A \leq 85°C$		1.2	
	Output low level voltage for a high sink I/O pin (see Figure 58 and Figure 61)		I_{IO}=+10µA, $T_A \leq 125°C$		0.1	
			I_{IO}=+7mA, $T_A \leq 125°C$		0.8	
			I_{IO}=+10mA, $T_A \leq 85°C$		0.8	
			I_{IO}=+15mA, $T_A \leq 125°C$		1.3	
			I_{IO}=+20mA, $T_A \leq 85°C$		1.3	
			I_{IO}=+30mA, $T_A \leq 85°C$		2	
V_{OH} 2)	Output high level voltage for an I/O pin (see Figure 59 and Figure 62)		I_{IO}=-10µA, $T_A \leq 125°C$	V_{DD}-0.1		
			I_{IO}=-3mA, $T_A \leq 125°C$	V_{DD}-1.5		
			I_{IO}=-5mA, $T_A \leq 85°C$	V_{DD}-1.5		

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 10.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current source must always respect the absolute maximum rating specified in Section 10.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}. True open drain I/O pins does not have V_{OH}.

Figure 57. Typical V_{OL} at V_{DD} = 5V (standard)

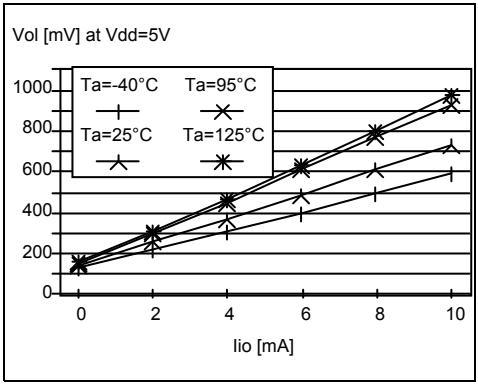
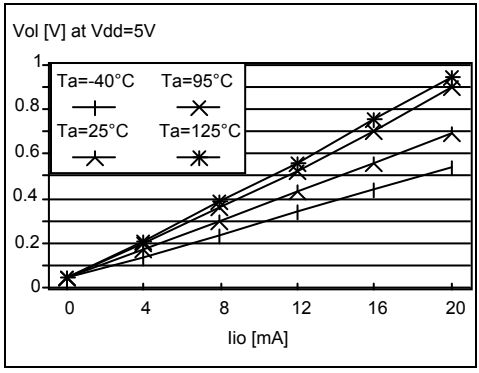


Figure 58. Typical V_{OL} at V_{DD} = 5V (high-sink)



10.9 CONTROL PIN CHARACTERISTICS

10.9.1 Asynchronous $\overline{\text{RESET}}$ Pin

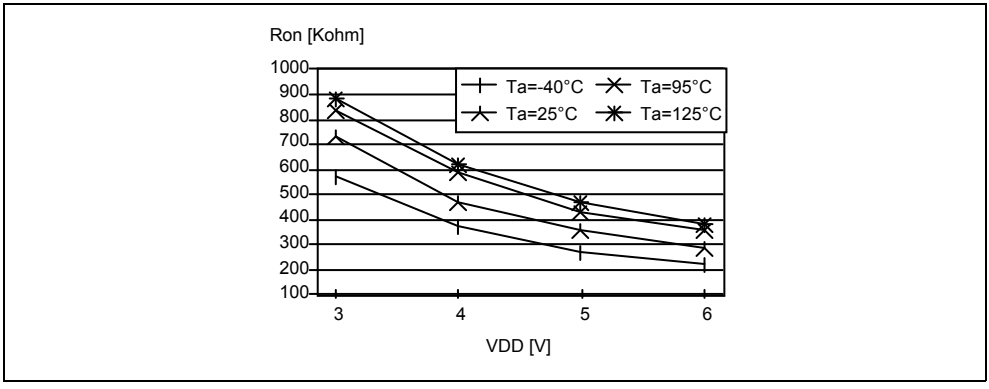
Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IL}	Input low level voltage [2]					$0.3xV_{DD}$	V
V_{IH}	Input high level voltage [2]			$0.7xV_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis [3]			200	400		mV
R_{ON}	Weak pull-up equivalent resistor [4]	$V_{IN}=V_{SS}$	V_{DD}=5V	150	350	900	kΩ
			V_{DD}=3.3V	300	730	1900	
R_{ESD}	ESD resistor protection	$V_{IN}=V_{SS}$	V_{DD}=5V		2.8		kΩ
			V_{DD}=3.3V				
$t_{w(RSTL)out}$	Generated reset pulse duration	External pin or internal reset sources					t_{CPU} µs
$t_{h(RSTL)in}$	External reset pulse hold time [5]						µs
$t_{g(RSTL)in}$	Filtered glitch duration [6]						ns

Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=5V.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, not tested in production.
5. All short pulse applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.
6. The reset network protects the device against parasitic resets, especially in a noisy environment.
7. The output of the external reset circuit must have an open-drain output to drive the ST6 reset pad. Otherwise the device can be damaged when the ST6 generates an internal reset (LVD or watchdog).

Figure 63. Typical R_{ON} vs V_{DD} with $V_{IN}=V_{SS}$



11.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient) DIP16 SO16 SSOP16	 90 90 125	°C/W
P_D	Power dissipation [1]	500	mW
T_{Jmax}	Maximum junction temperature [2]	150	°C

Notes:

1. The power dissipation is obtained from the formula $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD}xV_{DD}$) and P_{PORT} is the port power dissipation determined by the user.
2. The average chip-junction temperature can be obtained from the formula $T_J = T_A + P_D$ x RthJA.

11.3 ECOPACK INFORMATION

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

13 ST6 APPLICATION NOTES

IDENTIFICATION	DESCRIPTION
MOTOR CONTROL	
AN392	MICROCONTROLLER AND TRIACS ON THE 110/240V MAINS
AN414	CONTROLLING A BRUSH DC MOTOR WITH AN ST6265 MCU
AN416	SENSORLESS MOTOR DRIVE WITH THE ST62 MCU + TRIAC
AN422	IMPROVES UNIVERSAL MOTOR DRIVE
AN863	IMPROVED SENSORLESS CONTROL WITH THE ST62 MCU FOR UNIVERSAL MOTOR
BATTERY MANAGEMENT	
AN417	FROM NICD TO NIMH FAST BATTERY CHARGING
AN433	ULTRA FAST BATTERY CHARGER USING ST6210 MICROCONTROLLER
AN859	AN INTELLIGENT ONE HOUR MULTICHARGER FOR Li-Ion, NiMH and NiCd BATTERIES
HOME APPLIANCE	
AN674	MICROCONTROLLERS IN HOME APPLIANCES: A SOFT REVOLUTION
AN885	ST62 MICROCONTROLLERS DRIVE HOME APPLIANCE MOTOR TECHNOLOGY
GRAPHICAL DESIGN	
AN676	BATTERY CHARGER USING THE ST6-REALIZER
AN677	PAINLESS MICROCONTROLLER CODE BY GRAPHICAL APPLICATION DESCRIPTION
AN839	ANALOG MULTIPLE KEY DECODING USING THE ST6-REALIZER
AN840	CODED LOCK USING THE ST6-REALIZER
AN841	A CLOCK DESIGN USING THE ST6-REALIZER
AN842	7 SEGMENT DISPLAY DRIVE USING THE ST6-REALIZER
COST REDUCTION	
AN431	USING ST6 ANALOG INPUTS FOR MULTIPLE KEY DECODING
AN594	DIRECT SOFTWARE LCD DRIVE WITH ST621X AND ST626X
AN672	OPTIMIZING THE ST6 A/D CONVERTER ACCURACY
AN673	REDUCING CURRENT CONSUMPTION AT 32KHZ WITH ST62
DESIGN IMPROVEMENTS	
AN420	EXPANDING A/D RESOLUTION OF THE ST6 A/D CONVERTER
AN432	USING ST62XX I/O PORTS SAFELY
AN434	MOVEMENT DETECTOR CONCEPTS FOR NOISY ENVIRONMENTS
AN435	DESIGNING WITH MICROCONTROLLERS IN NOISY ENVIRONMENTS
AN669	SIMPLE RESET CIRCUITS FOR THE ST6
AN670	OSCILLATOR SELECTION FOR ST62
AN671	PREVENTION OF DATA CORRUPTION IN ST6 ON-CHIP EEPROM
AN911	ST6 MICRO IS EMC CHAMPION
AN975	UPGRADING FROM ST625X/6XB TO ST625X/6XC
AN1015	SOFTWARE TECHNIQUES FOR IMPROVING ST6 EMC PERFORMANCE
PERIPHERAL OPERATIONS	
AN590	PWM GENERATION WITH ST62 AUTO-RELOAD TIMER
AN591	INPUT CAPTURE WITH ST62 AUTO-RELOAD TIMER
AN592	PLL GENERATION USING THE ST62 AUTO-RELOAD TIMER
AN593	ST62 IN-CIRCUIT PROGRAMMING
AN678	LCD DRIVING WITH ST6240