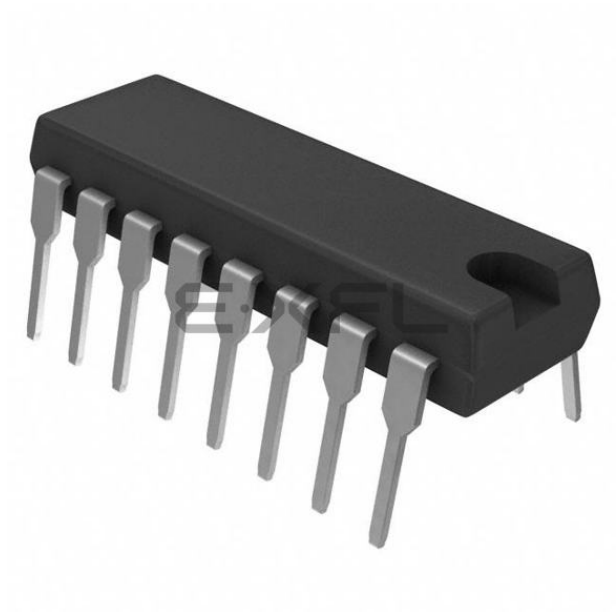

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	9
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t01cb6

MEMORY MAP (Cont'd)

3.1.2 Program Space

Program Space comprises the instructions to be executed, the data required for immediate addressing mode instructions, the reserved factory test area and the user vectors. Program Space is addressed via the 12-bit Program Counter register (PC register). Thus, the MCU is capable of addressing 4K bytes of memory directly.

3.1.3 Readout Protection

The Program Memory in in OTP, EPROM or ROM devices can be protected against external readout of memory by setting the Readout Protection bit in the option byte (Section 3.3 on page 15).

In the EPROM parts, Readout Protection option can be desactivated only by U.V. erasure that also results in the whole EPROM context being erased.

Note: Once the Readout Protection is activated, it is no longer possible, even for STMicroelectronics, to gain access to the OTP or ROM contents. Returned parts can therefore not be accepted if the Readout Protection bit is set.

3.1.4 Data Space

Data Space accommodates all the data necessary for processing the user program. This space comprises the RAM resource, the processor core and peripheral registers, as well as read-only data such as constants and look-up tables in OTP/EPROM.

3.1.4.1 Data ROM

All read-only data is physically stored in program memory, which also accommodates the Program Space. The program memory consequently contains the program code to be executed, as well as the constants and look-up tables required by the application.

The Data Space locations in which the different constants and look-up tables are addressed by the processor core may be thought of as a 64-byte window through which it is possible to access the read-only data stored in OTP/EPROM.

3.1.4.2 Data RAM

The data space includes the user RAM area, the accumulator (A), the indirect registers (X), (Y), the short direct registers (V), (W), the I/O port registers, the peripheral data and control registers, the interrupt option register and the Data ROM Window register (DRWR register).

3.1.5 Stack Space

Stack space consists of six 12-bit registers which are used to stack subroutine and interrupt return addresses, as well as the current program counter contents.

4 CENTRAL PROCESSING UNIT

4.1 INTRODUCTION

The CPU Core of ST6 devices is independent of the I/O or Memory configuration. As such, it may be thought of as an independent central processor communicating with on-chip I/O, Memory and Peripherals via internal address, data, and control buses.

4.2 MAIN FEATURES

- 40 basic instructions
- 9 main addressing modes
- Two 8-bit index registers
- Two 8-bit short direct registers
- Low power modes
- Maskable hardware interrupts
- 6-level hardware stack

4.3 CPU REGISTERS

The ST6 Family CPU core features six registers and three pairs of flags available to the programmer. These are described in the following paragraphs.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator can be addressed in Data Space as a RAM location at address FFh. Thus the ST6 can manipulate the accumulator just like any other register in Data Space.

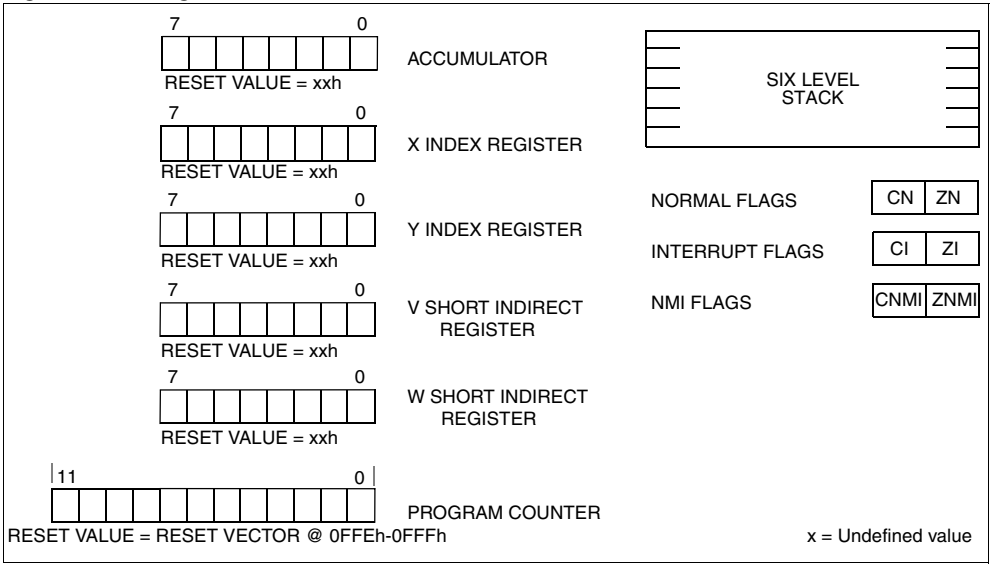
Index Registers (X, Y). These two registers are used in Indirect addressing mode as pointers to memory locations in Data Space. They can also be accessed in Direct, Short Direct, or Bit Direct addressing modes. They are mapped in Data Space at addresses 80h (X) and 81h (Y) and can be accessed like any other memory location.

Short Direct Registers (V, W). These two registers are used in Short Direct addressing mode. This means that the data stored in V or W can be accessed with a one-byte instruction (four CPU cycles). V and W can also be accessed using Direct and Bit Direct addressing modes. They are mapped in Data Space at addresses 82h (V) and 83h (W) and can be accessed like any other memory location.

Note: The X and Y registers can also be used as Short Direct registers in the same way as V and W.

Program Counter (PC). The program counter is a 12-bit register which contains the address of the next instruction to be executed by the core. This ROM location may be an opcode, an operand, or the address of an operand.

Figure 7. CPU Registers



CLOCK SYSTEM (Cont'd)

5.1.1 Main Oscillator

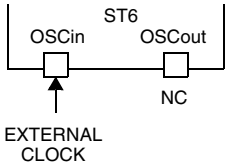
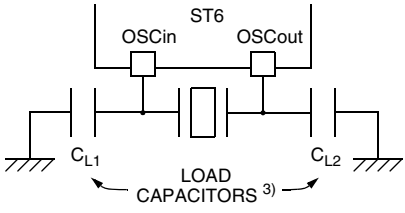
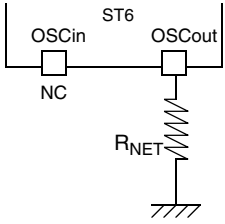
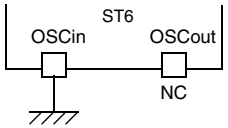
The oscillator configuration is specified by selecting the appropriate option in the option bytes (refer to the Option Bytes section of this document). When the CRYSTAL/RESONATOR option is selected, it must be used with a quartz crystal, a ceramic resonator or an external signal provided on the OSCin pin. When the RC NETWORK option is selected, the system clock is generated by an external resistor (the capacitor is implemented internally).

The main oscillator can be turned off (when the OSG ENABLED option is selected) by setting the OSCOFF bit of the ADC Control Register (not available on some devices). This will automatically start the Low Frequency Auxiliary Oscillator (LFAO).

The main oscillator can be turned off by resetting the OSCOFF bit of the A/D Converter Control Register or by resetting the MCU. When the main oscillator starts there is a delay made up of the oscillator start-up delay period plus the duration of the software instruction at a clock frequency f_{LFAO}.

Caution: It should be noted that when the RC network option is selected, the accuracy of the frequency is about 20% so it may not be suitable for some applications (For more details, please refer to the Electrical Characteristics Section).

Table 5. Oscillator Configurations

	Hardware Configuration
Crystal/Resonator Option 1)	External Clock 
Crystal/Resonator Option 1)	Crystal/Resonator Clock 2) 
RC Network Option 1)	RC Network 
OSG Enabled Option 1)	LFAO 

Notes:
1. To select the options shown in column 1 of the above table, refer to the Option Byte section.

2.This schematic are given for guidance only and are subject to the schematics given by the crystal or ceramic resonator manufacturer.
3. For more details, please refer to the Electrical Characteristics Section.

5.2 LOW VOLTAGE DETECTOR (LVD)

The on-chip Low Voltage Detector is enabled by setting a bit in the option bytes (refer to the Option Bytes section of this document).

The LVD allows the device to be used without any external RESET circuitry. In this case, the $\overline{\text{RESET}}$ pin should be left unconnected.

If the LVD is not used, an external circuit is mandatory to ensure correct Power On Reset operation, see figure in the Reset section. For more details, please refer to the application note AN669.

The LVD generates a static Reset when the supply voltage is below a reference value. This means that it secures the power-up as well as the power-down keeping the ST6 in reset.

The V_{IT-} reference value for a voltage drop is lower than the V_{IT+} reference value for power-on in order to avoid a parasitic reset when the MCU starts running and sinks current on the supply (hysteresis).

The LVD Reset circuitry generates a reset when V_{DD} is below:

– V_{IT+} when V_{DD} is rising

– V_{IT-} when V_{DD} is falling

The LVD function is illustrated in Figure 12.

If the LVD is enabled, the MCU can be in only one of two states:

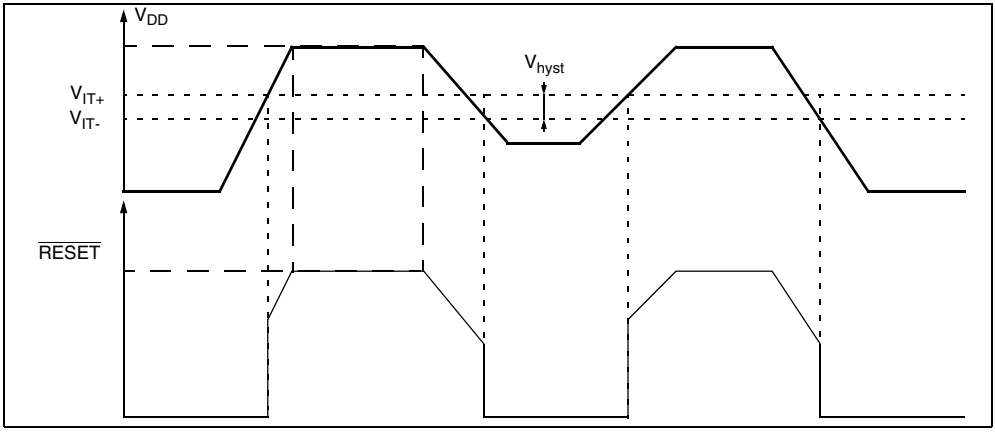
– Over the input threshold voltage, it is running under full software control

– Below the input threshold voltage, it is in static safe reset

In these conditions, secure operation is guaranteed without the need for external reset hardware.

During a Low Voltage Detector Reset, the $\overline{\text{RESET}}$ pin is held low, thus permitting the MCU to reset other devices.

Figure 12. Low Voltage Detector Reset



5.10 INTERRUPT HANDLING PROCEDURE

The interrupt procedure is very similar to a call procedure, in fact the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event, the user cannot know the context and the time at which it occurred. As a result, the user should save all Data space registers which may be used within the interrupt routines. The following list summarizes the interrupt procedure:

When an interrupt request occurs, the following actions are performed by the MCU automatically:

– The core switches from the normal flags to the interrupt flags (or the NMI flags).
– The PC contents are stored in the top level of the stack.
– The normal interrupt lines are inhibited (NMI still active).
– The internal latch (if any) is cleared.
– The associated interrupt vector is loaded in the PC.

When an interrupt request occurs, the following actions must be performed by the user software:

– User selected registers have to be saved within the interrupt service routine (normally on a software stack).
– The source of the interrupt must be determined by polling the interrupt flags (if more than one source is associated with the same vector).
– The RETI (RETurn from Interrupt) instruction must end the interrupt service routine.

After the RETI instruction is executed, the MCU returns to the main routine.

Caution: When a maskable interrupt occurs while the ST6 core is in NORMAL mode and during the execution of an “ldi IOR, 00h” instruction (disabling all maskable interrupts): if the interrupt request occurs during the first 3 cycles of the “ldi” instruction (which is a 4-cycle instruction) the core will switch to interrupt mode BUT the flags CN and ZN will NOT switch to the interrupt pair CI and ZI.

5.10.1 Interrupt Response Time

This is defined as the time between the moment when the Program Counter is loaded with the interrupt vector and when the program has jump to the interrupt subroutine and is ready to execute the code. It depends on when the interrupt occurs while the core is processing an instruction.

Figure 18. Interrupt Processing Flow Chart

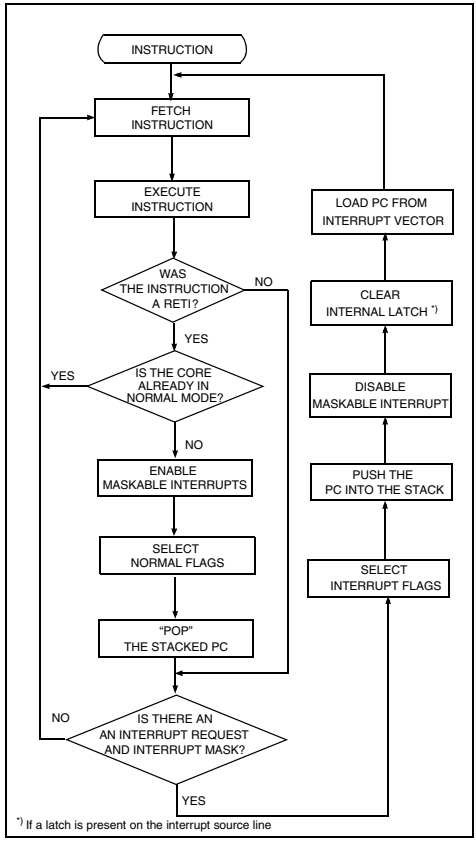


Table 6. Interrupt Response Time

Minimum	6 CPU cycles
Maximum	11 CPU cycles

One CPU cycle is 13 external clock cycles thus 11 CPU cycles = 11 x (13 /8M) = 17.875 µs with an 8 MHz external quartz.

I/O PORTS (Cont'd)

Figure 23. I/O Port Block Diagram

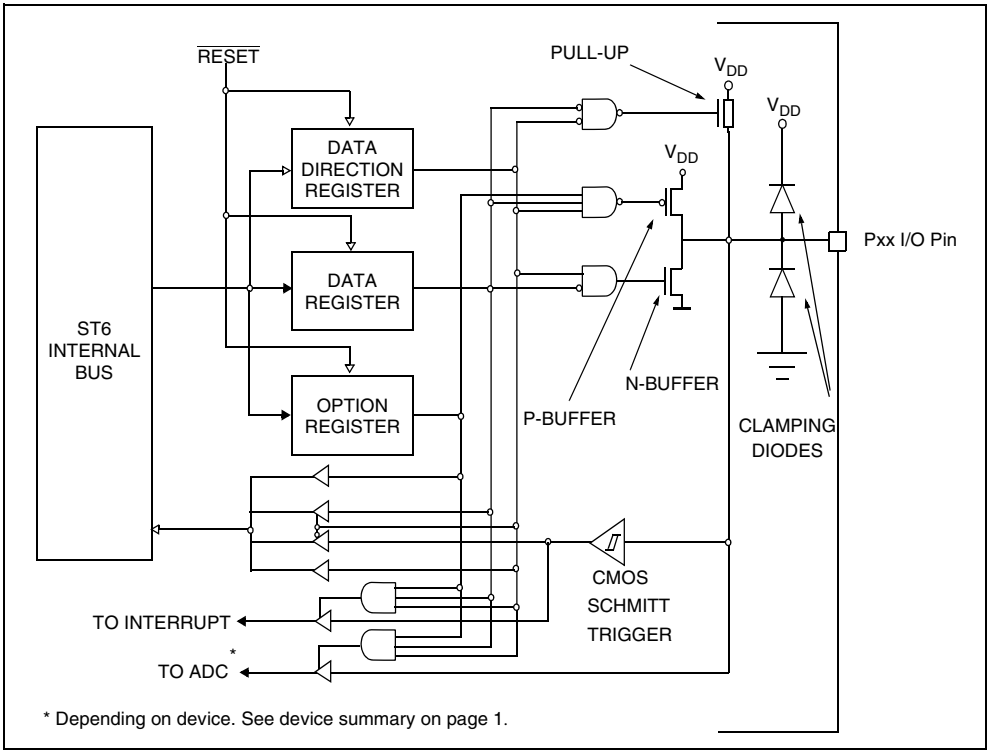


Table 8. I/O Port Configurations

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up and with interrupt
0	1	1	Input	Analog input (when available)
1	0	x	Output	Open-drain output (20mA sink when available)
1	1	x	Output	Push-pull output (20mA sink when available)

Note: x = Don't care

I/O PORTS (Cont'd)

7.2.5 Instructions NOT to be used to access Port Data registers (SET, RES, INC and DEC)

DO NOT USE READ-MODIFY-WRITE INSTRUCTIONS (SET, RES, INC and DEC) ON PORT DATA REGISTERS IF ANY PIN OF THE PORT IS CONFIGURED IN INPUT MODE.

These instructions make an implicit read and write back of the entire register. In port input mode, however, the data register reads from the input pins directly, and not from the data register latches. Since data register information in input mode is used to set the characteristics of the input pin (interrupt, pull-up, analog input), these may be unintentionally reprogrammed depending on the state of the input pins.

As a general rule, it is better to only use single bit instructions on data registers when the whole (8-bit) port is in output mode. In the case of inputs or of mixed inputs and outputs, it is advisable to keep a copy of the data register in RAM. Single bit instructions may then be used on the RAM copy, after which the whole copy register can be written to the port data register:

```
SET bit, datacopy
LD a, datacopy
LD DRA, a
```

7.2.6 Recommendations

1. Safe I/O State Switching Sequence

Switching the I/O ports from one state to another should be done in a sequence which ensures that no unwanted side effects can occur. The recommended safe transitions are illustrated in Figure 24 The Interrupt Pull-up to Input Analog transition (and vice-vesra) is potentially risky and should be avoided when changing the I/O operating mode.

2. Handling Unused Port Bits

On ports that have less than 8 external pins connected:

– Leave the unbonded pins in reset state and do not change their configuration.

– Do not use instructions that act on a whole port register (INC, DEC, or read operations). Unavailable bits must be masked by software (AND instruction). Thus, when a read operation performed on an incomplete port is followed by a comparison, use a mask.

3. High Impedance Input

On any CMOS device, it is not recommended to connect high impedance on input pins. The choice of these impedance has to be done with respect to the maximum leakage current defined in the datasheet. The risk is to be close or out of specification on the input levels applied to the device.

7.3 LOW POWER MODES

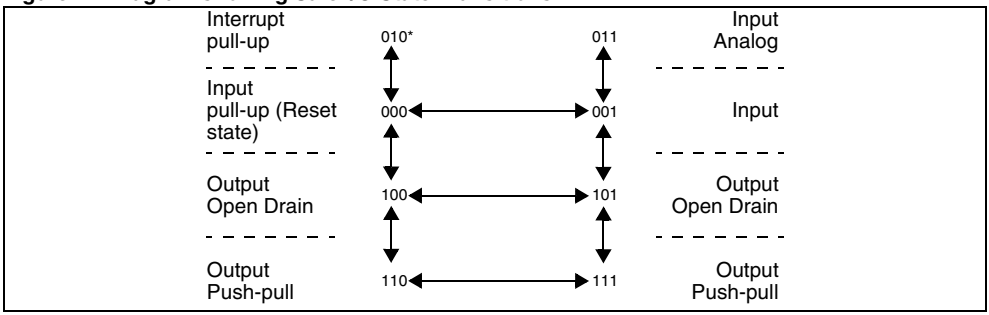
The WAIT and STOP instructions allow the ST62xx to be used in situations where low power consumption is needed. The lowest power consumption is achieved by configuring I/Os in output push-pull low mode.

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
STOP	No effect on I/O ports. External interrupts cause the device to exit from STOP mode.

7.4 INTERRUPTS

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR, DR and OR registers (see Table 8) and the GEN-bit in the IOR register is set.

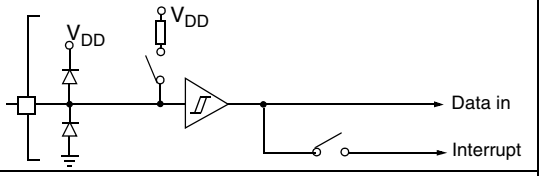
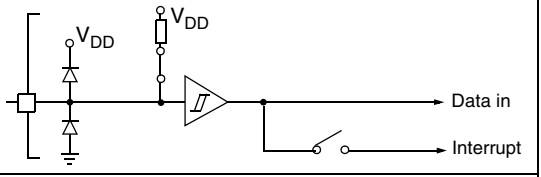
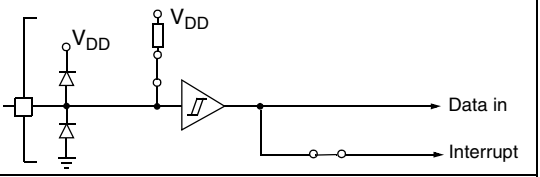
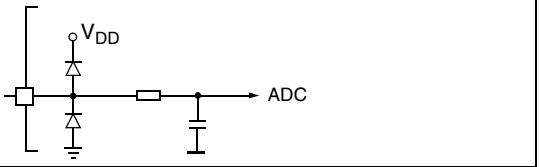
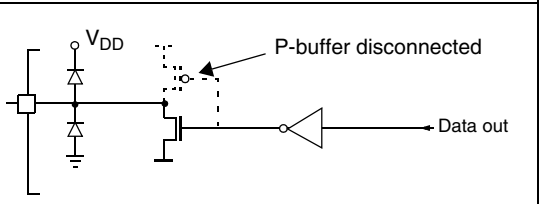
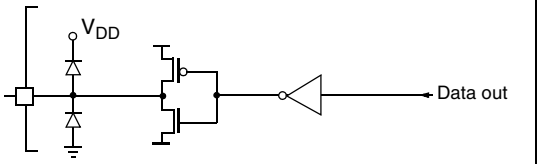
Figure 24. Diagram showing Safe I/O State Transitions



Note *. xxx = DDR, OR, DR Bits respectively

I/O PORTS (Cont'd)

Table 9. I/O Port Option Selections

	MODE	DDRx	ORx	DRx	AVAILABLE ON(1)	SCHEMATIC
Digital Input	Input	0	0	1	PA1-PA3 PB0, PB1, PB3, PB5-PB7	
	Reset state Input with pull up	0	0	0	PA1-PA3 PB0, PB1, PB3, PB5-PB7	
	Input with pull up with interrupt	0	1	0	PA1-PA3 PB0, PB1, PB3, PB5-PB7	
Analog Input	Analog Input	0	1	1	PB3, PB5-PB7 (Except on ST6203C)	
Digital output	Open drain output (5mA)	1	0	0/1	PB0, PB1, PB3, PB5-PB7	
	Open drain output (20 mA)	1	0	0/1	PA1-PA3	
	Push-pull output (5mA)	1	1	0/1	PB0, PB1, PB3, PB5-PB7	
	Push-pull output (20 mA)	1	1	0/1	PA1-PA3	

Note 1. Provided the correct configuration has been selected (see Table 8).

WATCHDOG TIMER (Cont'd)

8.1.3 Functional Description

The watchdog activation is selected through an option in the option bytes:

– **HARDWARE** Watchdog option

After reset, the watchdog is permanently active, the C bit in the WDGR is forced high and the user can not change it. However, this bit can be read equally as 0 or 1.

– **SOFTWARE** Watchdog option

After reset, the watchdog is deactivated. The function is activated by setting C bit in the WDGR register. Once activated, it cannot be deactivated. The counter value stored in the WDGR register (bits SR:T0), is decremented every 3072 clock cycles. The length of the timeout period can be programmed by the user in 64 steps of 3072 clock cycles.

If the watchdog is activated (by setting the C bit) and when the SR bit is cleared, the watchdog initiates a reset cycle pulling the reset pin low for typically 500ns.

The application program must write in the WDGR register at regular intervals during normal operation to prevent an MCU reset. The value to be stored in the WDGR register must be between FEh and 02h (see Table 11). To run the watchdog function the following conditions must be true:

– The C bit is set (watchdog activated)

– The SR bit is set to prevent generating an immediate reset

– The T[5:0] bits contain the number of decrements which represent the time delay before the watchdog produces a reset.

Table 11. Watchdog Timing (f_{OSC} = 8 MHz)

	WDGR Register initial value	WDG timeout period (ms)
Max.	FEh	24.576
Min.	02h	0.384

8.1.3.1 Software Reset

The SR bit can be used to generate a software reset by clearing the SR bit while the C bit is set.

8.1.4 Recommendations

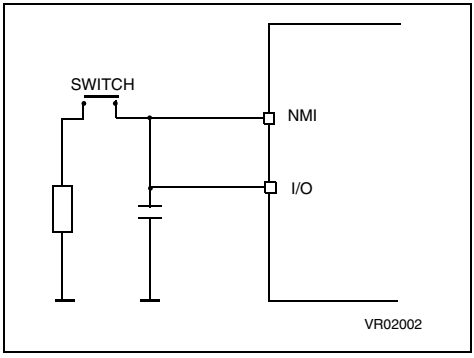
1. The Watchdog plays an important supporting role in the high noise immunity of ST62xx devices, and should be used wherever possible. Watchdog related options should be selected on the basis of a trade-off between application security and STOP mode availability (refer to the description of the WDACT and EXTCNTL bits on the Option Bytes).

When STOP mode is not required, hardware activation without EXTERNAL STOP MODE CONTROL should be preferred, as it provides maximum security, especially during power-on.

When STOP mode is required, hardware activation and EXTERNAL STOP MODE CONTROL should be chosen. NMI should be high by default, to allow STOP mode to be entered when the MCU is idle.

The NMI pin can be connected to an I/O line (see Figure 26) to allow its state to be controlled by software. The I/O line can then be used to keep NMI low while Watchdog protection is required, or to avoid noise or key bounce. When no more processing is required, the I/O line is released and the device placed in STOP mode for lowest power consumption.

Figure 26. A typical circuit making use of the EXERNAL STOP MODE CONTROL feature



2. When software activation is selected (WDACT bit in Option byte) and the Watchdog is not activated, the downcounter may be used as a simple 7-bit timer (remember that the bits are in reverse order).

The software activation option should be chosen only when the Watchdog counter is to be used as a timer. To ensure the Watchdog has not been unexpectedly activated, the following instructions should be executed:

```
jrr 0, WDGR, #+3 ; If C=0,jump to next
ldi WDGR, 0FDH   ; SR=0 -> reset

next :
```

WATCHDOG TIMER (Cont'd)

8.1.7 Register Description

WATCHDOG REGISTER (WDGR)

Address: 0D8h - Read/Write

Reset Value: 1111 1110 (FEh)

7							0
T0	T1	T2	T3	T4	T5	SR	C

Bits 7:2 = **T[5:0]** *Downcounter bits*
Caution: These bits are reversed and shifted with respect to the physical counter: bit-7 (T0) is the LSB of the Watchdog downcounter and bit-2 (T5) is the MSB.

Bit 1 = **SR**: *Software Reset bit*
Software can generate a reset by clearing this bit while the C bit is set. When C = 0 (Watchdog deactivated) the SR bit is the MSB of the 7-bit timer.
0: Generate (write)

1: No software reset generated, MSB of 7-bit timer

Bit 0 = **C** *Watchdog Control bit*.
If the hardware option is selected (WDACT bit in Option byte), this bit is forced high and cannot be changed by the user (the Watchdog is always active). When the software option is selected (WDACT bit in Option byte), the Watchdog function is activated by setting the C bit, and cannot then be deactivated (except by resetting the MCU).

When C is kept cleared the counter can be used as a 7-bit timer.
0: Watchdog deactivated
1: Watchdog activated

8.2 8-BIT TIMER

8.2.1 Introduction

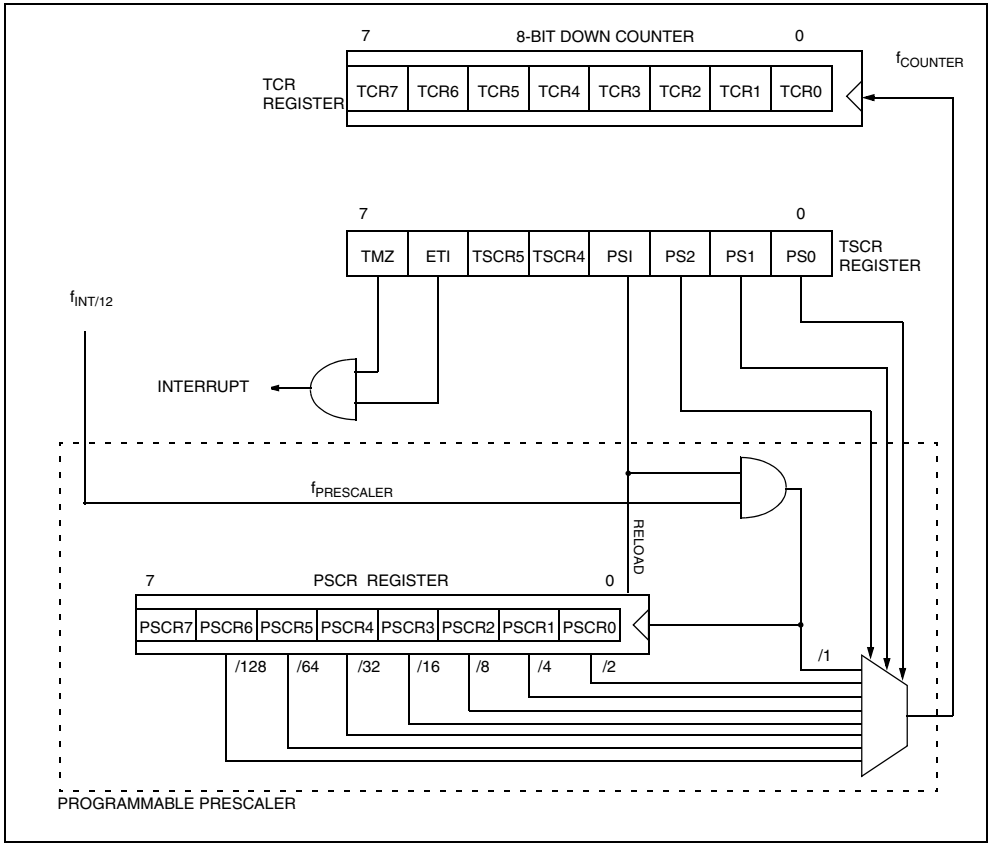
The 8-Bit Timer on-chip peripheral is a free running downcounter based on an 8-bit downcounter with a 7-bit programmable prescaler, giving a maximum count of 2^{15}.

8.2.2 Main Features

- Time-out downcounting mode with up to 15-bit accuracy
- Interrupt capability on counter underflow

The timer can be used in WAIT mode to wake up the MCU.

Figure 27. Timer Block Diagram



8.3 A/D CONVERTER (ADC)

8.3.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 8-bit, successive approximation converter. This peripheral has multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from different sources.

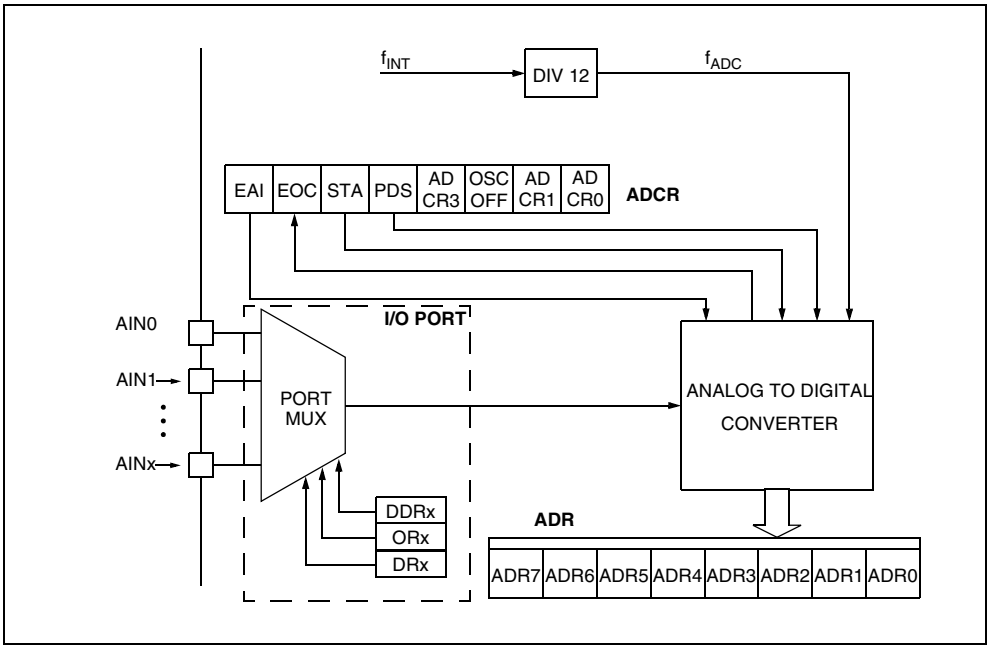
The result of the conversion is stored in a 8-bit Data Register. The A/D converter is controlled through a Control Register.

8.3.2 Main Features

- 8-bit conversion
- Multiplexed analog input channels
- Linear successive approximation
- Data register (DR) which contains the results
- End of Conversion flag
- On/Off bit (to reduce consumption)
- Typical conversion time 70 µs (with an 8 MHz crystal)

The block diagram is shown in Figure 28.

Figure 28. ADC Block Diagram



Note: ADC not present on some devices. See device summary on page 1.

A/D CONVERTER (Cont'd)

8.3.5 Low Power Modes

Mode	Description
WAIT	No effect on A/D Converter. ADC interrupts cause the device to exit from Wait mode.
STOP	A/D Converter disabled.

Note: The A/D converter may be disabled by clearing the PDS bit. This feature allows reduced power consumption when no conversion is needed.

8.3.6 Interrupts

Interrupt Event	Event Flag	Enable Bit	Exit from Wait	Exit from Stop
End of Conversion	EOC	EAI	Yes	No

Note: The EOC bit is cleared only when a new conversion is started (it cannot be cleared by writing 0). To avoid generating further EOC interrupt, the EAI bit has to be cleared within the ADC interrupt subroutine.

8.3.7 Register Description

A/D CONVERTER CONTROL REGISTER (ADCR)

Address: 0D1h - Read/Write (Bit 6 Read Only, Bit 5 Write Only)

Reset value: 0100 0000 (40h)

7							0
EAI	EOC	STA	PDS	ADCR 3	OSC OFF	ADCR 1	ADCR 0

Bit 7 = **EAI** *Enable A/D Interrupt.*
0: ADC interrupt disabled
1: ADC interrupt enabled

Bit 6 = **EOC** *End of conversion. Read Only*
When a conversion has been completed, this bit is set by hardware and an interrupt request is generated if the EAI bit is set. The EOC bit is automatically cleared when the STA bit is set. Data in the data conversion register are valid only when this bit is set to "1".
0: Conversion is not complete
1: Conversion can be read from the ADR register

Bit 5 = **STA***: Start of Conversion. Write Only*.
0: No effect
1: Start conversion

Note: Setting this bit automatically clears the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

Bit 4 = **PDS** *Power Down Selection.*

0: A/D converter is switched off
1: A/D converter is switched on

Bit 3 = **ADCR3 Reserved**, must be cleared.

Bit 2 = **OSCOFF** *Main Oscillator off.*

0: Main Oscillator enabled
1: Main Oscillator disabled

Note: This bit does not apply to the ADC peripheral but to the main clock system. Refer to the Clock System section.

Bits 1:0 = **ADCR[1:0] Reserved**, must be cleared.

A/D CONVERTER DATA REGISTER (ADR)

Address: 0D0h - Read only

Reset value: xxxx xxxx (xxh)

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

Bits 7:0 = **ADR[7:0]***: 8 Bit A/D Conversion Result.*

Table 14. ADC Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0D0h	**ADR** Reset Value	ADR7 0	ADR6 0	ADR5 0	ADR4 0	ADR3 0	ADR2 0	ADR1 0	ADR0 0
0D1h	**ADCR** Reset Value	EAI 0	EOC 1	STA 0	PDS 0	ADCR3 0	OSCOFF 0	ADCR1 0	ADCR0 0

INSTRUCTION SET (Cont'd)

Arithmetic and Logic. These instructions are used to perform arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while, depending on the addressing mode, the other can be either a data space memory location or an immediate value. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 16. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	Δ
AND A, (Y)	Indirect	1	4	Δ	Δ
AND A, rr	Direct	2	4	Δ	Δ
ANDI A, #N	Immediate	2	4	Δ	Δ
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y Index Registers
V, W Short Direct Registers
Δ Affected
Immediate data (stored in ROM memory)
* Not Affected
rr Data space register

CLOCK AND TIMING CHARACTERISTICS (Cont'd)

10.5.4 RC Oscillator

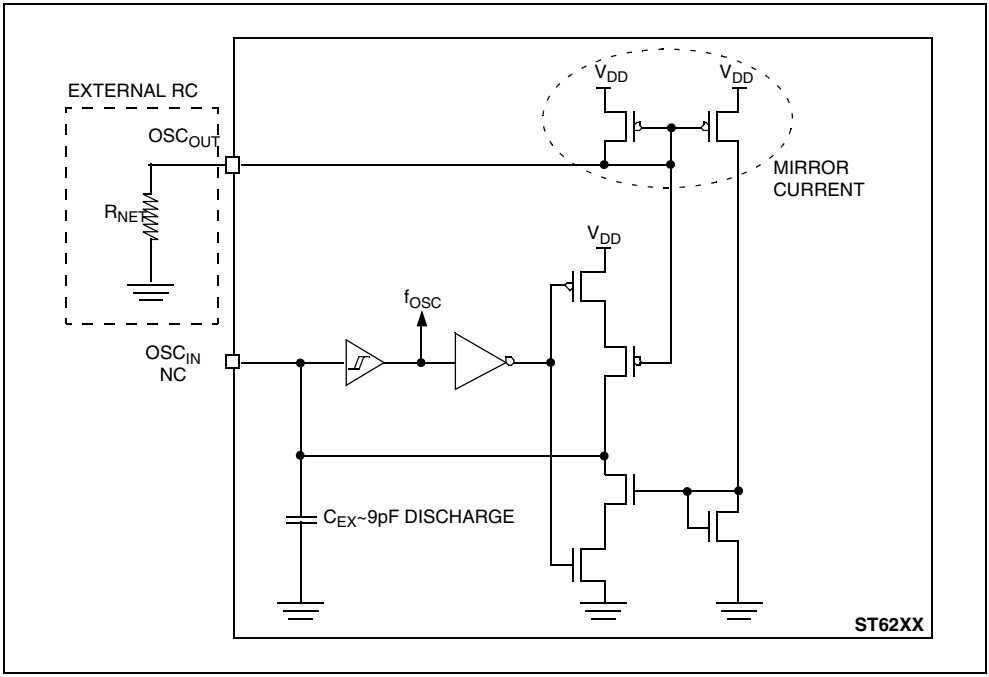
The ST6 internal clock can be supplied with an external RC oscillator. Depending on the R_{NET} value, the accuracy of the frequency is about 20%, so it may not be suitable for some applications.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{OSC}	RC oscillator frequency [1]	4.5V≤V_{DD}≤6.0V	R_{NET}=22 kΩ	7.2	8.6	10	MHz
			R_{NET}=47 kΩ	5.1	5.7	6.5	
			R_{NET}=100 kΩ	3.2	3.4	3.8	
			R_{NET}=220 kΩ	1.8	1.9	2	
			R_{NET}=470 kΩ	0.9	0.95	1.1	
		3V≤V_{DD}≤3.6V	R_{NET}=22 kΩ	3.7	4.3	4.9	
			R_{NET}=47 kΩ	2.8	3	3.3	
			R_{NET}=100 kΩ	1.8	1.9	2	
			R_{NET}=220 kΩ	1	1.1	1.2	
			R_{NET}=470 kΩ	0.5	0.55	0.6	
R_{NET}	RC Oscillator external resistor [2]		see Figure 46 & Figure 47	22		870	kΩ

Notes:

1. Data based on characterization results, not tested in production. These measurements were done with the OSCin pin unconnected (only soldered on the PCB).
2. R_{NET} must have a positive temperature coefficient (ppm/°C), carbon resistors should therefore not be used.

Figure 45. Typical Application with RC Oscillator



10.6 MEMORY CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

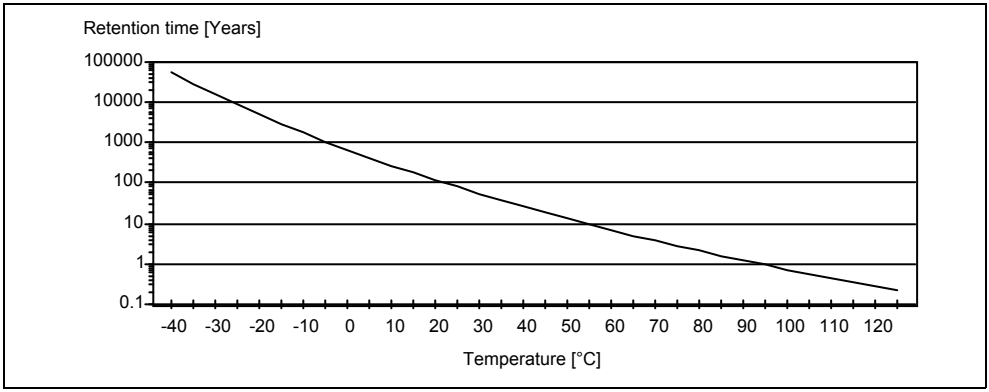
10.6.1 RAM and Hardware Registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention[1)]		0.7			V

10.6.2 EPROM Program Memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ret}	Data retention [2)]	T_A=+55°C [3)]	10			years

Figure 49. EPROM Retention Time vs. Temperature



Notes:

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in STOP mode or under RESET) or in hardware registers (only in STOP mode). Guaranteed by construction, not tested in production.
2. Data based on reliability test results and monitored in production. For OTP devices, data retention and programmability must be guaranteed by a screening procedure. Refer to Application Note AN886.
3. The data retention time increases when the T_A decreases, see Figure 49.

I/O PORT PIN CHARACTERISTICS (Cont'd)

10.8.2 Output Driving Current

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL} 1)	Output low level voltage for a standard I/O pin (see Figure 57 and Figure 60)	V_{DD}=5V	I_{IO}=+10µA, $T_A \leq 125°C$		0.1	V
			I_{IO}=+3mA, $T_A \leq 125°C$		0.8	
			I_{IO}=+5mA, $T_A \leq 85°C$		0.8	
			I_{IO}=+10mA, $T_A \leq 85°C$		1.2	
	Output low level voltage for a high sink I/O pin (see Figure 58 and Figure 61)		I_{IO}=+10µA, $T_A \leq 125°C$		0.1	
			I_{IO}=+7mA, $T_A \leq 125°C$		0.8	
			I_{IO}=+10mA, $T_A \leq 85°C$		0.8	
			I_{IO}=+15mA, $T_A \leq 125°C$		1.3	
			I_{IO}=+20mA, $T_A \leq 85°C$		1.3	
			I_{IO}=+30mA, $T_A \leq 85°C$		2	
V_{OH} 2)	Output high level voltage for an I/O pin (see Figure 59 and Figure 62)		I_{IO}=-10µA, $T_A \leq 125°C$	V_{DD}-0.1		
			I_{IO}=-3mA, $T_A \leq 125°C$	V_{DD}-1.5		
			I_{IO}=-5mA, $T_A \leq 85°C$	V_{DD}-1.5		

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 10.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current source must always respect the absolute maximum rating specified in Section 10.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}. True open drain I/O pins does not have V_{OH}.

Figure 57. Typical V_{OL} at V_{DD} = 5V (standard)

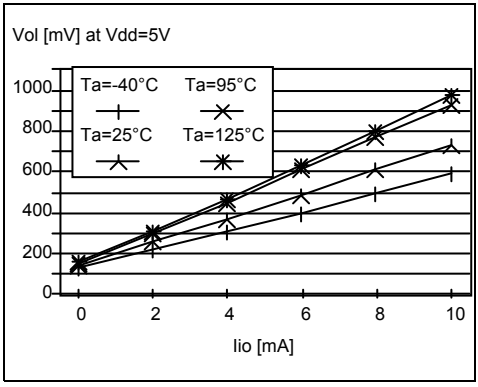
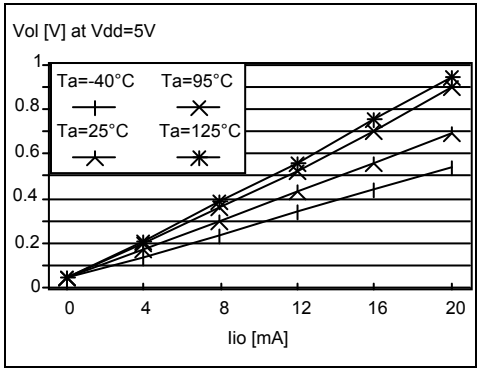


Figure 58. Typical V_{OL} at V_{DD} = 5V (high-sink)



11.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient) DIP16 SO16 SSOP16	 90 90 125	°C/W
P_D	Power dissipation [1]	500	mW
T_{Jmax}	Maximum junction temperature [2]	150	°C

Notes:

1. The power dissipation is obtained from the formula $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD}xV_{DD}$) and P_{PORT} is the port power dissipation determined by the user.
2. The average chip-junction temperature can be obtained from the formula $T_J = T_A + P_D$ x RthJA.

11.6 TRANSFER OF CUSTOMER CODE

Customer code is made up of the ROM contents and the list of the selected FASTROM options. The ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected options are communicated to STMicroelectronics using the correctly filled OPTION LIST appended. See page 94.

The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.

Listing Generation and Verification. When STMicroelectronics receives the user's ROM contents, a computer listing is generated from it. This listing refers exactly to the ROM contents and options which will be used to produce the specified MCU. The listing is then returned to the customer who must thoroughly check, complete, sign and return it to STMicroelectronics. The signed listing forms a part of the contractual agreement for the production of the specific customer MCU.

11.6.1 FASTROM version

The ST62P00C, P01C and P03C are the **F**actory **A**dvanced **S**ervice **T**echnique ROM (FASTROM) versions of ST62T00C, T01 and T03C OTP devices.

They offer the same functionality as OTP devices, but they do not have to be programmed by the customer. The customer code must be sent to STMicroelectronics in the same way as for ROM devices. The FASTROM option list has the same options as defined in the programmable option byte of the OTP version. It also offers an identifier option. If this option is enabled, each FASTROM device is programmed with a unique 5-byte number which is mapped at addresses 0F9Bh-0F9Fh. The user must therefore leave these bytes blanked.

The identification number is structured as follows:

0F9Bh	T0
0F9Ch	T1
0F9Dh	T2
0F9Eh	T3
0F9Fh	Test ID

with T0, T1, T2, T3 = time in seconds since 01/01/1970 and Test ID = Tester Identifier.

DEVELOPMENT TOOLS (Cont'd)

STMicroelectronics Tools

Four types of development tool are offered by ST, all of them connect to a PC via a parallel or serial port: see Table 25 and Table 26 for more details.

Table 25. STMicroelectronics Tool Features

	Emulation Type	Programming Capability	Software Included
ST6 Starter Kit	Device simulation (limited emulation as interrupts are not supported)	Yes (DIP packages only)	MCU CD ROM with: – Rkit-ST6 from Raisonance – ST6 Assembly toolchain – WGDB6 powerful Source Level Debugger for Win 3.1, Win 95 and NT – Various software demo versions. – Windows Programming Tools for Win 3.1, Win 95 and NT
ST6 HDS2 Emulator	In-circuit powerful emulation features including trace/ logic analyzer	No	
ST6 EPROM Programmer Board	No	Yes (All packages except SSOP)	

Table 26. Dedicated STMicroelectronics Development Tools

Supported Products	ST6 Starter Kit	ST6 HDS2 Emulator	ST6 Programming Board
ST6200C, 001C and 003C	ST622XC-KIT	Complete: ST62GP-EMU2 Dedication board: ST62GP-DBE	ST62E2XC-EPB