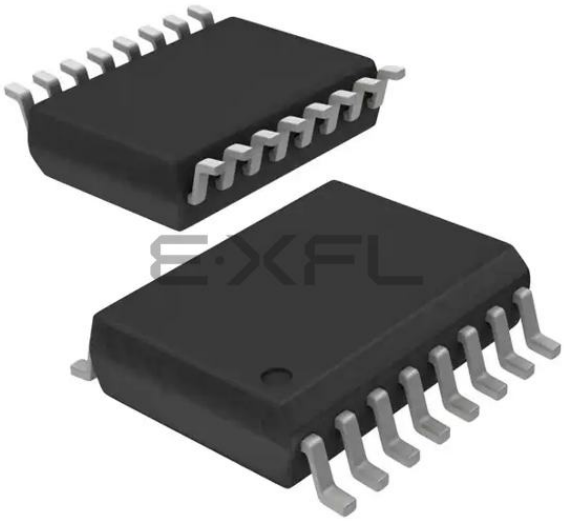

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What is "Embedded - Microcontrollers"?

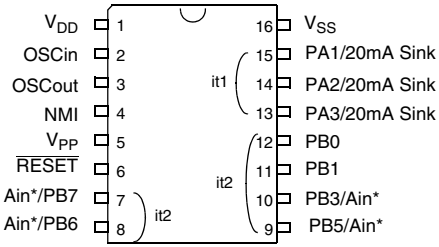
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	9
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t01cm6-tr

2 PIN DESCRIPTION

Figure 2. 16-Pin Package Pinout



itX associated interrupt vector
* Depending on device. Please refer to I/O Port section.

Table 1. Device Pin Description

Pin n°	Pin Name	Type	Main Function (after Reset)	Alternate Function
1	V_{DD}	S	Main power supply	
2	OSCin	I	External clock input or resonator oscillator inverter input	
3	OSCout	O	Resonator oscillator inverter output or resistor input for RC oscillator	
4	NMI	I	Non maskable interrupt (falling edge sensitive)	
5	V_{PP}		Must be held at Vss for normal operation, if a 12.5V level is applied to the pin during the reset phase, the device enters EPROM programming mode.	
6	$\overline{RESET}$	I/O	Top priority non maskable interrupt (active low)	
7	PB7/Ain*	I/O	Pin B7 (IPU)	Analog input
8	PB6/Ain*	I/O	Pin B6 (IPU)	Analog input
9	PB5/Ain*	I/O	Pin B5 (IPU)	Analog input
10	PB3/Ain*	I/O	Pin B3 (IPU)	Analog input
11	PB1	I/O	Pin B1 (IPU)	
12	PB0	I/O	Pin B0 (IPU)	
13	PA3/ 20mA Sink	I/O	Pin A3 (IPU)	
14	PA2/ 20mA Sink	I/O	Pin A2 (IPU)	
15	PA1/ 20mA Sink	I/O	Pin A1 (IPU)	
16	V_{SS}	S	Ground	

Legend / Abbreviations for Table 1**:**

* Depending on device. Please refer to I/O Port section.

I = input, O = output, S = supply, IPU = input pull-up

The input with pull-up configuration (reset state) is valid as long as the user software does not change it. Refer to Section 7 "I/O PORTS" on page 36 for more details on the software configuration of the I/O ports.

3 MEMORY MAPS, PROGRAMMING MODES AND OPTION BYTES

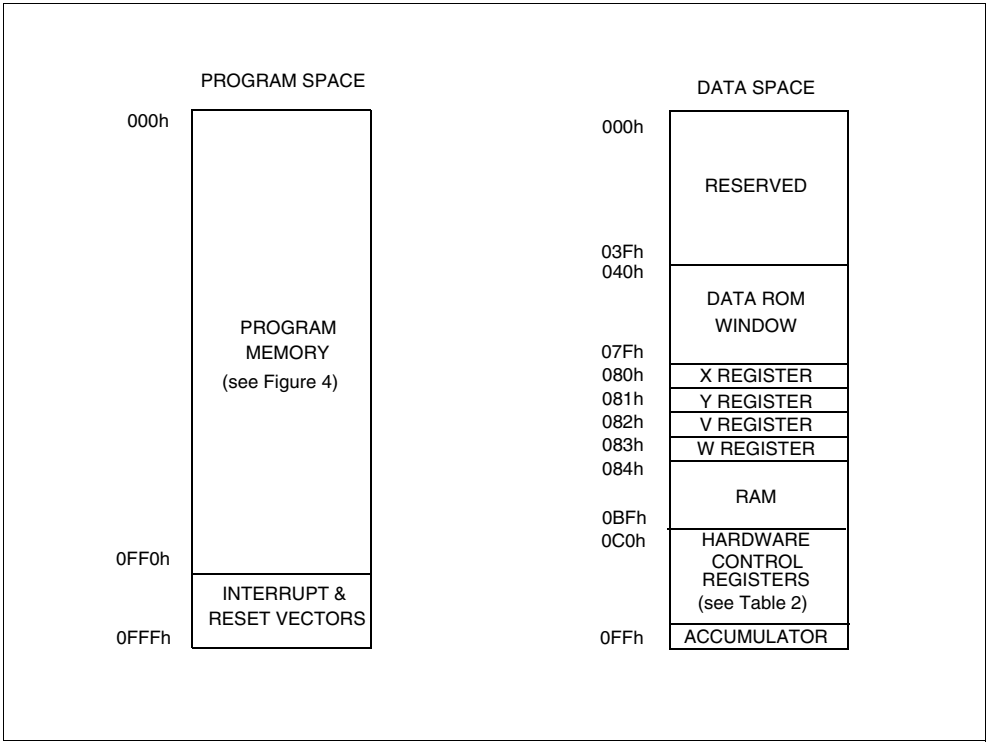
3.1 MEMORY AND REGISTER MAPS

3.1.1 Introduction

The MCU operates in three separate memory spaces: Program space, Data space, and Stack space. Operation in these three memory spaces is described in the following paragraphs.

Briefly, Program space contains user program code in OTP and user vectors; Data space contains user data in RAM and in OTP, and Stack space accommodates six levels of stack for subroutine and interrupt service routine nesting.

Figure 3. Memory Addressing Diagram



RESET (Cont'd)

5.3.4 Watchdog Reset

The MCU provides a Watchdog timer function in order to be able to recover from software hang-ups. If the Watchdog register is not refreshed before an end-of-count condition is reached, a Watchdog reset is generated.

After a Watchdog reset, the MCU restarts in the same way as if a Reset was generated by the $\overline{\text{RESET}}$ pin.

Note: When a watchdog reset occurs, the $\overline{\text{RESET}}$ pin is tied low for very short time period, to flag the reset phase. This time is not long enough to reset external circuits.

For more details refer to the Watchdog Timer chapter.

5.3.5 LVD Reset

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-On RESET
- Voltage Drop RESET

During an LVD reset, the $\overline{\text{RESET}}$ pin is pulled low when $V_{DD}<V_{IT+}$ (rising edge) or $V_{DD}<V_{IT-}$ (falling edge).

For more details, refer to the LVD chapter.

Caution: Do not externally connect directly the $\overline{\text{RESET}}$ pin to V_{DD}, this may cause damage to the component in case of internal RESET (Watchdog or LVD).

Figure 15. Simple External Reset Circuitry

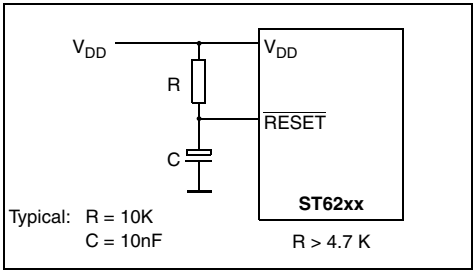
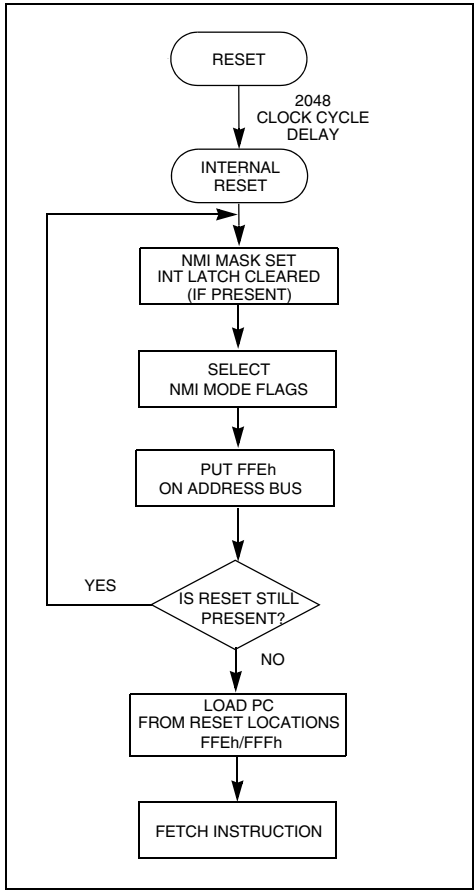


Figure 16. Reset Processing



5.10 INTERRUPT HANDLING PROCEDURE

The interrupt procedure is very similar to a call procedure, in fact the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event, the user cannot know the context and the time at which it occurred. As a result, the user should save all Data space registers which may be used within the interrupt routines. The following list summarizes the interrupt procedure:

When an interrupt request occurs, the following actions are performed by the MCU automatically:

– The core switches from the normal flags to the interrupt flags (or the NMI flags).
– The PC contents are stored in the top level of the stack.
– The normal interrupt lines are inhibited (NMI still active).
– The internal latch (if any) is cleared.
– The associated interrupt vector is loaded in the PC.

When an interrupt request occurs, the following actions must be performed by the user software:

– User selected registers have to be saved within the interrupt service routine (normally on a software stack).
– The source of the interrupt must be determined by polling the interrupt flags (if more than one source is associated with the same vector).
– The RETI (RETurn from Interrupt) instruction must end the interrupt service routine.

After the RETI instruction is executed, the MCU returns to the main routine.

Caution: When a maskable interrupt occurs while the ST6 core is in NORMAL mode and during the execution of an “ldi IOR, 00h” instruction (disabling all maskable interrupts): if the interrupt request occurs during the first 3 cycles of the “ldi” instruction (which is a 4-cycle instruction) the core will switch to interrupt mode BUT the flags CN and ZN will NOT switch to the interrupt pair CI and ZI.

5.10.1 Interrupt Response Time

This is defined as the time between the moment when the Program Counter is loaded with the interrupt vector and when the program has jump to the interrupt subroutine and is ready to execute the code. It depends on when the interrupt occurs while the core is processing an instruction.

Figure 18. Interrupt Processing Flow Chart

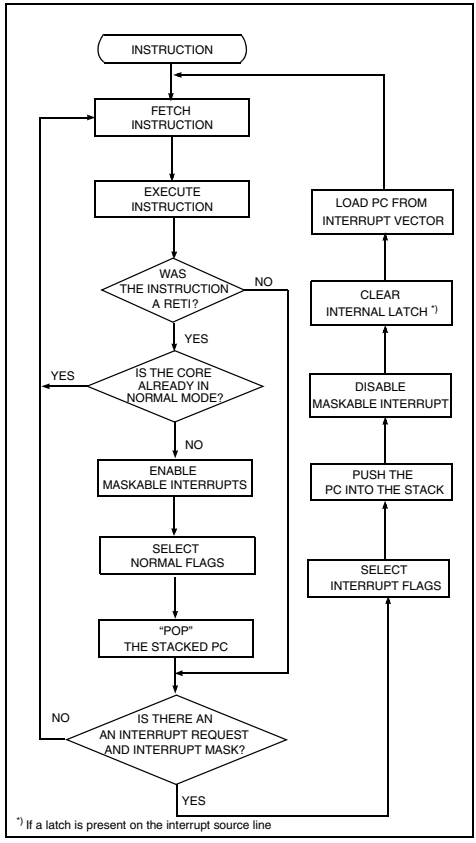


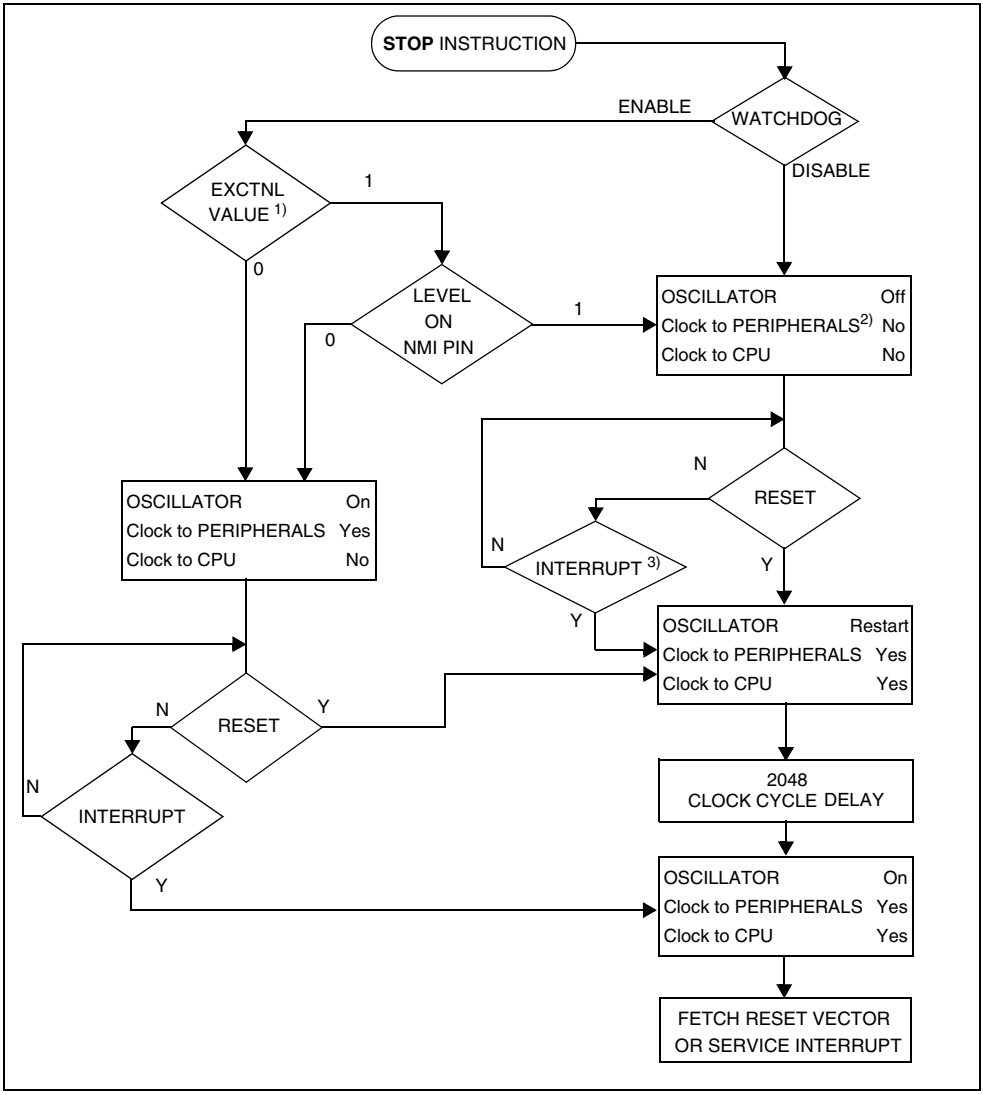
Table 6. Interrupt Response Time

Minimum	6 CPU cycles
Maximum	11 CPU cycles

One CPU cycle is 13 external clock cycles thus 11 CPU cycles = 11 x (13 /8M) = 17.875 µs with an 8 MHz external quartz.

STOP MODE (Cont'd)

Figure 22. STOP Mode Flowchart



Notes:

1. EXCTNL is an option bit. See option byte section for more details.

2. Peripheral clocked with an external clock source can still be active.

3. Only some specific interrupts can exit the MCU from STOP mode (such as external interrupt). Refer to the Interrupt Mapping table for more details.

6.4 NOTES RELATED TO WAIT AND STOP MODES

6.4.1 Exit from Wait and Stop Modes

6.4.1.1 NMI Interrupt

It should be noted that when the GEN bit in the IOR register is low (interrupts disabled), the NMI interrupt is active but cannot cause a wake up from STOP/WAIT modes.

6.4.1.2 Restart Sequence

When the MCU exits from WAIT or STOP mode, it should be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) prior to entering WAIT or STOP mode, as well as on the interrupt type.

Normal Mode. If the MCU was in the main routine when the WAIT or STOP instruction was executed, exit from Stop or Wait mode will occur as soon as an interrupt occurs; the related interrupt routine is executed and, on completion, the instruction which follows the STOP or WAIT instruction is then executed, providing no other interrupts are pending.

Non Maskable Interrupt Mode. If the STOP or WAIT instruction has been executed during execution of the non-maskable interrupt routine, the MCU exits from Stop or Wait mode as soon as an interrupt occurs: the instruction which follows the STOP or WAIT instruction is executed, and the MCU remains in non-maskable interrupt mode, even if another interrupt has been generated.

Normal Interrupt Mode. If the MCU was in interrupt mode before the STOP or WAIT instruction was executed, it exits from STOP or WAIT mode as soon as an interrupt occurs. Nevertheless, two cases must be considered:

– If the interrupt is a normal one, the interrupt routine in which the WAIT or STOP mode was entered will be completed, starting with the execution of the instruction which follows the STOP or the WAIT instruction, and the MCU is still in interrupt mode. At the end of this routine pending interrupts will be serviced according to their priority.

– In the event of a non-maskable interrupt, the non-maskable interrupt service routine is processed first, then the routine in which the WAIT or STOP mode was entered will be completed by executing the instruction following the STOP or WAIT instruction. The MCU remains in normal interrupt mode.

6.4.2 Recommended MCU Configuration

For lowest power consumption during RUN or WAIT modes, the user software must configure the MCU as follows:

– Configure unused I/Os as output push-pull low mode

– Place all peripherals in their power down modes before entering STOP mode

– Select the Low Frequency Auxiliary Oscillator (provided this runs at a lower frequency than the main oscillator).

The WAIT and STOP instructions are not executed if an enabled interrupt request is pending.

WATCHDOG TIMER (Cont'd)

8.1.7 Register Description

WATCHDOG REGISTER (WDGR)

Address: 0D8h - Read/Write

Reset Value: 1111 1110 (FEh)

7							0
T0	T1	T2	T3	T4	T5	SR	C

Bits 7:2 = **T[5:0]** *Downcounter bits*
Caution: These bits are reversed and shifted with respect to the physical counter: bit-7 (T0) is the LSB of the Watchdog downcounter and bit-2 (T5) is the MSB.

Bit 1 = **SR**: *Software Reset bit*
Software can generate a reset by clearing this bit while the C bit is set. When C = 0 (Watchdog deactivated) the SR bit is the MSB of the 7-bit timer.
0: Generate (write)

1: No software reset generated, MSB of 7-bit timer

Bit 0 = **C** *Watchdog Control bit*.
If the hardware option is selected (WDACT bit in Option byte), this bit is forced high and cannot be changed by the user (the Watchdog is always active). When the software option is selected (WDACT bit in Option byte), the Watchdog function is activated by setting the C bit, and cannot then be deactivated (except by resetting the MCU).

When C is kept cleared the counter can be used as a 7-bit timer.
0: Watchdog deactivated
1: Watchdog activated

8-BIT TIMER (Cont'd)

8.2.3 Counter/Prescaler Description

Prescaler

The prescaler input is the internal frequency f_{INT} divided by 12. The prescaler decrements on the rising edge, depending on the division factor programmed by the PS[2:0] bits in the TSCR register.

The state of the 7-bit prescaler can be read in the PSCR register.

When the prescaler reaches 0, it is automatically reloaded with 7Fh.

Counter

The free running 8-bit downcounter is fed by the output of the programmable prescaler, and is decremented on every rising edge of the $f_{COUNTER}$ clock signal coming from the prescaler.

It is possible to read or write the contents of the counter on the fly, by reading or writing the timer counter register (TCR).

When the downcounter reaches 0, it is automatically reloaded with the value 0FFh.

Counter Clock and Prescaler

The counter clock frequency is given by:

$$f_{COUNTER} = f_{PRESCALER} / 2^{PS[2:0]}$$

where $f_{PRESCALER}$ is:

– $f_{INT}/12$

The timer input clock feeds the 7-bit programmable prescaler. The prescaler output can be programmed by selecting one of the 8 available prescaler taps using the PS[2:0] bits in the Status/Control Register (TSCR). Thus the division factor of the prescaler can be set to 2^n (where n equals 0, to 7). See Figure 27.

The clock input is enabled by the PSI (Prescaler Initialize) bit in the TSCR register. When PSI is reset, the counter is frozen and the prescaler is loaded with the value 7Fh. When PSI is set, the prescaler and the counter run at the rate of the selected clock source.

Counter and Prescaler Initialization

After RESET, the counter and the prescaler are initialized to 0FFh and 7Fh respectively.

The 7-bit prescaler can be initialized to 7Fh by clearing the PSI bit. Direct write access to the prescaler is also possible when PSI =1. Then, any value between 0 and 7Fh can be loaded into it.

The 8-bit counter can be initialized separately by writing to the TCR register.

8.2.3.1 8-bit Counting and Interrupt Capability on Counter Underflow

Whatever the division factor defined for the prescaler, the Timer Counter works as an 8-bit downcounter. The input clock frequency is user selectable using the PS[2:0] bits.

When the downcounter decrements to zero, the TMZ (Timer Zero) bit in the TSCR is set. If the ETI (Enable Timer Interrupt) bit in the TSCR is also set, an interrupt request is generated.

The Timer interrupt can be used to exit the MCU from WAIT or STOP mode.

The TCR can be written at any time by software to define a time period ending with an underflow event, and therefore manage delay or timer functions.

TMZ is set when the downcounter reaches zero; however, it may also be set by writing 00h in the TCR register or by setting bit 7 of the TSCR register.

The TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine.

Note: A write to the TCR register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter underflows again.

8.2.4 Low Power Modes

Mode	Description
WAIT	No effect on timer. Timer interrupt events cause the device to exit from WAIT mode.
STOP	Timer registers are frozen.

8.2.5 Interrupts

Interrupt Event	Event Flag	Enable Bit	Exit from Wait	Exit from Stop
Timer Zero Event	TMZ	ETI	Yes	No

8.3 A/D CONVERTER (ADC)

8.3.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 8-bit, successive approximation converter. This peripheral has multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from different sources.

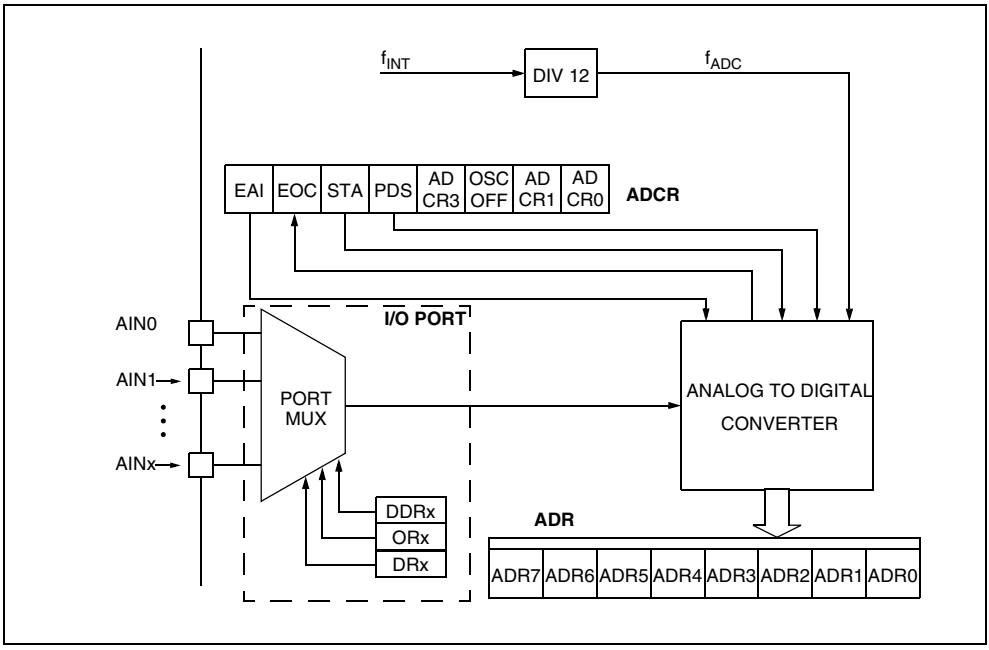
The result of the conversion is stored in a 8-bit Data Register. The A/D converter is controlled through a Control Register.

8.3.2 Main Features

- 8-bit conversion
- Multiplexed analog input channels
- Linear successive approximation
- Data register (DR) which contains the results
- End of Conversion flag
- On/Off bit (to reduce consumption)
- Typical conversion time 70 µs (with an 8 MHz crystal)

The block diagram is shown in Figure 28.

Figure 28. ADC Block Diagram



Note: ADC not present on some devices. See device summary on page 1.

A/D CONVERTER (Cont'd)

8.3.3 Functional Description

8.3.3.1 Analog Power Supply

The high and low level reference voltage pins are internally connected to the V_{DD} and V_{SS} pins.

Conversion accuracy may therefore be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines.

8.3.3.2 Digital A/D Conversion Result

The conversion is monotonic, meaning that the result never decreases if the analog input does not and never increases if the analog input does not.

If the input voltage (V_{AIN}) is greater than or equal to V_{DDA} (high-level voltage reference) then the conversion result in the DR register is FFh (full scale) without overflow indication.

If input voltage (V_{AIN}) is lower than or equal to V_{SSA} (low-level voltage reference) then the conversion result in the DR register is 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADR register. The accuracy of the conversion is described in the parametric section.

R_{AIN} is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the allocated time. Refer to the electrical characteristics chapter for more details.

With an oscillator clock frequency less than 1.2MHz, conversion accuracy is decreased.

8.3.3.3 Analog Input Selection

Selection of the input pin is done by configuring the related I/O line as an analog input via the Data Direction, Option and Data registers (refer to I/O ports description for additional information).

Caution: Only one I/O line must be configured as an analog input at any time. The user must avoid any situation in which more than one I/O pin is selected as an analog input simultaneously, because they will be shorted internally.

8.3.3.4 Software Procedure

Refer to the Control register (ADCR) and Data register (ADR) in Section 8.3.7 for the bit definitions.

Analog Input Configuration

The analog input must be configured through the Port Control registers (DDRx, ORx and DRx). Refer to the I/O port chapter.

ADC Configuration

In the ADCR register:

– Reset the PDS bit to power on the ADC. This bit must be set at least one instruction before the beginning of the conversion to allow stabilisation of the A/D converter.

– Set the EAI bit to enable the ADC interrupt if needed.

ADC Conversion

In the ADCR register:

– Set the STA bit to start a conversion. This automatically clears (resets to "0") the End Of Conversion Bit (EOC).

When a conversion is complete

– The EOC bit is set by hardware to flag that conversion is complete and that the data in the ADC data conversion register is valid.

– An interrupt is generated if the EAI bit was set

Setting the STA bit will start a new count and will clear the EOC bit (thus clearing the interrupt condition)

Note:

Setting the STA bit must be done by a different instruction from the instruction that powers-on the ADC (setting the PDS bit) in order to make sure the voltage to be converted is present on the pin.

Each conversion has to be separately initiated by writing to the STA bit.

The STA bit is continuously scanned so that, if the user sets it to "1" while a previous conversion is in progress, a new conversion is started before completing the previous one. The start bit (STA) is a write only bit, any attempt to read it will show a logical "0".

INSTRUCTION SET (Cont'd)

Conditional Branch. Branch instructions perform a branch in the program when the selected condition is met.

Bit Manipulation Instructions. These instructions can handle any bit in Data space memory. One group either sets or clears. The other group (see Conditional Branch) performs the bit test branch operations.

Control Instructions. Control instructions control microcontroller operations during program execution.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutine calls to any location in the whole program space.

Table 17. Conditional Branch Instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b 3-bit address
e 5 bit signed displacement in the range -15 to +16
ee 8 bit signed displacement in the range -126 to +129
rr Data space register
Δ Affected. The tested bit is shifted into carry.
* Not Affected

Table 18. Bit Manipulation Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b 3-bit address
rr Data space register
* Not Affected
Bit Manipulation Instructions should not be used on Port Data Registers and any registers with read only and/or write only bits (see I/O port chapter)

Table 19. Control Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated and a WAIT is automatically executed instead of a STOP if the watchdog function is selected.
Δ Affected
*Not Affected

Table 20. Jump & Call Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc 12-bit address
* Not Affected

Opcode Map Summary (Continued)

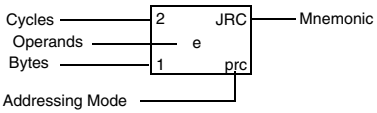
LOW / HI	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW / HI
0 **0000**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b.d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 prc	4 LD a,(y) 1 ind	**0** **0000**
1 **0001**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b.d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 prc	4 LD a,rr 2 dir	**1** **0001**
2 **0010**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b.d	2 JRZ e 1 pcr	4 COM a	2 JRC e 1 prc	4 CP a,(y) 1 ind	**2** **0010**
3 **0011**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b.d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 prc	4 CP a,rr 2 dir	**3** **0011**
4 **0100**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b.d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 prc	4 ADD a,(y) 1 ind	**4** **0100**
5 **0101**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b.d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 prc	4 ADD a,rr 2 dir	**5** **0101**
6 **0110**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b.d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 prc	4 INC (y) 1 ind	**6** **0110**
7 **0111**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b.d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 prc	4 INC rr 2 dir	**7** **0111**
8 **1000**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b.d	2 JRZ e 1 pcr	# 1 prc	2 JRC e 1 prc	4 LD (y),a 1 ind	**8** **1000**
9 **1001**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b.d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 prc	4 LD rr,a 2 dir	**9** **1001**
A **1010**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b.d	2 JRZ e 1 pcr	4 RCL a 1 inh	2 JRC e 1 prc	4 AND a,(y) 1 ind	**A** **1010**
B **1011**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b.d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 prc	4 AND a,rr 2 dir	**B** **1011**
C **1100**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b.d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 prc	4 SUB a,(y) 1 ind	**C** **1100**
D **1101**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b.d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 prc	4 SUB a,rr 2 dir	**D** **1101**
E **1110**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b.d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 prc	4 DEC (y) 1 ind	**E** **1110**
F **1111**	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b.d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 prc	4 DEC rr 2 dir	**F** **1111**

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5-bit Displacement
b	3-bit Address
rr	1-byte Data space address
nn	1-byte immediate data
abc	12-bit address
ee	8-bit Displacement



10.4 SUPPLY CURRENT CHARACTERISTICS

The following current consumption specified for the ST6 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for STOP mode for which the clock is stopped).

10.4.1 RUN Modes

Symbol	Parameter	Conditions		Typ [1]	Max [2]	Unit
I_{DD}	Supply current in RUN mode [3] (see Figure 36 & Figure 37)	4.5V≤V_{DD}≤6.0V	f_{OSC}=32kHz	0.5	0.7	mA
			f_{OSC}=1MHz	1.3	1.7	
			f_{OSC}=2MHz	1.6	2.4	
			f_{OSC}=4MHz	2.2	3.3	
			f_{OSC}=8MHz	3.3	4.8	
	Supply current in RUN mode [3] (see Figure 36 & Figure 37)	3V≤V_{DD}≤3.6V	f_{OSC}=32kHz	0.3	0.4	
			f_{OSC}=1MHz	0.6	0.8	
			f_{OSC}=2MHz	0.9	1.2	
			f_{OSC}=4MHz	1.0	1.5	
			f_{OSC}=8MHz	1.8	2.3	

Notes:

1. Typical data are based on T_A=25°C, V_{DD}=5V (4.5V≤V_{DD}≤6.0V range) and V_{DD}=3.3V (3V≤V_{DD}≤3.6V range).
2. Data based on characterization results, tested in production at V_{DD} max. and f_{OSC} max.
3. CPU running with memory access, all I/O pins in input with pull-up mode (no load), all peripherals in reset state; clock input (OSC_{IN}) driven by external square wave, OSG and LVD disabled, option bytes not programmed.

Figure 36. Typical I_{DD} in RUN vs. f_{CPU}

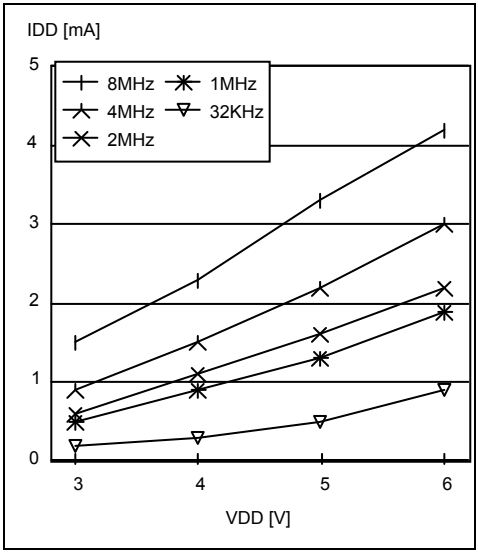
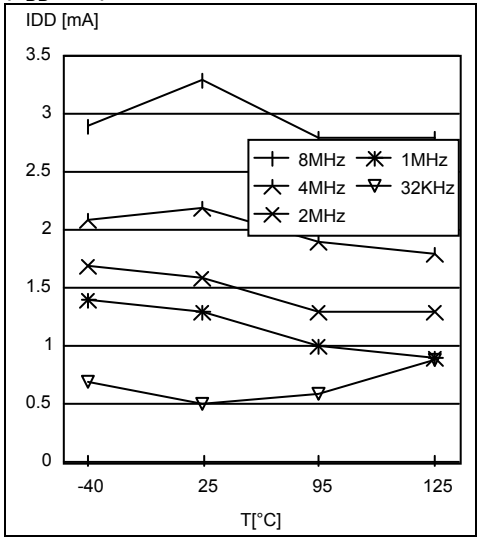


Figure 37. Typical I_{DD} in RUN vs. Temperature (V_{DD} = 5V)



SUPPLY CURRENT CHARACTERISTICS (Cont'd)

Figure 38. Typical I_{DD} in WAIT vs f_{CPU} and Temperature for OTP devices with option bytes not programmed

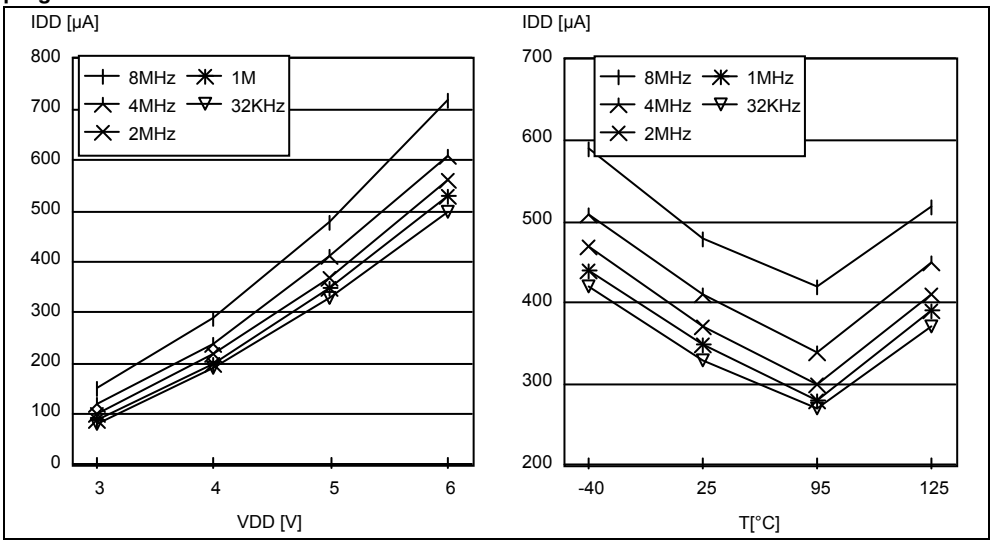
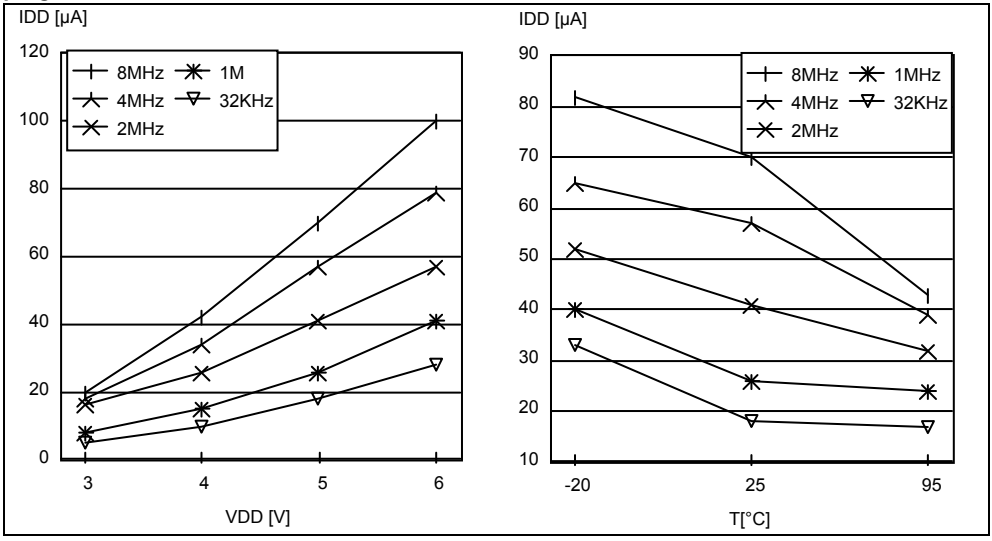


Figure 39. Typical I_{DD} in WAIT vs f_{CPU} and Temperature for OTP devices with option bytes programmed to 00H



10.5 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

10.5.1 General Timings

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	4	5	t_{CPU}
		f_{CPU}=8 MHz	3.25	6.5	8.125	µs
$t_{v(IT)}$	Interrupt reaction time [2] $t_{v(IT)} = \Delta t_{c(INST)} + 6$		6		11	t_{CPU}
		f_{CPU}=8 MHz	9.75		17.875	µs

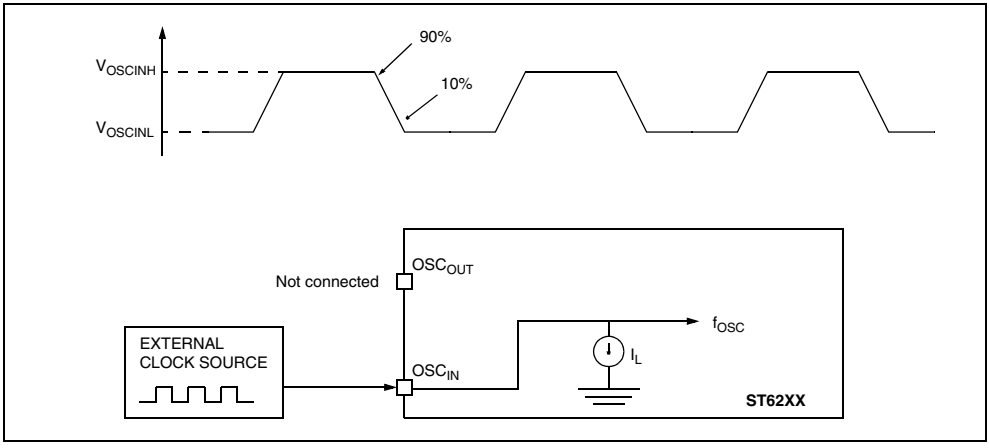
10.5.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSCINH}	OSC_{IN} input pin high level voltage	See Figure 43	$0.7xV_{DD}$		V_{DD}	V
V_{OSCINL}	OSC_{IN} input pin low level voltage		V_{SS}		$0.3xV_{DD}$	
I_L	OSCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			± 2	µA

Notes:

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

Figure 43. Typical Application with an External Clock Source



10.7 EMC CHARACTERISTICS

Susceptibility tests are performed on a sample basis during product characterization.

10.7.1 Functional EMS

(Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

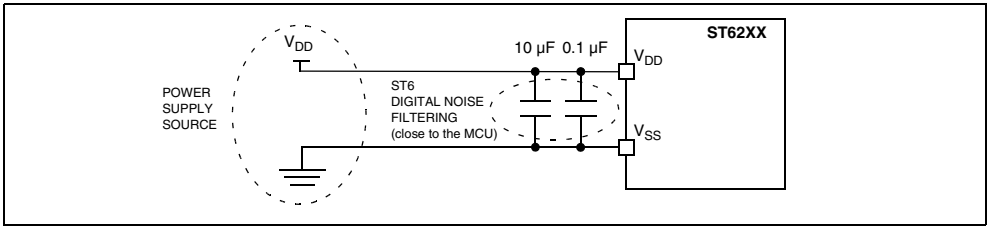
A device reset allows normal operations to be resumed.

Symbol	Parameter	Conditions	Neg [1]	Pos [1]	Unit
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-2	-2	2	kV
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-4	-2.5	3	

Notes:

1. Data based on characterization results, not tested in production.
2. The suggested 10 µF and 0.1 µF decoupling capacitors on the power supply lines are proposed as a good price vs. EMC performance tradeoff. They have to be put as close as possible to the device power supply pins. Other EMC recommendations are given in other sections (I/Os, RESET, OSCx pin characteristics).

Figure 50. EMC Recommended Star Network Power Supply Connection [2]



I/O PORT PIN CHARACTERISTICS (Cont'd)

10.8.2 Output Driving Current

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL} 1)	Output low level voltage for a standard I/O pin (see Figure 57 and Figure 60)	V_{DD}=5V	I_{IO}=+10µA, $T_A \leq 125°C$		0.1	V
			I_{IO}=+3mA, $T_A \leq 125°C$		0.8	
			I_{IO}=+5mA, $T_A \leq 85°C$		0.8	
			I_{IO}=+10mA, $T_A \leq 85°C$		1.2	
	Output low level voltage for a high sink I/O pin (see Figure 58 and Figure 61)		I_{IO}=+10µA, $T_A \leq 125°C$		0.1	
			I_{IO}=+7mA, $T_A \leq 125°C$		0.8	
			I_{IO}=+10mA, $T_A \leq 85°C$		0.8	
			I_{IO}=+15mA, $T_A \leq 125°C$		1.3	
			I_{IO}=+20mA, $T_A \leq 85°C$		1.3	
			I_{IO}=+30mA, $T_A \leq 85°C$		2	
V_{OH} 2)	Output high level voltage for an I/O pin (see Figure 59 and Figure 62)		I_{IO}=-10µA, $T_A \leq 125°C$	V_{DD}-0.1		
			I_{IO}=-3mA, $T_A \leq 125°C$	V_{DD}-1.5		
			I_{IO}=-5mA, $T_A \leq 85°C$	V_{DD}-1.5		

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 10.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current source must always respect the absolute maximum rating specified in Section 10.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}. True open drain I/O pins does not have V_{OH}.

Figure 57. Typical V_{OL} at V_{DD} = 5V (standard)

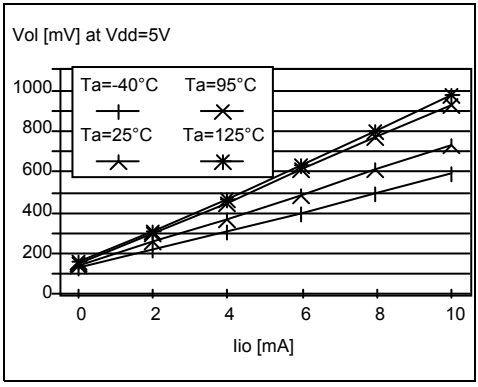
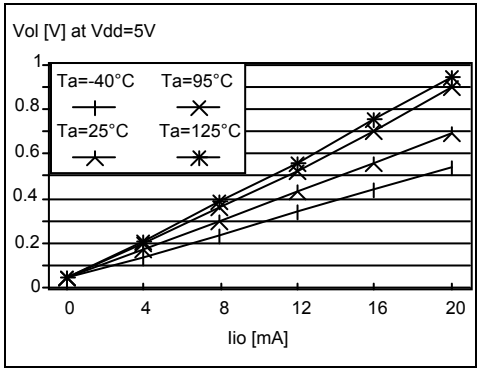
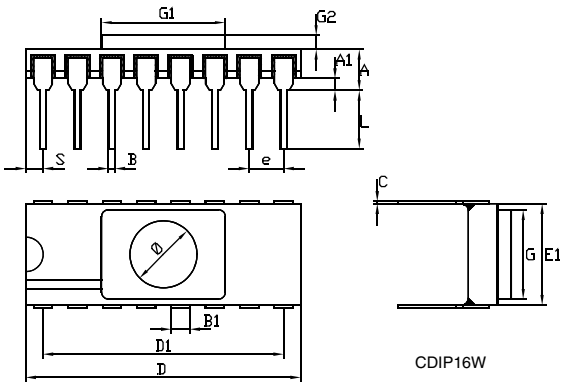


Figure 58. Typical V_{OL} at V_{DD} = 5V (high-sink)



PACKAGE MECHANICAL DATA (Cont'd)

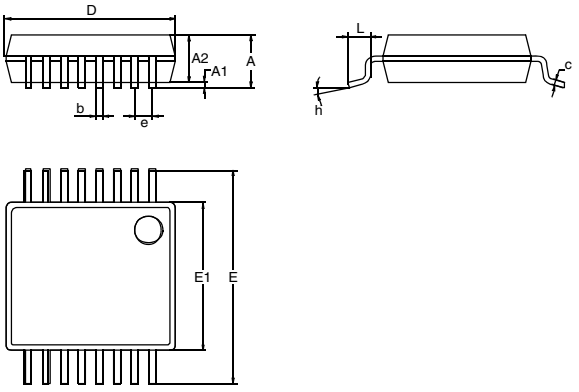
Figure 70. 16-Pin Ceramic Side-Brazed Dual In-Line Package



CDIP16W

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.78			0.149
A1	0.38			0.015		
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.14	1.37	1.78	0.045	0.054	0.070
C	0.20	0.25	0.36	0.008	0.010	0.014
D	19.86	20.32	20.78	0.782	0.800	0.818
D1		17.78			0.700	
E1	7.04	7.49	7.95	0.277	0.295	0.313
e		2.54			0.100	
G	6.35	6.60	6.86	0.250	0.260	0.270
G1	9.47	9.73	9.98	0.373	0.383	0.393
G2		1.02			0.040	
L	2.92	3.30	3.81	0.115	0.130	0.150
S		1.27			0.050	
Ø		4.22			0.166	
	Number of Pins					
N	16					

Figure 71. 16-Pin Plastic Shrink Small Outline Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			2.00			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22		0.38	0.009		0.015
c	0.09		0.25	0.004		0.010
D	5.90	6.20	6.50	0.232	0.244	0.256
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e		0.65			0.026	
θ	0°	4°	8°	0°	4°	8°
L	0.55	0.75	0.95	0.022	0.030	0.037
	Number of Pins					
N	16					

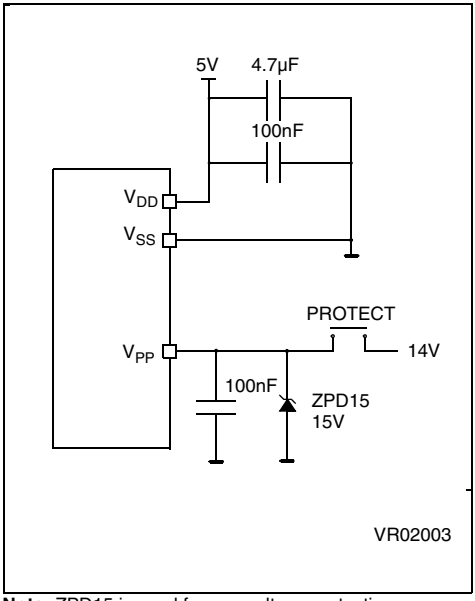
TRANSFER OF CUSTOMER CODE (Cont'd)

11.6.2 ROM VERSION

The ST6200C, 01C and 03C are mask programmed ROM version of ST62T00C, T01 and T03C OTP devices.

They offer the same functionality as OTP devices, selecting as ROM options the options defined in the programmable option byte of the OTP version.

Figure 73. Programming Circuit

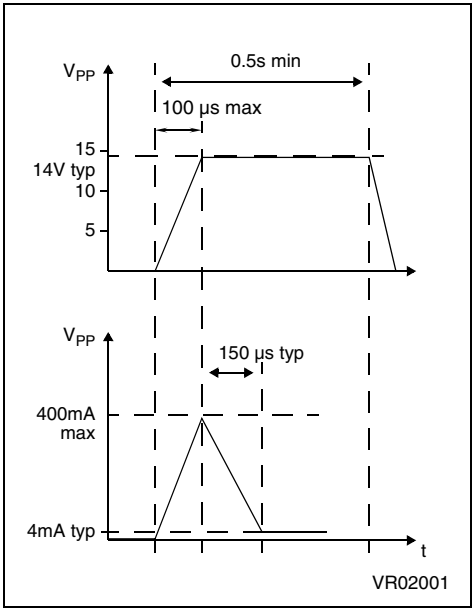


Note: ZPD15 is used for overvoltage protection

ROM Readout Protection. If the ROM READOUT PROTECTION option is selected, a protection fuse can be blown to prevent any access to the program memory content.

In case the user wants to blow this fuse, high voltage must be applied on the V_{PP} pin.

Figure 74. Programming wave form



IDENTIFICATION	DESCRIPTION
AN913	PWM GENERATION WITH ST62 16-BIT AUTO-RELOAD TIMER
AN914	USING ST626X SPI AS UART
AN1016	ST6 USING THE ST623XB/ST628XB UART
AN1050	ST6 INPUT CAPTURE WITH ST62 16-BIT AUTO-RELOAD TIMER
AN1127	USING THE ST62T6XC/5XC SPI IN MASTER MODE
GENERAL	
AN683	MCUS - 8/16-BIT MICROCONTROLLERS (MCUS) APPLICATION NOTES ABSTRACTS BY TOPICS
AN886	SELECTING BETWEEN ROM AND OTP FOR A MICROCONTROLLER
AN887	MAKING IT EASY WITH MICROCONTROLLERS
AN898	EMC GENERAL INFORMATION
AN899	SOLDERING RECOMMENDATIONS AND PACKAGING INFORMATION
AN900	INTRODUCTION TO SEMICONDUCTOR TECHNOLOGY
AN901	EMC GUIDE-LINES FOR MICROCONTROLLER - BASED APPLICATIONS
AN902	QUALITY AND RELIABILITY INFORMATION
AN912	A SIMPLE GUIDE TO DEVELOPMENT TOOLS
AN1181	ELECTROSTATIC DISHARGE SENSITIVITY MEASUREMENT