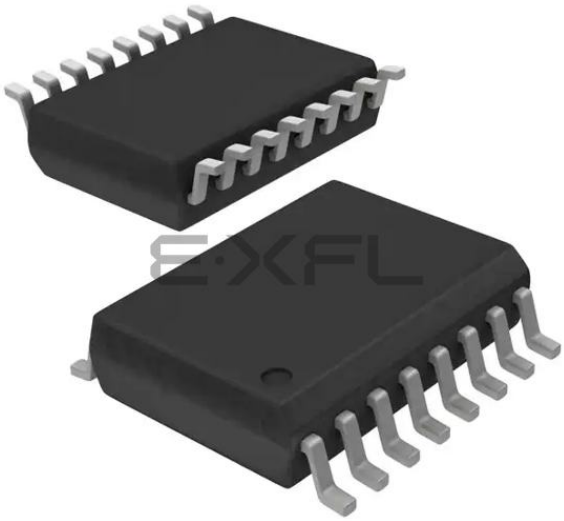

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	9
Program Memory Size	2KB (2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t01cm6

MEMORY MAP (Cont'd)

Table 2. Hardware Register Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
080h to 083h	CPU	X,Y,V,W	X,Y index registers V,W short direct registers	xxh	R/W
0C0h 0C1h	I/O Ports	DRA [1) 2) 3)] DRB [1) 2) 3)]	Port A Data Register Port B Data Register	00h 00h	R/W R/W
0C2h 0C3h	Reserved (2 Bytes)				
0C4h 0C5h	I/O Ports	DDRA [2)] DDRB [2)]	Port A Direction Register Port B Direction Register	00h 00h	R/W R/W
0C6h 0C7h	Reserved (2 Bytes)				
0C8h	CPU	IOR	Interrupt Option Register	xxh	Write-only
0C9h	ROM	DRWR	Data ROM Window register	xxh	Write-only
0CAh 0CBh	Reserved (2 Bytes)				
0CCh 0CDh	I/O Ports	ORA [2)] ORB [2)]	Port A Option Register Port B Option Register	00h 00h	R/W R/W
0CEh 0CFh	Reserved (2 bytes)				
0D0h 0D1h	ADC	ADR ADCR	A/D Converter Data Register A/D Converter Control Register	xxh 40h	Read-only Ro/Wo
0D2h 0D3h 0D4h	Timer 1	PSCR TCR TSCR	Timer 1 Prescaler Register Timer 1 Downcounter Register Timer 1 Status Control Register	7Fh 0FFh 00h	R/W R/W R/W
0D5h to 0D7h	Reserved (3 Bytes)				
0D8h	Watchdog Timer	WDGR	Watchdog Register	0FEh	R/W
0D9h to 0FEh	Reserved (38 Bytes)				
0FFh	CPU	A	Accumulator	xxh	R/W

Legend :

x = undefined, R/W = Read/Write, Ro = Read-only Bit(s) in the register, Wo = Write-only Bit(s) in the register.

Notes :

1. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.

2. The bits associated with unavailable pins must always be kept at their reset value.

3. Do not use single-bit instructions (SET, RES...) on Port Data Registers if any pin of the port is configured in input mode (refer to Section 7 "I/O PORTS" on page 36 for more details).
4. Depending on device. See device summary on page 1.

CLOCK SYSTEM (Cont'd)

5.1.1 Main Oscillator

The oscillator configuration is specified by selecting the appropriate option in the option bytes (refer to the Option Bytes section of this document). When the CRYSTAL/RESONATOR option is selected, it must be used with a quartz crystal, a ceramic resonator or an external signal provided on the OSCin pin. When the RC NETWORK option is selected, the system clock is generated by an external resistor (the capacitor is implemented internally).

The main oscillator can be turned off (when the OSG ENABLED option is selected) by setting the OSCOFF bit of the ADC Control Register (not available on some devices). This will automatically start the Low Frequency Auxiliary Oscillator (LFAO).

The main oscillator can be turned off by resetting the OSCOFF bit of the A/D Converter Control Register or by resetting the MCU. When the main oscillator starts there is a delay made up of the oscillator start-up delay period plus the duration of the software instruction at a clock frequency f_{LFAO}.

Caution: It should be noted that when the RC network option is selected, the accuracy of the frequency is about 20% so it may not be suitable for some applications (For more details, please refer to the Electrical Characteristics Section).

Table 5. Oscillator Configurations

	Hardware Configuration
Crystal/Resonator Option 1)	External Clock ST6 OSCin OSCout NC EXTERNAL CLOCK
Crystal/Resonator Option 1)	Crystal/Resonator Clock 2) ST6 OSCin OSCout C_{L1} C_{L2} LOAD CAPACITORS 3)
RC Network Option 1)	RC Network ST6 OSCin OSCout NC R_{NET}
OSG Enabled Option 1)	LFAO ST6 OSCin OSCout NC

Notes:
1. To select the options shown in column 1 of the above table, refer to the Option Byte section.

2.This schematic are given for guidance only and are subject to the schematics given by the crystal or ceramic resonator manufacturer.
3. For more details, please refer to the Electrical Characteristics Section.

CLOCK SYSTEM (Cont'd)

5.1.2 Oscillator Safeguard (OSG)

The Oscillator Safeguard (OSG) feature is a means of dramatically improving the operational integrity of the MCU. It is available when the OSG ENABLED option is selected in the option byte (refer to the Option Bytes section of this document).

The OSG acts as a filter whose cross-over frequency is device dependent and provides three basic functions:

– Filtering spikes on the oscillator lines which would result in driving the CPU at excessive frequencies

– Management of the Low Frequency Auxiliary Oscillator (LFAO), (useable as low cost internal clock source, backup clock in case of main oscillator failure or for low power consumption)

– Automatically limiting the f_{INT} clock frequency as a function of supply voltage, to ensure correct operation even if the power supply drops.

5.1.2.1 Spike Filtering

Spikes on the oscillator lines result in an effectively increased internal clock frequency. In the absence of an OSG circuit, this may lead to an over frequency for a given power supply voltage. The OSG filters out such spikes (as illustrated in Figure 10). In all cases, when the OSG is active, the maximum internal clock frequency, f_{INT}, is limited to f_{OSG}, which is supply voltage dependent.

5.1.2.2 Management of Supply Voltage Variations

Over-frequency, at a given power supply level, is seen by the OSG as spikes; it therefore filters out some cycles in order that the internal clock frequency of the device is kept within the range the particular device can stand (depending on V_{DD}), and below f_{OSG}: the maximum authorised frequency with OSG enabled.

5.1.2.3 LFAO Management

When the OSG is enabled, the Low Frequency Auxiliary Oscillator can be used (see Section 5.1.3).

Note: The OSG should be used wherever possible as it provides maximum security for the application. It should be noted however, that it can increase power consumption and reduce the maximum operating frequency to f_{OSG} (see Electrical Characteristics section).

Caution: Care has to be taken when using the OSG, as the internal frequency is defined between a minimum and a maximum value and may vary depending on both V_{DD} and temperature. For precise timing measurements, it is not recommended to use the OSG.

Figure 10. OSG Filtering Function

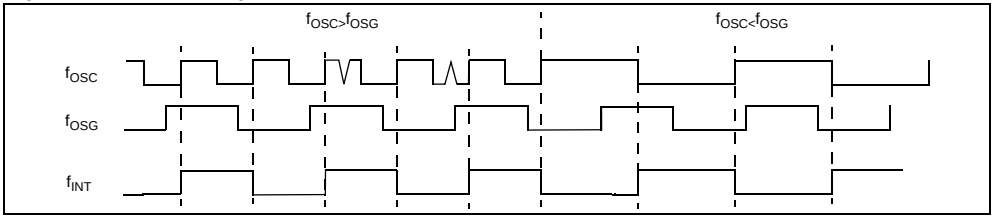
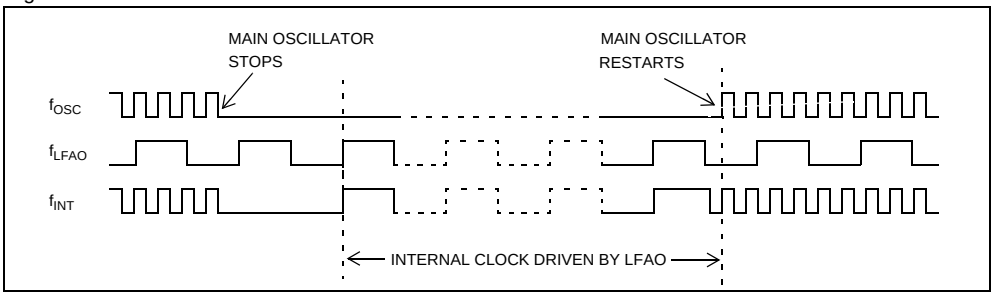


Figure 11. LFAO Oscillator Function



6.2 WAIT MODE

The MCU goes into WAIT mode as soon as the WAIT instruction is executed. This has the following effects:

– Program execution is stopped, the microcontroller software can be considered as being in a "frozen" state.

– RAM contents and peripheral registers are preserved as long as the power supply voltage is higher than the RAM retention voltage.

– The oscillator is kept running to provide a clock to the peripherals; they are still active.

WAIT mode can be used when the user wants to reduce the MCU power consumption during idle periods, while not losing track of time or the ability to monitor external events. WAIT mode places the MCU in a low power consumption mode by stopping the CPU. The active oscillator (main oscillator or LFAO) is kept running in order to provide a clock signal to the peripherals.

If the power consumption has to be further reduced, the Low Frequency Auxiliary Oscillator (LFAO) can be used in place of the main oscillator, if its operating frequency is lower. If required, the LFAO must be switched on before entering WAIT mode.

Exit from Wait mode

The MCU remains in WAIT mode until one of the following events occurs:

– RESET (Watchdog, LVD or $\overline{\text{RESET}}$ pin)

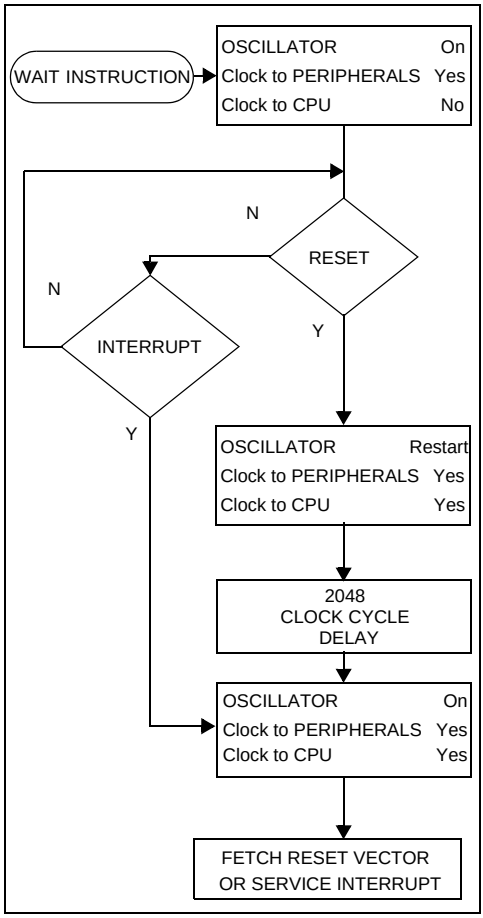
– A peripheral interrupt (timer, ADC,...),

– An external interrupt (I/O port, NMI)

The Program Counter then branches to the starting address of the interrupt or RESET service routine. Refer to Figure 20.

See also Section 6.4.1.

Figure 20. WAIT Mode Flowchart



I/O PORTS (Cont'd)

7.5 REGISTER DESCRIPTION

DATA REGISTER (DR)

Port x Data Register
DRx with x = A or B.

Address DRA: 0C0h - Read/Write
Address DRB: 0C1h - Read/Write

Reset Value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7:0 = D[7:0] *Data register bits.*

Reading the DR register returns either the DR register latch content (pin configured as output) or the digital value applied to the I/O pin (pin configured as input).

Caution: In input mode, modifying this register will modify the I/O port configuration (see Table 8).

Do not use the Single bit instructions on I/O port data registers. See (Section 7.2.5).

DATA DIRECTION REGISTER (DDR)

Port x Data Direction Register
DDRx with x = A or B.

Address DDRA: 0C4h - Read/Write
Address DDRB: 0C5h - Read/Write

Reset Value: 0000 0000 (00h)

7							0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Bit 7:0 = DD[7:0] *Data direction register bits.*

The DDR register gives the input/output direction configuration of the pins. Each bit is set and cleared by software.
0: Input mode
1: Output mode

OPTION REGISTER (OR)

Port x Option Register
ORx with x = A or B.

Address ORA: 0CCh - Read/Write
Address ORB: 0CDh - Read/Write

Reset Value: 0000 0000 (00h)

7							0
O7	O6	O5	O4	O3	O2	O1	O0

Bit 7:0 = O[7:0] *Option register bits.*

The OR register allows to distinguish in output mode if the push-pull or open drain configuration is selected.

Output mode:
0: Open drain output(with P-Buffer deactivated)
1: Push-pull Output

Input mode: See Table 8.

Each bit is set and cleared by software.

Caution: Modifying this register, will also modify the I/O port configuration in input mode. (see Table 8).

Table 10. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Reset Value of all I/O port registers		0	0	0	0	0	0	0	0
0C0h	DRA	MSB							LSB
0C1h	DRB								
0C4h	DDRA	MSB							LSB
0C5h	DDRB								
0CCh	ORA	MSB							LSB
0CDh	ORB								

WATCHDOG TIMER (Cont'd)

8.1.7 Register Description

WATCHDOG REGISTER (WDGR)

Address: 0D8h - Read/Write

Reset Value: 1111 1110 (FEh)

7							0
T0	T1	T2	T3	T4	T5	SR	C

Bits 7:2 = T[5:0] *Downcounter bits*
Caution: These bits are reversed and shifted with respect to the physical counter: bit-7 (T0) is the LSB of the Watchdog downcounter and bit-2 (T5) is the MSB.

Bit 1 = SR: *Software Reset bit*
Software can generate a reset by clearing this bit while the C bit is set. When C = 0 (Watchdog deactivated) the SR bit is the MSB of the 7-bit timer.
0: Generate (write)

1: No software reset generated, MSB of 7-bit timer

Bit 0 = C *Watchdog Control bit*.
If the hardware option is selected (WDACT bit in Option byte), this bit is forced high and cannot be changed by the user (the Watchdog is always active). When the software option is selected (WDACT bit in Option byte), the Watchdog function is activated by setting the C bit, and cannot then be deactivated (except by resetting the MCU).

When C is kept cleared the counter can be used as a 7-bit timer.
0: Watchdog deactivated
1: Watchdog activated

8.2 8-BIT TIMER

8.2.1 Introduction

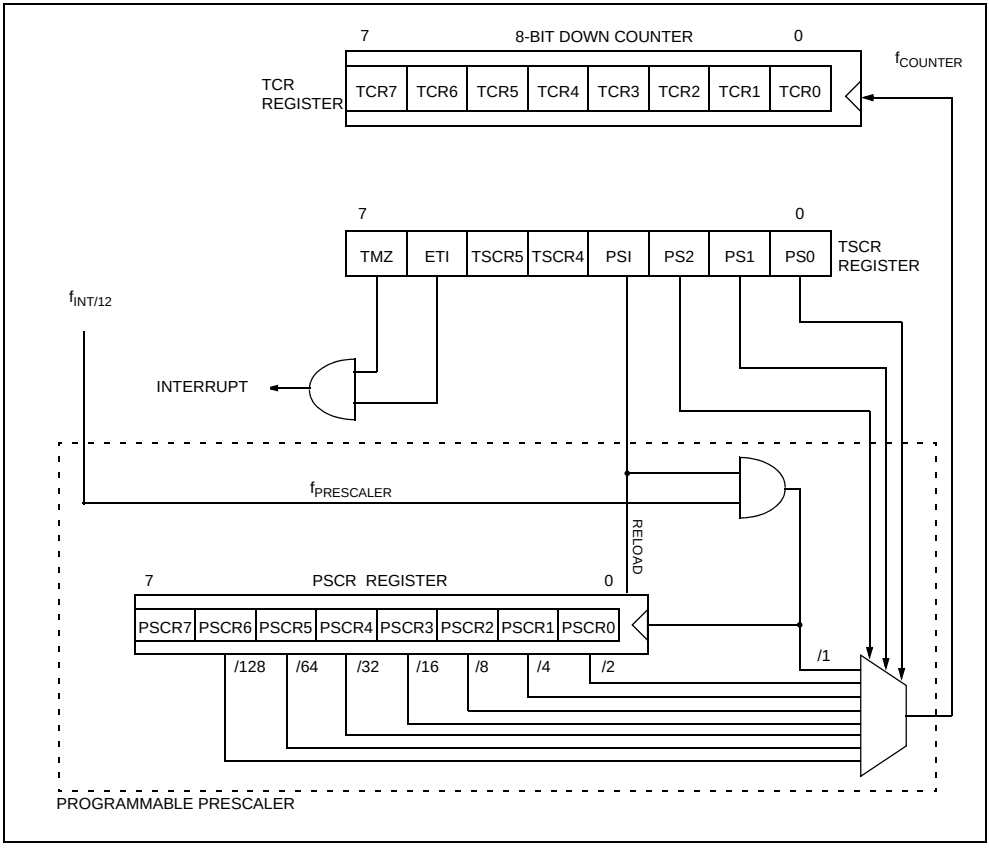
The 8-Bit Timer on-chip peripheral is a free running downcounter based on an 8-bit downcounter with a 7-bit programmable prescaler, giving a maximum count of 2^{15}.

8.2.2 Main Features

- Time-out downcounting mode with up to 15-bit accuracy
- Interrupt capability on counter underflow

The timer can be used in WAIT mode to wake up the MCU.

Figure 27. Timer Block Diagram



8-BIT TIMER (Cont'd)

8.2.3 Counter/Prescaler Description

Prescaler

The prescaler input is the internal frequency f_{INT} divided by 12. The prescaler decrements on the rising edge, depending on the division factor programmed by the PS[2:0] bits in the TSCR register.

The state of the 7-bit prescaler can be read in the PSCR register.

When the prescaler reaches 0, it is automatically reloaded with 7Fh.

Counter

The free running 8-bit downcounter is fed by the output of the programmable prescaler, and is decremented on every rising edge of the $f_{COUNTER}$ clock signal coming from the prescaler.

It is possible to read or write the contents of the counter on the fly, by reading or writing the timer counter register (TCR).

When the downcounter reaches 0, it is automatically reloaded with the value 0FFh.

Counter Clock and Prescaler

The counter clock frequency is given by:

$$f_{COUNTER} = f_{PRESCALER} / 2^{PS[2:0]}$$

where $f_{PRESCALER}$ is:

– $f_{INT}/12$

The timer input clock feeds the 7-bit programmable prescaler. The prescaler output can be programmed by selecting one of the 8 available prescaler taps using the PS[2:0] bits in the Status/Control Register (TSCR). Thus the division factor of the prescaler can be set to 2^n (where n equals 0, to 7). See Figure 27.

The clock input is enabled by the PSI (Prescaler Initialize) bit in the TSCR register. When PSI is reset, the counter is frozen and the prescaler is loaded with the value 7Fh. When PSI is set, the prescaler and the counter run at the rate of the selected clock source.

Counter and Prescaler Initialization

After RESET, the counter and the prescaler are initialized to 0FFh and 7Fh respectively.

The 7-bit prescaler can be initialized to 7Fh by clearing the PSI bit. Direct write access to the prescaler is also possible when PSI =1. Then, any value between 0 and 7Fh can be loaded into it.

The 8-bit counter can be initialized separately by writing to the TCR register.

8.2.3.1 8-bit Counting and Interrupt Capability on Counter Underflow

Whatever the division factor defined for the prescaler, the Timer Counter works as an 8-bit downcounter. The input clock frequency is user selectable using the PS[2:0] bits.

When the downcounter decrements to zero, the TMZ (Timer Zero) bit in the TSCR is set. If the ETI (Enable Timer Interrupt) bit in the TSCR is also set, an interrupt request is generated.

The Timer interrupt can be used to exit the MCU from WAIT or STOP mode.

The TCR can be written at any time by software to define a time period ending with an underflow event, and therefore manage delay or timer functions.

TMZ is set when the downcounter reaches zero; however, it may also be set by writing 00h in the TCR register or by setting bit 7 of the TSCR register.

The TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine.

Note: A write to the TCR register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter underflows again.

8.2.4 Low Power Modes

Mode	Description
WAIT	No effect on timer. Timer interrupt events cause the device to exit from WAIT mode.
STOP	Timer registers are frozen.

8.2.5 Interrupts

Interrupt Event	Event Flag	Enable Bit	Exit from Wait	Exit from Stop
Timer Zero Event	TMZ	ETI	Yes	No

A/D CONVERTER (Cont'd)

8.3.5 Low Power Modes

Mode	Description
WAIT	No effect on A/D Converter. ADC interrupts cause the device to exit from Wait mode.
STOP	A/D Converter disabled.

Note: The A/D converter may be disabled by clearing the PDS bit. This feature allows reduced power consumption when no conversion is needed.

8.3.6 Interrupts

Interrupt Event	Event Flag	Enable Bit	Exit from Wait	Exit from Stop
End of Conversion	EOC	EAI	Yes	No

Note: The EOC bit is cleared only when a new conversion is started (it cannot be cleared by writing 0). To avoid generating further EOC interrupt, the EAI bit has to be cleared within the ADC interrupt subroutine.

8.3.7 Register Description

A/D CONVERTER CONTROL REGISTER (ADCR)

Address: 0D1h - Read/Write (Bit 6 Read Only, Bit 5 Write Only)

Reset value: 0100 0000 (40h)

7							0
EAI	EOC	STA	PDS	ADCR 3	OSC OFF	ADCR 1	ADCR 0

Bit 7 = EAI *Enable A/D Interrupt.*
0: ADC interrupt disabled
1: ADC interrupt enabled

Bit 6 = EOC *End of conversion. Read Only*
When a conversion has been completed, this bit is set by hardware and an interrupt request is generated if the EAI bit is set. The EOC bit is automatically cleared when the STA bit is set. Data in the data conversion register are valid only when this bit is set to "1".
0: Conversion is not complete
1: Conversion can be read from the ADR register

Bit 5 = STA*: Start of Conversion. Write Only*.
0: No effect
1: Start conversion

Note: Setting this bit automatically clears the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

Bit 4 = PDS *Power Down Selection.*

0: A/D converter is switched off
1: A/D converter is switched on

Bit 3 = ADCR3 Reserved , must be cleared.

Bit 2 = OSCOFF *Main Oscillator off.*

0: Main Oscillator enabled
1: Main Oscillator disabled

Note: This bit does not apply to the ADC peripheral but to the main clock system. Refer to the Clock System section.

Bits 1:0 = ADCR[1:0] Reserved , must be cleared.

A/D CONVERTER DATA REGISTER (ADR)

Address: 0D0h - Read only

Reset value: xxxx xxxx (xxh)

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

Bits 7:0 = ADR[7:0] *: 8 Bit A/D Conversion Result.*

Table 14. ADC Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0D0h	ADR Reset Value	ADR7 0	ADR6 0	ADR5 0	ADR4 0	ADR3 0	ADR2 0	ADR1 0	ADR0 0
0D1h	ADCR Reset Value	EAI 0	EOC 1	STA 0	PDS 0	ADCR3 0	OSCOFF 0	ADCR1 0	ADCR0 0

10.7 EMC CHARACTERISTICS

Susceptibility tests are performed on a sample basis during product characterization.

10.7.1 Functional EMS

(Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- ESD: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

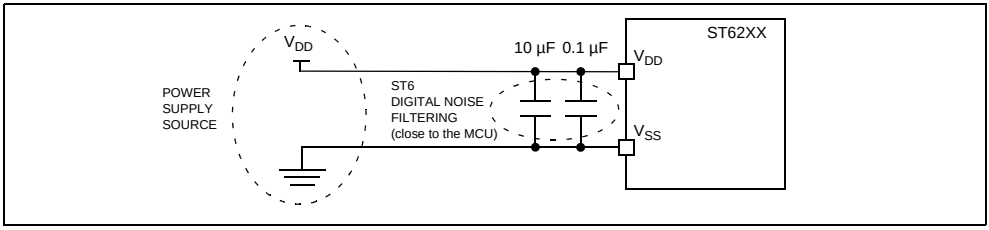
A device reset allows normal operations to be resumed.

Symbol	Parameter	Conditions	Neg [1]	Pos [1]	Unit
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-2	-2	2	kV
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-4	-2.5	3	

Notes:

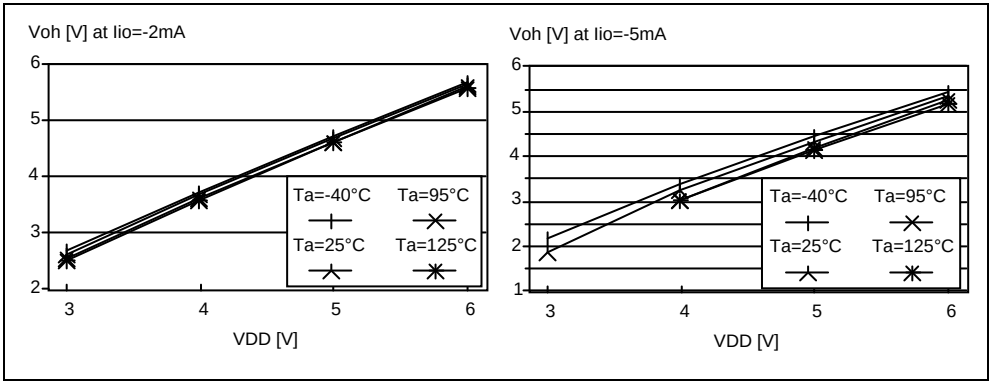
1. Data based on characterization results, not tested in production.
2. The suggested 10 µF and 0.1 µF decoupling capacitors on the power supply lines are proposed as a good price vs. EMC performance tradeoff. They have to be put as close as possible to the device power supply pins. Other EMC recommendations are given in other sections (I/Os, RESET, OSCx pin characteristics).

Figure 50. EMC Recommended Star Network Power Supply Connection [2]



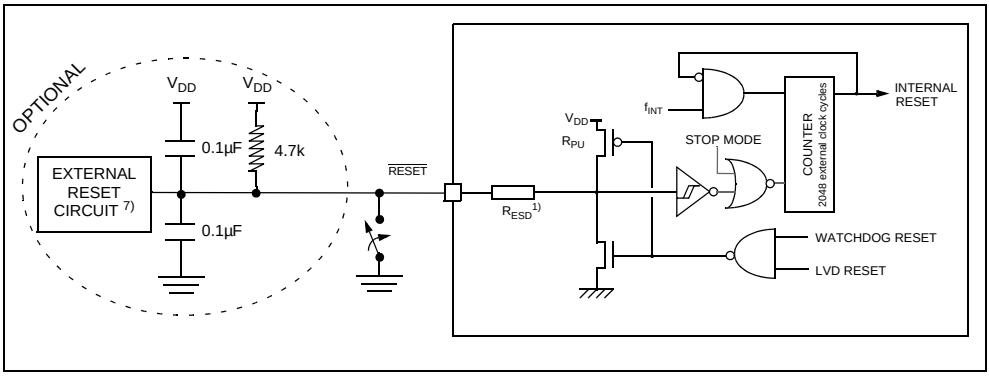
I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 62. Typical V_{OH} vs V_{DD}



CONTROL PIN CHARACTERISTICS (Cont'd)

Figure 64. Typical Application with $\overline{\text{RESET}}$ pin [8)]



10.9.2 NMI Pin

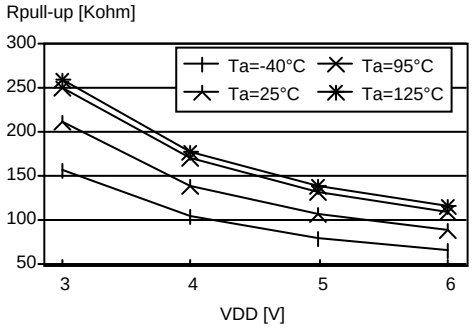
Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1)]	Max	Unit
V_{IL}	Input low level voltage [2)]					$0.3xV_{DD}$	V
V_{IH}	Input high level voltage [2)]			$0.7xV_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis [3)]			200	400		mV
$R_{pull-up}$	Weak pull-up equivalent resistor [4)]	$V_{IN}=V_{SS}$	V_{DD}=5V	40	100	350	k
			V_{DD}=3.3V	80	200	700	

Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}=5V.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The $R_{pull-up}$ equivalent resistor is based on a resistive transistor. This data is based on characterization results, not tested in production.

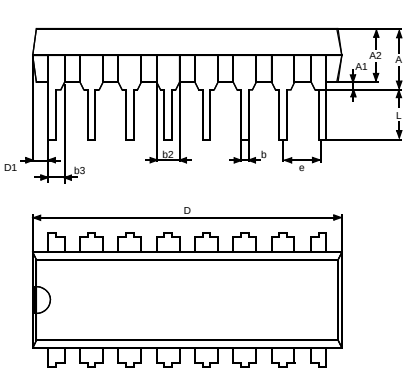
Figure 65. Typical $R_{pull-up}$ vs. V_{DD} with $V_{IN}=V_{SS}$



11 GENERAL INFORMATION

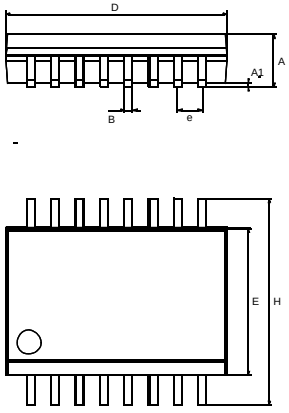
11.1 PACKAGE MECHANICAL DATA

Figure 68. 16-Pin Plastic Dual In-Line Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
b3	0.76	0.99	1.14	0.030	0.039	0.045
c	0.20	0.25	0.36	0.008	0.010	0.014
D	18.67	19.18	19.69	0.735	0.755	0.775
D1	0.13			0.005		
e		2.54			0.100	
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150
eB			10.92			0.430
	Number of Pins					
N	16					

Figure 69. 16-Pin Plastic Small Outline Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	10.10		10.50	0.398		0.413
E	7.40		7.60	0.291		0.299
H	10.00		10.65	0.394		0.419
e		1.27			0.050	
h	0.25		0.75	0.010		0.030
	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
	Number of Pins					
N	16					

12 DEVELOPMENT TOOLS

STMicroelectronics offers a range of hardware and software development tools for the ST6 microcontroller family. Full details of tools available for the ST6 from third party manufacturers can be obtain from the STMicroelectronics Internet site: ➟ http://www.st.com.

Table 24. Dedicated Third Parties Development Tools

Third Party [1)]	Designation	ST Sales Type	Web site address
ACTUM	ST-REALIZER II: Graphical Schematic based Development available from STMicroelectronics.	STREALIZER-II	http://www.actum.com/
CEIBO	Low cost emulator available from CEIBO.		http://www.ceibo.com/
RAISONANCE	This tool includes in the same environment: an assembler, linker, C compiler, debugger and simulator. The assembler package (plus limited C compiler) is free and can be downloaded from raisonance web site. The full version is available both from STMicroelectronics and Raisonance.	ST6RAIS-SWC/PC	http://www.raisonance.com/
SOFTEC	High end emulator available from SOFTEC.		http://www.softecmicro.com/
	Gang programmer available from SOFTEC.		
ADVANCED EQUIPMENT	Single and gang programmers		http://www.aec.com.tw/
ADVANCED TRANSDATA			http://www.adv-transdata.com/
BP MICROSYSTEMS			http://www.bpmicro.com/
DATA I/O			http://www.data-io.com/
DATAMAN			http://www.dataman.com/
EE TOOLS			http://www.eetools.com/
ELNEC			http://www.elnec.com/
HI-LO SYSTEMS			http://www.hilosystems.com.tw/
ICE TECHNOLOGY			http://www.icetech.com/
LEAP			http://www.leap.com.tw/
LLOYD RESEARCH			http://www.lloyd-research.com/
LOGICAL DEVICES			http://www.chipprogrammers.com/
MQP ELECTRONICS			http://www.mqp.com/
NEEDHAMS ELECTRONICS			http://www.needhams.com/
STAG PROGRAMMERS			http://www.stag.co.uk/
SYSTEM GENERAL CORP			http://www.sg.com.tw
TRIBAL MICROSYSTEMS			http://www.tribalmicro.com/
XELTEK			http://www.xeltek.com/

Note 1: For latest information on third party tools, please visit our Internet site: ➟ http://www.st.com.

IDENTIFICATION	DESCRIPTION
AN913	PWM GENERATION WITH ST62 16-BIT AUTO-RELOAD TIMER
AN914	USING ST626X SPI AS UART
AN1016	ST6 USING THE ST623XB/ST628XB UART
AN1050	ST6 INPUT CAPTURE WITH ST62 16-BIT AUTO-RELOAD TIMER
AN1127	USING THE ST62T6XC/5XC SPI IN MASTER MODE
GENERAL	
AN683	MCUS - 8/16-BIT MICROCONTROLLERS (MCUS) APPLICATION NOTES ABSTRACTS BY TOPICS
AN886	SELECTING BETWEEN ROM AND OTP FOR A MICROCONTROLLER
AN887	MAKING IT EASY WITH MICROCONTROLLERS
AN898	EMC GENERAL INFORMATION
AN899	SOLDERING RECOMMENDATIONS AND PACKAGING INFORMATION
AN900	INTRODUCTION TO SEMICONDUCTOR TECHNOLOGY
AN901	EMC GUIDE-LINES FOR MICROCONTROLLER - BASED APPLICATIONS
AN902	QUALITY AND RELIABILITY INFORMATION
AN912	A SIMPLE GUIDE TO DEVELOPMENT TOOLS
AN1181	ELECTROSTATIC DISHARGE SENSITIVITY MEASUREMENT