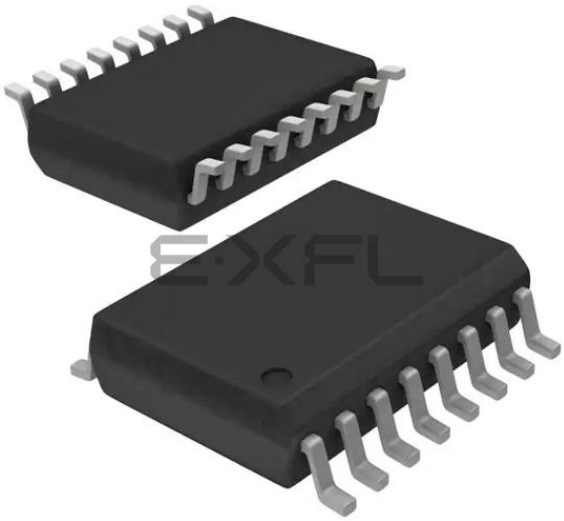

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST6
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	9
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st62t03cm6-tr

Table of Contents

1 INTRODUCTION

The ST6200C, 01C and 03C devices are low cost members of the ST62xx 8-bit HCMOS family of microcontrollers, which is targeted at low to medium complexity applications. All ST62xx devices are based on a building block approach: a common core is surrounded by a number of on-chip peripherals.

The ST62E01C is the erasable EPROM version of the ST62T00C, T01 and T03C devices, which may be used during the development phase for the ST62T00C, T01 and T03C target devices, as well as the respective ST6200C, 01C and 03C ROM devices.

OTP and EPROM devices are functionally identical. OTP devices offer all the advantages of user programmability at low cost, which make them the ideal choice in a wide range of applications where frequent code changes, multiple code versions or last minute programmability are required.

The ROM based versions offer the same functionality, selecting the options defined in the programmable option bytes of the OTP/EPROM versions in the ROM option list (See Section 11.6 on page 92).

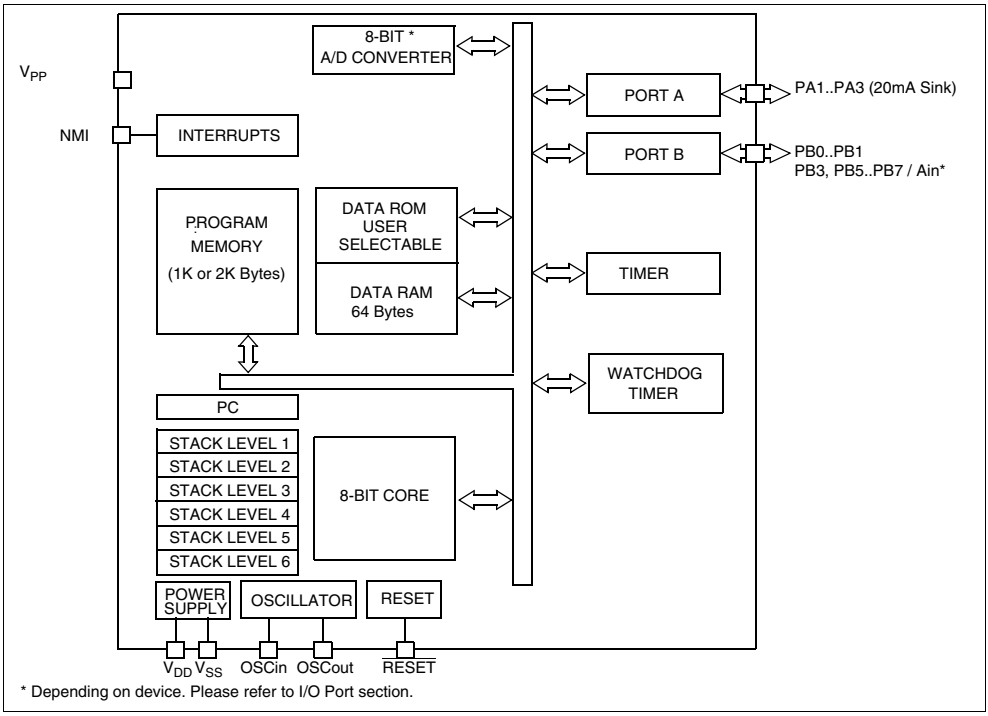
The ST62P00C, P01C and P03C are the **F**actory **A**dvanced **S**ervice **T**echnique ROM (FASTROM) versions of ST62T00C, T01 and T03C OTP devices.

They offer the same functionality as OTP devices, but they do not have to be programmed by the customer (See Section 11 on page 86).

These compact low-cost devices feature a Timer comprising an 8-bit counter with a 7-bit programmable prescaler, an 8-bit A/D Converter with 4 analog inputs (depending on device, see device summary on page 1) and a Digital Watchdog timer, making them well suited for a wide range of automotive, appliance and industrial applications.

For easy reference, all parametric data are located in Section 10 on page 58.

Figure 1. Block Diagram



* Depending on device. Please refer to I/O Port section.

CPU REGISTERS (Cont'd)

The 12-bit length allows the direct addressing of 4096 bytes in Program Space.

However, if the program space contains more than 4096 bytes, the additional memory in program space can be addressed by using the Program ROM Page register.

The PC value is incremented after reading the address of the current instruction. To execute relative jumps, the PC and the offset are shifted through the ALU, where they are added; the result is then shifted back into the PC. The program counter can be changed in the following ways:

– JP (Jump) instruction	PC = Jump address
– CALL instruction	PC = Call address
– Relative Branch Instruction	PC = PC +/- offset
– Interrupt	PC = Interrupt vector
– Reset	PC = Reset vector
– RET & RETI instructions	PC = Pop (stack)
– Normal instruction	PC = PC + 1

Flags (C, Z). The ST6 CPU includes three pairs of flags (Carry and Zero), each pair being associated with one of the three normal modes of operation: Normal mode, Interrupt mode and Non Maskable Interrupt mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during Normal operation, another pair is used during Interrupt mode (CI, ZI), and a third pair is used in the Non Maskable Interrupt mode (CNMI, ZNMI).

The ST6 CPU uses the pair of flags associated with the current mode: as soon as an interrupt (or a Non Maskable Interrupt) is generated, the ST6 CPU uses the Interrupt flags (or the NMI flags) instead of the Normal flags. When the RETI instruction is executed, the previously used set of flags is restored. It should be noted that each flag set can only be addressed in its own context (Non Maskable Interrupt, Normal Interrupt or Main routine). The flags are not cleared during context switching and thus retain their status.

C : Carry flag.

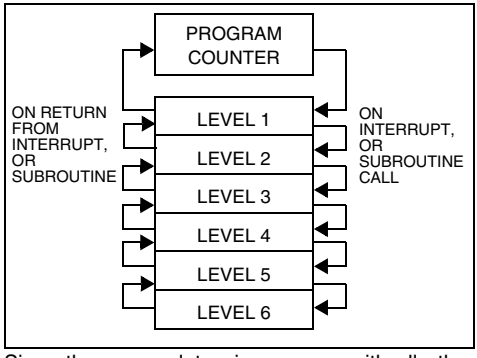
This bit is set when a carry or a borrow occurs during arithmetic operations; otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction; it also participates in the rotate left instruction.
0: No carry has occured
1: A carry has occured

Z : Zero flag
This flag is set if the result of the last arithmetic or logical operation was equal to zero; otherwise it is cleared.
0: The result of the last operation is different from zero
1: The result of the last operation is zero

Switching between the three sets of flags is performed automatically when an NMI, an interrupt or a RETI instruction occurs. As NMI mode is automatically selected after the reset of the MCU, the ST6 core uses the NMI flags first.

Stack. The ST6 CPU includes a true LIFO (Last In First Out) hardware stack which eliminates the need for a stack pointer. The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level are shifted into the next level down, while the content of the PC is shifted into the first level (the original contents of the sixth stack level are lost). When a subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is popped back into the previous level.

Figure 8. Stack manipulation



Since the accumulator, in common with all other data space registers, is not stored in this stack, management of these registers should be performed within the subroutine.

Caution: The stack will remain in its "deepest" position if more than 6 nested calls or interrupts are executed, and consequently the last return address will be lost.

It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

5 CLOCKS, SUPPLY AND RESET

5.1 CLOCK SYSTEM

The main oscillator of the MCU can be driven by any of these clock sources:

– external clock signal

– external AT-cut parallel-resonant crystal

– external ceramic resonator

– external RC network (R_{NET}).

In addition, an on-chip Low Frequency Auxiliary Oscillator (LFAO) is available as a back-up clock system or to reduce power consumption.

An optional Oscillator Safeguard (OSG) filters spikes from the oscillator lines, and switches to the LFAO backup oscillator in the event of main oscillator failure. It also automatically limits the internal clock frequency (f_{INT}) as a function of V_{DD}, in order to guarantee correct operation. These functions are illustrated in Figure 10, and Figure 11.

Table 5 illustrates various possible oscillator configurations using an external crystal or ceramic resonator, an external clock input, an external resistor (R_{NET}), or the lowest cost solution using only the LFAO.

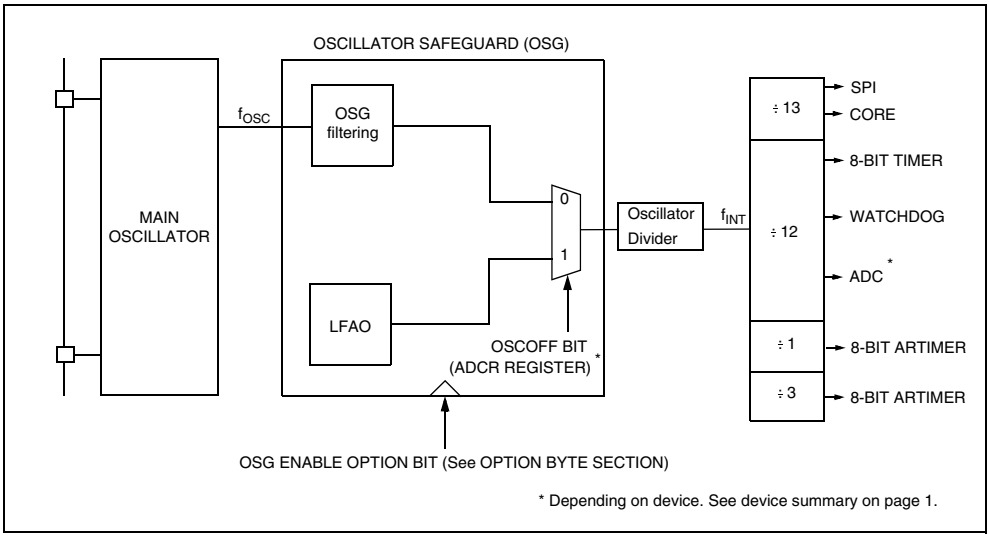
For more details on configuring the clock options, refer to the Option Bytes section of this document.

The internal MCU clock frequency (f_{INT}) is divided by 12 to drive the Timer, the Watchdog timer and the A/D converter, by 13 to drive the CPU core and the SPI and by 1 or 3 to drive the ARTIMER, as shown in Figure 9.

With an 8 MHz oscillator, the fastest CPU cycle is therefore 1.625µs.

A CPU cycle is the smallest unit of time needed to execute any operation (for instance, to increment the Program Counter). An instruction may require two, four, or five CPU cycles for execution.

Figure 9. Clock Circuit Block Diagram



CLOCK SYSTEM (Cont'd)

5.1.2 Oscillator Safeguard (OSG)

The Oscillator Safeguard (OSG) feature is a means of dramatically improving the operational integrity of the MCU. It is available when the OSG ENABLED option is selected in the option byte (refer to the Option Bytes section of this document).

The OSG acts as a filter whose cross-over frequency is device dependent and provides three basic functions:

– Filtering spikes on the oscillator lines which would result in driving the CPU at excessive frequencies

– Management of the Low Frequency Auxiliary Oscillator (LFAO), (useable as low cost internal clock source, backup clock in case of main oscillator failure or for low power consumption)

– Automatically limiting the f_{INT} clock frequency as a function of supply voltage, to ensure correct operation even if the power supply drops.

5.1.2.1 Spike Filtering

Spikes on the oscillator lines result in an effectively increased internal clock frequency. In the absence of an OSG circuit, this may lead to an over frequency for a given power supply voltage. The OSG filters out such spikes (as illustrated in Figure 10). In all cases, when the OSG is active, the maximum internal clock frequency, f_{INT}, is limited to f_{OSG}, which is supply voltage dependent.

5.1.2.2 Management of Supply Voltage Variations

Over-frequency, at a given power supply level, is seen by the OSG as spikes; it therefore filters out some cycles in order that the internal clock frequency of the device is kept within the range the particular device can stand (depending on V_{DD}), and below f_{OSG}: the maximum authorised frequency with OSG enabled.

5.1.2.3 LFAO Management

When the OSG is enabled, the Low Frequency Auxiliary Oscillator can be used (see Section 5.1.3).

Note: The OSG should be used wherever possible as it provides maximum security for the application. It should be noted however, that it can increase power consumption and reduce the maximum operating frequency to f_{OSG} (see Electrical Characteristics section).

Caution: Care has to be taken when using the OSG, as the internal frequency is defined between a minimum and a maximum value and may vary depending on both V_{DD} and temperature. For precise timing measurements, it is not recommended to use the OSG.

Figure 10. OSG Filtering Function

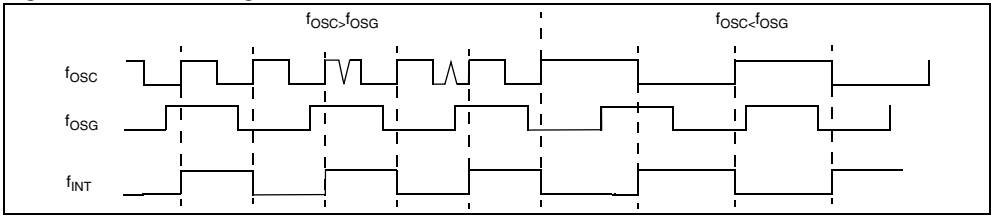
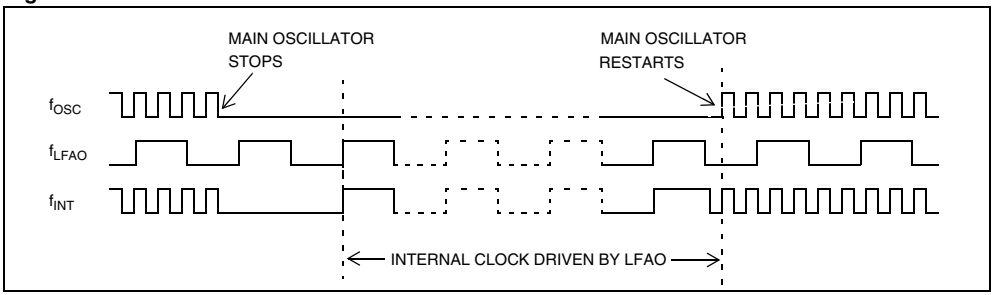


Figure 11. LFAO Oscillator Function



RESET (Cont'd)

5.3.4 Watchdog Reset

The MCU provides a Watchdog timer function in order to be able to recover from software hang-ups. If the Watchdog register is not refreshed before an end-of-count condition is reached, a Watchdog reset is generated.

After a Watchdog reset, the MCU restarts in the same way as if a Reset was generated by the $\overline{\text{RESET}}$ pin.

Note: When a watchdog reset occurs, the $\overline{\text{RESET}}$ pin is tied low for very short time period, to flag the reset phase. This time is not long enough to reset external circuits.

For more details refer to the Watchdog Timer chapter.

5.3.5 LVD Reset

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-On RESET
- Voltage Drop RESET

During an LVD reset, the $\overline{\text{RESET}}$ pin is pulled low when $V_{DD}<V_{IT+}$ (rising edge) or $V_{DD}<V_{IT-}$ (falling edge).

For more details, refer to the LVD chapter.

Caution: Do not externally connect directly the $\overline{\text{RESET}}$ pin to V_{DD}, this may cause damage to the component in case of internal RESET (Watchdog or LVD).

Figure 15. Simple External Reset Circuitry

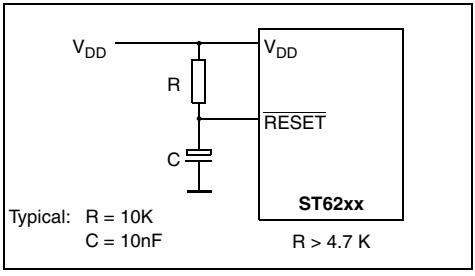
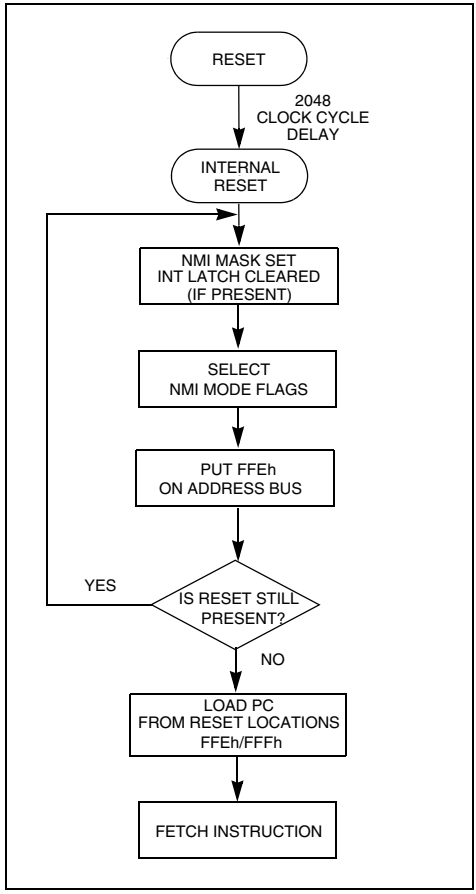


Figure 16. Reset Processing



5.5 INTERRUPT RULES AND PRIORITY MANAGEMENT

- A Reset can interrupt the NMI and peripheral interrupt routines
- The Non Maskable Interrupt request has the highest priority and can interrupt any peripheral interrupt routine at any time but cannot interrupt another NMI interrupt.
- No peripheral interrupt can interrupt another. If more than one interrupt request is pending, these are processed by the processor core according to their priority level: vector #1 has the highest priority while vector #4 the lowest. The priority of each interrupt source is fixed by hardware (see Interrupt Mapping table).

5.6 INTERRUPTS AND LOW POWER MODES

All interrupts cause the processor to exit from WAIT mode. Only the external and some specific interrupts from the on-chip peripherals cause the processor to exit from STOP mode (refer to the “Exit from STOP“ column in the Interrupt Mapping Table).

5.7 NON MASKABLE INTERRUPT

This interrupt is triggered when a falling edge occurs on the NMI pin regardless of the state of the GEN bit in the IOR register. An interrupt request on NMI vector #0 is latched by a flip flop which is automatically reset by the core at the beginning of the NMI service routine.

5.8 PERIPHERAL INTERRUPTS

Different peripheral interrupt flags in the peripheral control registers are able to cause an interrupt when they are active if both:

– The GEN bit of the IOR register is set

– The corresponding enable bit is set in the peripheral control register.

Peripheral interrupts are linked to vectors #3 and #4. Interrupt requests are flagged by a bit in their corresponding control register. This means that a request cannot be lost, because the flag bit must be cleared by user software.

6.3 STOP MODE

STOP mode is the lowest power consumption mode of the MCU (see Figure 22).

The MCU goes into STOP mode as soon as the STOP instruction is executed. This has the following effects:

– Program execution is stopped, the microcontroller can be considered as being “frozen”.

– The contents of RAM and the peripheral registers are kept safely as long as the power supply voltage is higher than the RAM retention voltage.

– The oscillator is stopped, so peripherals cannot work except the those that can be driven by an external clock.

Exit from STOP Mode

The MCU remains in STOP mode until one of the following events occurs:

– RESET (Watchdog, LVD or $\overline{\text{RESET}}$ pin)

– A peripheral interrupt (assuming this peripheral can be driven by an external clock)

– An external interrupt (I/O port, NMI)

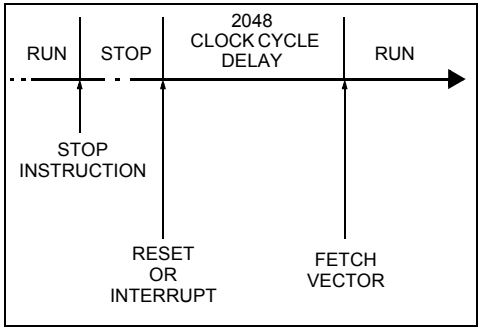
In all cases a delay of 2048 clock cycles (f_{INT}) is generated to make sure the oscillator has started properly.

The Program Counter then points to the starting address of the interrupt or RESET service routine (see Figure 21).

STOP Mode and Watchdog

When the Watchdog is active (hardware or software activation), the STOP instruction is disabled and a WAIT instruction will be executed in its place unless the EXCTNL option bit is set to 1 in the option bytes and a a high level is present on the NMI pin. In this case, the STOP instruction will be executed and the Watchdog will be frozen.

Figure 21. STOP Mode Timing Overview



I/O PORTS (Cont'd)

7.5 REGISTER DESCRIPTION

DATA REGISTER (DR)

Port x Data Register
DRx with x = A or B.

Address DRA: 0C0h - Read/Write
Address DRB: 0C1h - Read/Write

Reset Value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7:0 = **D[7:0]** *Data register bits.*

Reading the DR register returns either the DR register latch content (pin configured as output) or the digital value applied to the I/O pin (pin configured as input).

Caution: In input mode, modifying this register will modify the I/O port configuration (see Table 8).

Do not use the Single bit instructions on I/O port data registers. See (Section 7.2.5).

DATA DIRECTION REGISTER (DDR)

Port x Data Direction Register
DDRx with x = A or B.

Address DDRA: 0C4h - Read/Write
Address DDRB: 0C5h - Read/Write

Reset Value: 0000 0000 (00h)

7							0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Bit 7:0 = **DD[7:0]** *Data direction register bits.*

The DDR register gives the input/output direction configuration of the pins. Each bit is set and cleared by software.
0: Input mode
1: Output mode

OPTION REGISTER (OR)

Port x Option Register
ORx with x = A or B.

Address ORA: 0CCh - Read/Write
Address ORB: 0CDh - Read/Write

Reset Value: 0000 0000 (00h)

7							0
O7	O6	O5	O4	O3	O2	O1	O0

Bit 7:0 = **O[7:0]** *Option register bits.*

The OR register allows to distinguish in output mode if the push-pull or open drain configuration is selected.

Output mode:
0: Open drain output(with P-Buffer deactivated)
1: Push-pull Output

Input mode: See Table 8.

Each bit is set and cleared by software.

Caution: Modifying this register, will also modify the I/O port configuration in input mode. (see Table 8).

Table 10. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Reset Value of all I/O port registers		0	0	0	0	0	0	0	0
0C0h	**DRA**	MSB							LSB
0C1h	**DRB**								
0C4h	**DDRA**	MSB							LSB
0C5h	**DDRB**								
0CCh	**ORA**	MSB							LSB
0CDh	**ORB**								

9 INSTRUCTION SET

9.1 ST6 ARCHITECTURE

The ST6 architecture has been designed for maximum efficiency while keeping byte usage to a minimum; in short, to provide byte-efficient programming. The ST6 core has the ability to set or clear any register or RAM location bit in Data space using a single instruction. Furthermore, programs can branch to a selected address depending on the status of any bit in Data space.

9.2 ADDRESSING MODES

The ST6 has nine addressing modes, which are described in the following paragraphs. Three different address spaces are available: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X, Y, V and W registers, peripheral and Input/Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In direct addressing mode, the address of the byte which is processed by the instruction is stored in the location which follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct. The core can address the four RAM registers X, Y, V, W (locations 80h, 81h, 82h, 83h) in short-direct addressing mode. In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four least significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) which use extended addressing mode are able to branch to any address in the 4 Kbyte Program space.

Extended addressing mode instructions are two bytes long.

Program Counter Relative. Relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations next to the address of the relative instruction. If the condition is not true, the instruction which follows the relative instruction is executed. Relative addressing mode instructions are one byte long. The opcode is obtained by adding the three most significant bits which characterize the test condition, one bit which determines whether it is a forward branch (when it is 0) or backward branch (when it is 1) and the four least significant bits which give the span of the branch (0h to Fh) which must be added or subtracted from the address of the relative instruction to obtain the branch destination address.

Bit Direct. In bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch. Bit test and branch addressing mode is a combination of direct addressing and relative addressing. Bit test and branch instructions are three bytes long. The bit identification and the test condition are included in the opcode byte. The address of the byte to be tested is given in the next byte. The third byte is the jump displacement, which is in the range of -127 to +128. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed to by the content of one of the indirect registers, X or Y (80h, 81h). The indirect register is selected by bit 4 of the opcode. Register indirect instructions are one byte long.

Inherent. In inherent addressing mode, all the information necessary for executing the instruction is contained in the opcode. These instructions are one byte long.

OPERATING CONDITIONS (Cont'd)

10.3.2 Operating Conditions with Low Voltage Detector (LVD)

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IT+}	Reset release threshold (V_{DD} rise)		3.9	4.1	4.3	V
V_{IT-}	Reset generation threshold (V_{DD} fall)		3.6	3.8	4	
V_{hys}	LVD voltage threshold hysteresis	V_{IT+}-V_{IT-}	50	300	700	mV
Vt_{POR}	V_{DD} rise time rate [2]					mV/s
$t_{g(VDD)}$	Filtered glitch delay on V_{DD} [3]	Not detected by the LVD		30		ns

Notes:

1. LVD typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. The minimum V_{DD} rise time rate is needed to insure a correct device power-on and LVD reset. Not tested in production.
3. Data based on characterization results, not tested in production.

Figure 33. LVD Threshold Versus V_{DD} and f_{OSC} [3]

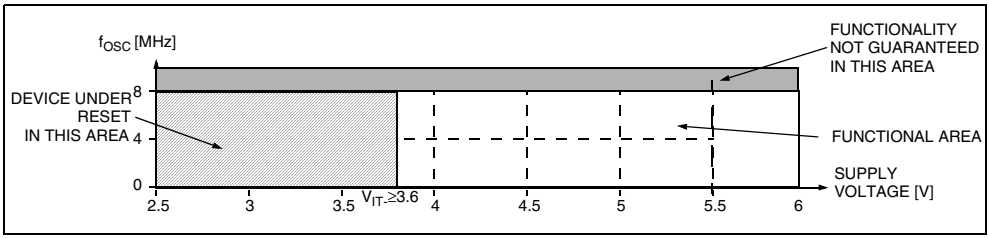


Figure 34. Typical LVD Thresholds Versus Temperature for OTP devices

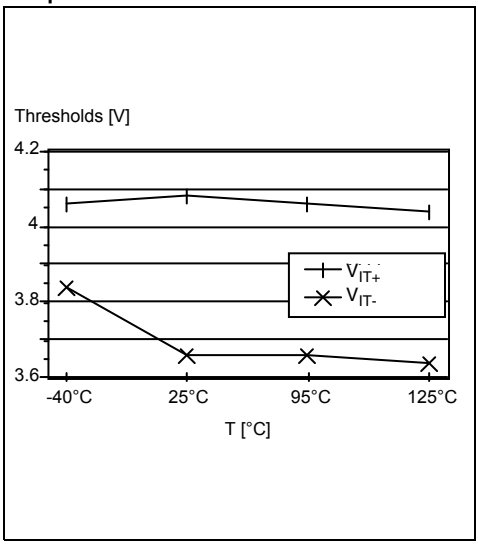
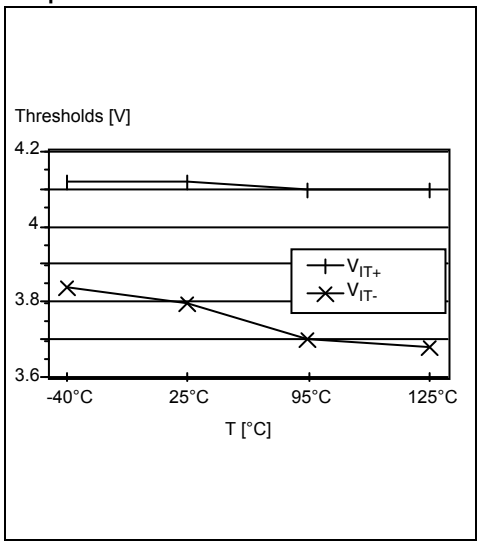


Figure 35. Typical LVD thresholds vs. Temperature for ROM devices



SUPPLY CURRENT CHARACTERISTICS (Cont'd)

10.4.2 WAIT Modes

Symbol	Parameter	Conditions			Typ [1]	Max [2]	Unit
I_{DD}	Supply current in WAIT mode [3] Option bytes not programmed (see Figure 38)	4.5V≤V_{DD}≤6.0V	OTP devices	f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	330 350 370 410 480	550 600 650 700 800	µA
	Supply current in WAIT mode [3] Option bytes programmed to 00H (see Figure 39)			f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	18 26 41 57 70	60 80 120 180 200	
	Supply current in WAIT mode[3] (see Figure 40)		ROM devices	f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	190 210 240 280 350	300 350 400 500 600	
	Supply current in WAIT mode [3] Option bytes not programmed (see Figure 38)	3V≤V_{DD}≤3.6V	OTP devices	f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	80 90 100 120 150	120 140 150 200 250	
	Supply current in WAIT mode [3] Option bytes programmed to 00H (see Figure 39)			f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	5 8 16 18 20	30 40 50 60 100	
	Supply current in WAIT mode [3] Option bytes not programmed (see Figure 40)		ROM devices	f_{OSC}=32kHz f_{OSC}=1MHz f_{OSC}=2MHz f_{OSC}=4MHz f_{OSC}=8MHz	60 65 80 100 130	100 110 120 150 210	

Notes:

1. Typical data are based on T_A=25°C, V_{DD}=5V (4.5V≤V_{DD}≤6.0V range) and V_{DD}=3.3V (3V≤V_{DD}≤3.6V range).
2. Data based on characterization results, tested in production at V_{DD} max. and f_{OSC} max.
3. All I/O pins in input with pull-up mode (no load), all peripherals in reset state; clock input (OSC_{IN}) driven by external square wave, OSG and LVD disabled.

SUPPLY CURRENT CHARACTERISTICS (Cont'd)

10.4.3 STOP Mode

Symbol	Parameter	Conditions	Typ [1]	Max	Unit
I_{DD}	Supply current in STOP mode [2] (see Figure 41 & Figure 42)	OTP devices	0.3	10 [3] 20 [4]	µA
		ROM devices	0.1	2 [3] 20 [4]	

Notes:

1. Typical data are based on V_{DD}=5.0V at T_A=25°C.
2. All I/O pins in input with pull-up mode (no load), all peripherals in reset state, OSG and LVD disabled, option bytes programmed to 00H. Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
3. Maximum STOP consumption for -40°C<Ta<90°C
4. Maximum STOP consumption for -40°C<Ta<125°C

Figure 41. Typical I_{DD} in STOP vs Temperature for OTP devices

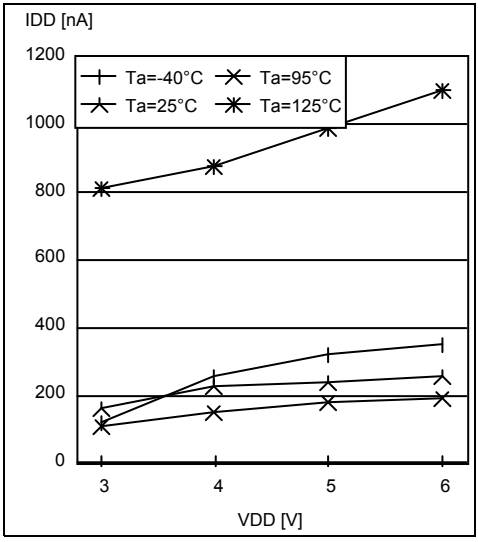
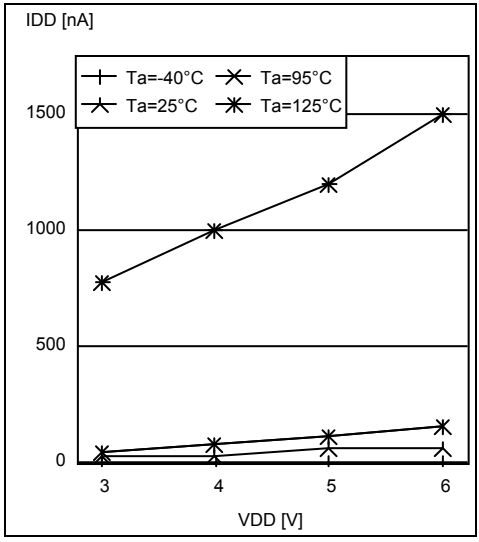


Figure 42. Typical I_{DD} in STOP vs Temperature for ROM devices



10.7 EMC CHARACTERISTICS

Susceptibility tests are performed on a sample basis during product characterization.

10.7.1 Functional EMS

(Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

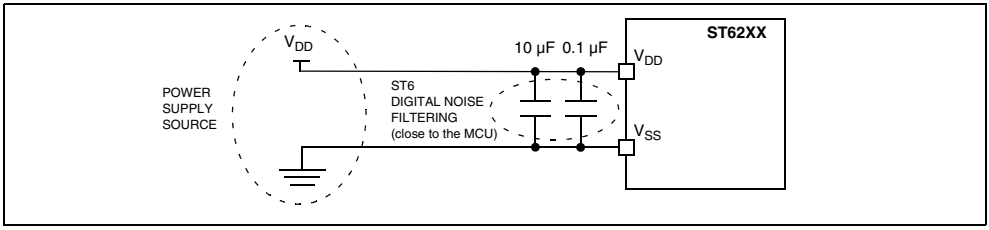
A device reset allows normal operations to be resumed.

Symbol	Parameter	Conditions	Neg [1]	Pos [1]	Unit
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-2	-2	2	kV
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-4	-2.5	3	

Notes:

1. Data based on characterization results, not tested in production.
2. The suggested 10 µF and 0.1 µF decoupling capacitors on the power supply lines are proposed as a good price vs. EMC performance tradeoff. They have to be put as close as possible to the device power supply pins. Other EMC recommendations are given in other sections (I/Os, RESET, OSCx pin characteristics).

Figure 50. EMC Recommended Star Network Power Supply Connection [2]



CONTROL PIN CHARACTERISTICS (Cont'd)

10.10 TIMER PERIPHERAL CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (TIMER).

10.10.1 Watchdog Timer

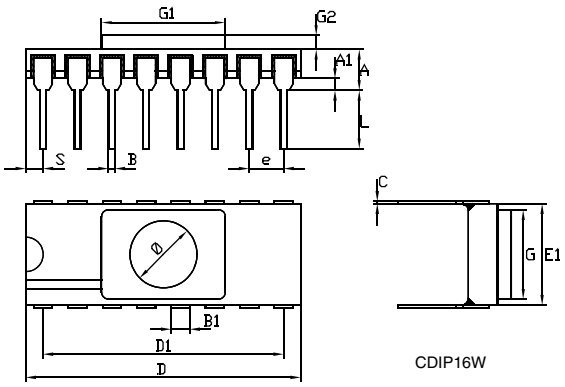
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(WDG)}$	Watchdog time-out duration		3,072		196,608	t_{INT}
		f_{CPU}=4MHz	0.768		49.152	ms
		f_{CPU}=8MHz	0.384		24.576	ms

10.10.2 8-Bit Timer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency		0		$f_{INT}/4$	MHz
t_w	Pulse width at TIMER pin	VDD>4.5V	125			ns
		VDD=3V	1			µs

PACKAGE MECHANICAL DATA (Cont'd)

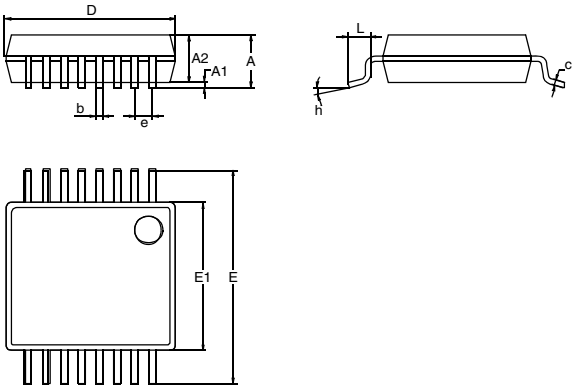
Figure 70. 16-Pin Ceramic Side-Brazed Dual In-Line Package



CDIP16W

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.78			0.149
A1	0.38			0.015		
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.14	1.37	1.78	0.045	0.054	0.070
C	0.20	0.25	0.36	0.008	0.010	0.014
D	19.86	20.32	20.78	0.782	0.800	0.818
D1		17.78			0.700	
E1	7.04	7.49	7.95	0.277	0.295	0.313
e		2.54			0.100	
G	6.35	6.60	6.86	0.250	0.260	0.270
G1	9.47	9.73	9.98	0.373	0.383	0.393
G2		1.02			0.040	
L	2.92	3.30	3.81	0.115	0.130	0.150
S		1.27			0.050	
Ø		4.22			0.166	
	Number of Pins					
N	16					

Figure 71. 16-Pin Plastic Shrink Small Outline Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			2.00			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22		0.38	0.009		0.015
c	0.09		0.25	0.004		0.010
D	5.90	6.20	6.50	0.232	0.244	0.256
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e		0.65			0.026	
θ	0°	4°	8°	0°	4°	8°
L	0.55	0.75	0.95	0.022	0.030	0.037
	Number of Pins					
N	16					

11.3 ECOPACK INFORMATION

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

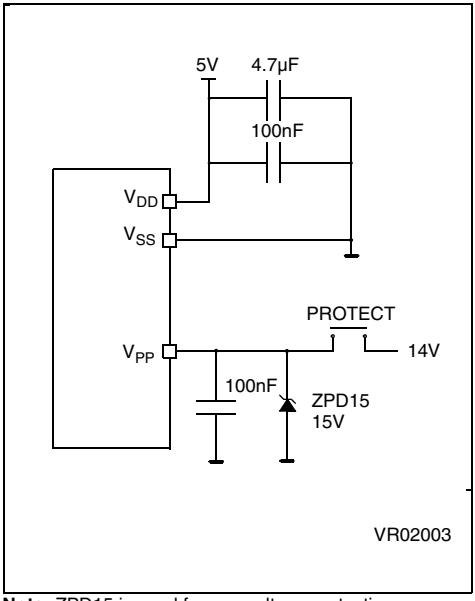
TRANSFER OF CUSTOMER CODE (Cont'd)

11.6.2 ROM VERSION

The ST6200C, 01C and 03C are mask programmed ROM version of ST62T00C, T01 and T03C OTP devices.

They offer the same functionality as OTP devices, selecting as ROM options the options defined in the programmable option byte of the OTP version.

Figure 73. Programming Circuit

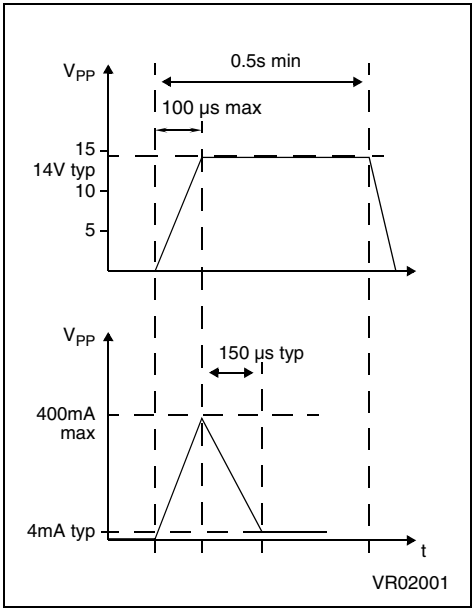


Note: ZPD15 is used for overvoltage protection

ROM Readout Protection. If the ROM READOUT PROTECTION option is selected, a protection fuse can be blown to prevent any access to the program memory content.

In case the user wants to blow this fuse, high voltage must be applied on the V_{PP} pin.

Figure 74. Programming wave form



TRANSFER OF CUSTOMER CODE (Cont'd)

ST6200C/01C/03C/P00C/P01C/P03C MICROCONTROLLER OPTION LIST

Customer: . . . . . .
Address: . . . . . .
. . . . . .
Contact: . . . . . .
Phone: . . . . . .
Reference: . . . . . .

STMicroelectronics references:

Device:
[ ] ST6200C (1 KB) [ ] ST62P00C (1 KB)
[ ] ST6201C (2 KB) [ ] ST62P01C (2 KB)
[ ] ST6203C (1 KB) [ ] ST62P03C (1 KB)

Package:
[ ] Dual in Line Plastic
[ ] Small Outline Plastic with conditioning
[ ] Shrink Small Outline Plastic with conditioning

Conditioning option:
[ ] Standard (Tube)
[ ] Tape & Reel

Temperature Range:
[ ] 0°C to + 70°C [ ] - 40°C to + 85°C
[ ] - 40°C to + 125°C

Marking:
[ ] Standard marking
[ ] Special marking (ROM only):
PDIP16 (9 char. max): _ _ _ _ _ _ _ _ _
SO16 (6 char. max): _ _ _ _ _ _
SSOP16 (10 char. max): _ _ _ _ _ _ _ _ _ _

Authorized characters are letters, digits, '.', '-', '/' and spaces only.

Oscillator Safeguard: [ ] Enabled [ ] Disabled
Watchdog Selection: [ ] Software Activation
[ ] Hardware Activation
NMI pull-up: [ ] Enabled [ ] Disabled
Oscillator Selection: [ ] Quartz crystal / Ceramic resonator
[ ] RC network

Readout Protection:
FASTROM:
[ ] Enabled [ ] Disabled
ROM:
[ ] Enabled:
[ ] Fuse is blown by STMicroelectronics
[ ] Fuse can be blown by the customer
[ ] Disabled

Low Voltage Detector: [ ] Enabled [ ] Disabled
External STOP Mode Control: [ ] Enabled [ ] Disabled
Identifier (FASTROM only): [ ] Enabled [ ] Disabled

Comments:

Oscillator Frequency in the application: . . . . . .
Supply Operating Range in the application: . . . . . .
Notes: . . . . . .
Date: . . . . . .
Signature: . . . . . .

12 DEVELOPMENT TOOLS

STMicroelectronics offers a range of hardware and software development tools for the ST6 microcontroller family. Full details of tools available for the ST6 from third party manufacturers can be obtain from the STMicroelectronics Internet site: ➟ http://www.st.com.

Table 24. Dedicated Third Parties Development Tools

Third Party [1)]	Designation	ST Sales Type	Web site address
ACTUM	ST-REALIZER II: Graphical Schematic based Development available from STMicroelectronics.	STREALIZER-II	http://www.actum.com/
CEIBO	Low cost emulator available from CEIBO.		http://www.ceibo.com/
RAISONANCE	This tool includes in the same environment: an assembler, linker, C compiler, debugger and simulator. The assembler package (plus limited C compiler) is free and can be downloaded from raisonance web site. The full version is available both from STMicroelectronics and Raisonance.	ST6RAIS-SWC/PC	http://www.raisonance.com/
SOFTEC	High end emulator available from SOFTEC.		http://www.softecmicro.com/
	Gang programmer available from SOFTEC.		
ADVANCED EQUIPMENT	Single and gang programmers		http://www.aec.com.tw/
ADVANCED TRANSDATA			http://www.adv-transdata.com/
BP MICROSYSTEMS			http://www.bpmicro.com/
DATA I/O			http://www.data-io.com/
DATAMAN			http://www.dataman.com/
EE TOOLS			http://www.eetools.com/
ELNEC			http://www.elnec.com/
HI-LO SYSTEMS			http://www.hilosystems.com.tw/
ICE TECHNOLOGY			http://www.icetech.com/
LEAP			http://www.leap.com.tw/
LLOYD RESEARCH			http://www.lloyd-research.com/
LOGICAL DEVICES			http://www.chipprogrammers.com/
MQP ELECTRONICS			http://www.mqp.com/
NEEDHAMS ELECTRONICS			http://www.needhams.com/
STAG PROGRAMMERS			http://www.stag.co.uk/
SYSTEM GENERAL CORP			http://www.sg.com.tw
TRIBAL MICROSYSTEMS			http://www.tribalmicro.com/
XELTEK			http://www.xeltek.com/

Note 1: For latest information on third party tools, please visit our Internet site: ➟ http://www.st.com.