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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f63j11t-i-pt

PIC18F85J11 FAMILY

TABLE 1-3: PIC18F6XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0	3	I/O	ST	PORTG is a bidirectional I/O port. Digital I/O.
RG1/TX2/CK2	4	I/O	ST	Digital I/O.
RG1		I/O	ST	Digital I/O.
TX2		O	—	AUSART asynchronous transmit.
CK2		I/O	ST	AUSART synchronous clock (see related RX2/DT2).
RG2/RX2/DT2	5	I/O	ST	Digital I/O.
RG2		I/O	ST	Digital I/O.
RX2		I	ST	AUSART asynchronous receive.
DT2		I/O	ST	AUSART synchronous data (see related TX2/CK2).
RG3	6	I/O	ST	Digital I/O.
RG4	8	I/O	ST	Digital I/O.
VSS	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVSS	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.
ENVREG	18	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP	10	P	—	Core logic power or external filter capacitor connection.
VDDCORE		P	—	Positive supply for microcontroller core logic (regulator disabled).
VCAP		P	—	External filter capacitor connection (regulator enabled).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C™ = I²C/SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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5.5 Configuration Mismatch (CM)

The Configuration Mismatch (CM) Reset is designed to detect and attempt to recover from random, memory corrupting events. These include Electrostatic Discharge (ESD) events, which can cause widespread, single bit changes throughout the device and result in catastrophic failure.

In PIC18FXXJXX Flash devices, the device Configuration registers (located in the configuration memory space) are continuously monitored during operation by comparing their values to complimentary Shadow registers.

If a mismatch is detected between the two sets of registers, a CM Reset automatically occurs. These events are captured by the CM bit (RCON<5>) being set to '0'. This bit does not change for any other Reset event.

A CM Reset behaves similarly to a Master Clear Reset, RESET instruction, WDT time-out or Stack Event Resets. As with all hard and power Reset events, the device Configuration Words are reloaded from the Flash Configuration Words in program memory as the device restarts.

5.6 Power-up Timer (PWRT)

PIC18F85J11 family devices incorporate an on-chip Power-up Timer (PWRT) to help regulate the Power-on Reset process. The PWRT is always enabled. The main function is to ensure that the device voltage is stable before code is executed.

The Power-up Timer (PWRT) of the PIC18F85J11 family devices is an 11-bit counter which uses the INTRC source as the clock input. This yields an approximate time interval of $2048 \times 32 \mu\text{s} = 65.6 \text{ ms}$. While the PWRT is counting, the device is held in Reset.

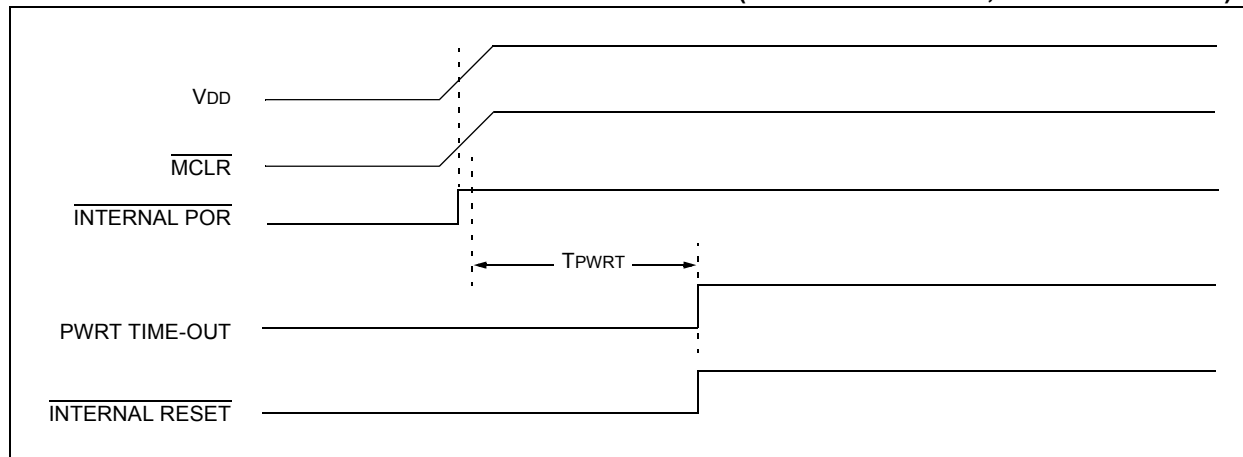
The power-up time delay depends on the INTRC clock and will vary from chip-to-chip due to temperature and process variation. See DC parameter 33 for details.

5.6.1 TIME-OUT SEQUENCE

If enabled, the PWRT time-out is invoked after the POR pulse has cleared. The total time-out will vary based on the status of the PWRT. Figure 5-3, Figure 5-4, Figure 5-5 and Figure 5-6 all depict time-out sequences on power-up with the Power-up Timer enabled.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the PWRT will expire. Bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 5-5). This is useful for testing purposes, or to synchronize more than one PIC18FXXXX device operating in parallel.

FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD} , V_{DD} RISE < T_{PWRT})



8.2 Address and Data Width

The PIC18F85J11 family of devices can be independently configured for different address and data widths on the same memory bus. Both address and data width are set by Configuration bits in the CONFIG3L register. As Configuration bits, this means that these options can only be configured by programming the device and are not controllable in software.

The BW bit selects an 8-bit or 16-bit data bus width. Setting this bit (default) selects a data width of 16 bits.

The EMB<1:0> bits determine both the Program Memory mode and the address bus width. The available options are 20-bit, 16-bit and 12-bit, as well as the default Microcontroller mode (external bus disabled). Selecting a 16-bit or 12-bit width makes a corresponding number of high-order lines available for I/O functions; these pins are no longer affected by the setting of the EBDIS bit. For example, selecting a 16-Bit Address mode (EMB<1:0> = 01) disables A<19:16> and allows PORTH<3:0> to function without interruptions from the bus. Using the smaller address widths allows users to tailor the memory bus to the size of the external memory space for a particular design while freeing up pins for dedicated I/O operation.

Because the EMB bits have the effect of disabling pins for memory bus operations, it is important to always select an address width at least equal to the data width. If a 12-bit address width is used with a 16-bit data width, the upper four bits of data will not be available on the bus.

All combinations of address and data widths require multiplexing of address and data information on the same lines. The address and data multiplexing, as well as I/O ports made available by the use of smaller address widths, are summarized in Table 8-2.

8.2.1 ADDRESS SHIFTING ON THE EXTERNAL BUS

By default, the address presented on the external bus is the value of the PC. In practical terms, this means that addresses in the external memory device below the top of on-chip memory are unavailable to the microcontroller. To access these physical locations, the glue logic between the microcontroller and the external memory must somehow translate addresses.

To simplify the interface, the external bus offers an extension of Extended Microcontroller mode that automatically performs address shifting. This feature is controlled by the EASHFT Configuration bit. Setting this bit offsets addresses on the bus by the size of the microcontroller's on-chip program memory and sets the bottom address at 0000h. This allows the device to use the entire range of physical addresses of the external memory.

8.2.2 21-BIT ADDRESSING

As an extension of 20-bit address width operation, the external memory bus can also fully address a 2-Mbyte memory space. This is done by using the Bus Address bit 0 (BA0) control line as the Least Significant bit of the address. The UB and LB control signals may also be used with certain memory devices to select the upper and lower bytes within a 16-bit wide data word.

This addressing mode is available in both 8-bit and certain 16-Bit Data Width modes. Additional details are provided in **Section 8.6.3 "16-Bit Byte Select Mode"** and **Section 8.7 "8-Bit Data Width Mode"**.

TABLE 8-2: ADDRESS AND DATA LINES FOR DIFFERENT ADDRESS AND DATA WIDTHS

Data Width	Address Width	Multiplexed Data and Address Lines (and Corresponding Ports)	Address-Only Lines (and Corresponding Ports)	Ports Available for I/O
8-bit	12-bit	AD<7:0> (PORTD<7:0>)	AD<11:8> (PORTE<3:0>)	PORTE<7:4>, All of PORTH
	16-bit		AD<15:8> (PORTE<7:0>)	All of PORTH
	20-bit		A<19:16>, AD<15:8> (PORTH<3:0>, PORTE<7:0>)	—
16-bit	16-bit	AD<15:0> (PORTD<7:0>, PORTE<7:0>)	—	All of PORTH
	20-bit		A<19:16> (PORTH<3:0>)	—

8.7 8-Bit Data Width Mode

In 8-Bit Data Width mode, the external memory bus operates only in Multiplexed mode; that is, data shares the 8 Least Significant bits of the address bus.

Figure 8-6 shows an example of 8-Bit Multiplexed mode for 80-pin devices. This mode is used for a single 8-bit memory connected for 16-bit operation. The instructions will be fetched as two 8-bit bytes on a shared data/address bus. The two bytes are sequentially fetched within one instruction cycle (T_{CY}). Therefore, the designer must choose external memory devices according to timing calculations based on $1/2 T_{CY}$ (2 times the instruction rate). For proper memory speed selection, glue logic propagation delay times must be considered, along with setup and hold times.

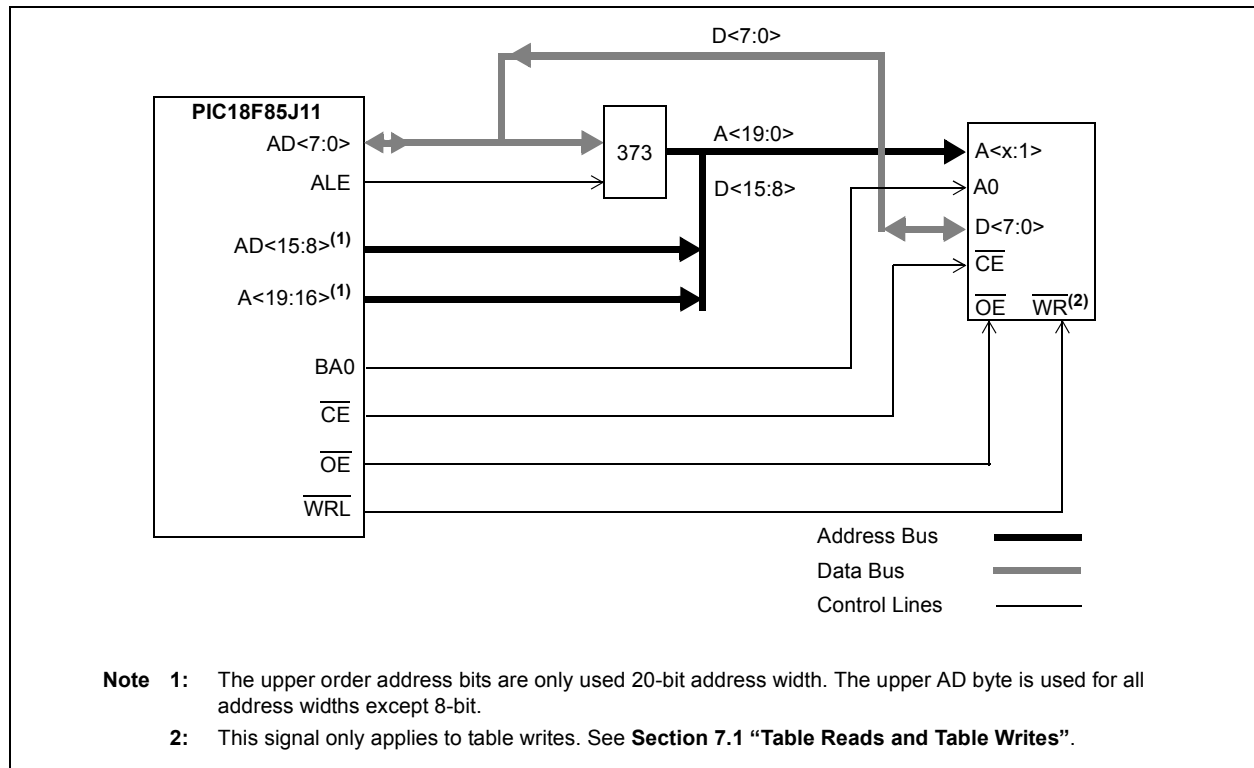
The Address Latch Enable (ALE) pin indicates that the address bits, $AD<15:0>$, are available on the external memory interface bus. The Output Enable signal (\overline{OE})

will enable one byte of program memory for a portion of the instruction cycle, then $BA0$ will change and the second byte will be enabled to form the 16-bit instruction word. The Least Significant bit of the address, $BA0$, must be connected to the memory devices in this mode. The Chip Enable signal (\overline{CE}) is active at any time that the microcontroller accesses external memory, whether reading or writing. It is inactive (asserted high) whenever the device is in Sleep mode.

This generally includes basic EPROM and Flash devices. It allows table writes to byte-wide external memories.

During a $TBLWT$ instruction cycle, the $TABLAT$ data is presented on the upper and lower bytes of the $AD<15:0>$ bus. The appropriate level of the $BA0$ control line is strobed on the LSb of the $TBLPTR$.

FIGURE 8-6: 8-BIT MULTIPLEXED MODE EXAMPLE



10.5 RCON Register

The RCON register contains bits used to determine the cause of the last Reset or wake-up from Idle or Sleep modes. RCON also contains the bit that enables interrupt priorities (IPEN).

REGISTER 10-13: RCON: RESET CONTROL REGISTER

R/W-0	U-0	R/W-1	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	$\overline{\text{CM}}$	$\overline{\text{RI}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	IPEN: Interrupt Priority Enable bit 1 = Enables priority levels on interrupts 0 = Disables priority levels on interrupts (PIC16CXXX Compatibility mode)
bit 6	Unimplemented: Read as '0'
bit 5	CM: Configuration Mismatch Flag bit For details of bit operation, see Register 5-1.
bit 4	RI: RESET Instruction Flag bit For details of bit operation, see Register 5-1.
bit 3	TO: Watchdog Timer Time-out Flag bit For details of bit operation, see Register 5-1.
bit 2	PD: Power-Down Detection Flag bit For details of bit operation, see Register 5-1.
bit 1	POR: Power-on Reset Status bit For details of bit operation, see Register 5-1.
bit 0	BOR: Brown-out Reset Status bit For details of bit operation, see Register 5-1.

13.2 Timer1 16-Bit Read/Write Mode

Timer1 can be configured for 16-bit reads and writes (see Figure 13-2). When the RD16 control bit (T1CON<7>) is set, the address for TMR1H is mapped to a buffer register for the high byte of Timer1. A read from TMR1L will load the contents of the high byte of Timer1 into the Timer1 High Byte Buffer register. This provides the user with the ability to accurately read all 16 bits of Timer1 without having to determine whether a read of the high byte, followed by a read of the low byte, has become invalid due to a rollover between reads.

A write to the high byte of Timer1 must also take place through the TMR1H Buffer register. The Timer1 high byte is updated with the contents of TMR1H when a write occurs to TMR1L. This allows a user to write all 16 bits to both the high and low bytes of Timer1 at once.

The high byte of Timer1 is not directly readable or writable in this mode. All reads and writes must take place through the Timer1 High Byte Buffer register. Writes to TMR1H do not clear the Timer1 prescaler. The prescaler is only cleared on writes to TMR1L.

13.3 Timer1 Oscillator

An on-chip crystal oscillator circuit is incorporated between pins, T1OSI (input) and T1OSO (amplifier output). It is enabled by setting the Timer1 Oscillator Enable bit, T1OSCEN (T1CON<3>). The oscillator is a low-power circuit rated for 32 kHz crystals. It will continue to run during all power-managed modes. The circuit for a typical LP oscillator is shown in Figure 13-3. Table 13-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

FIGURE 13-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR

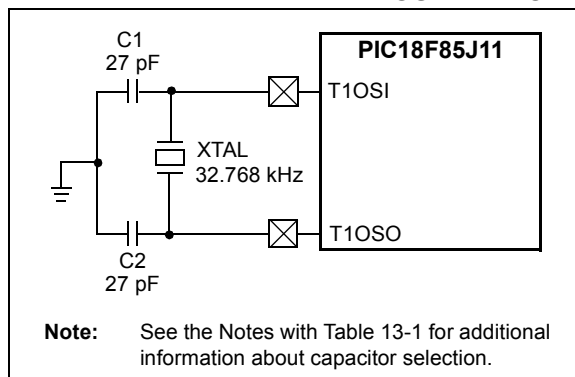


TABLE 13-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR^(2,3,4)

Oscillator Type	Freq.	C1	C2
LP	32.768 kHz	27 pF ⁽¹⁾	27 pF ⁽¹⁾

Note 1: Microchip suggests these values as a starting point in validating the oscillator circuit.

2: Higher capacitance increases the stability of the oscillator but also increases the start-up time.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Capacitor values are for design guidance only.

13.3.1 USING TIMER1 AS A CLOCK SOURCE

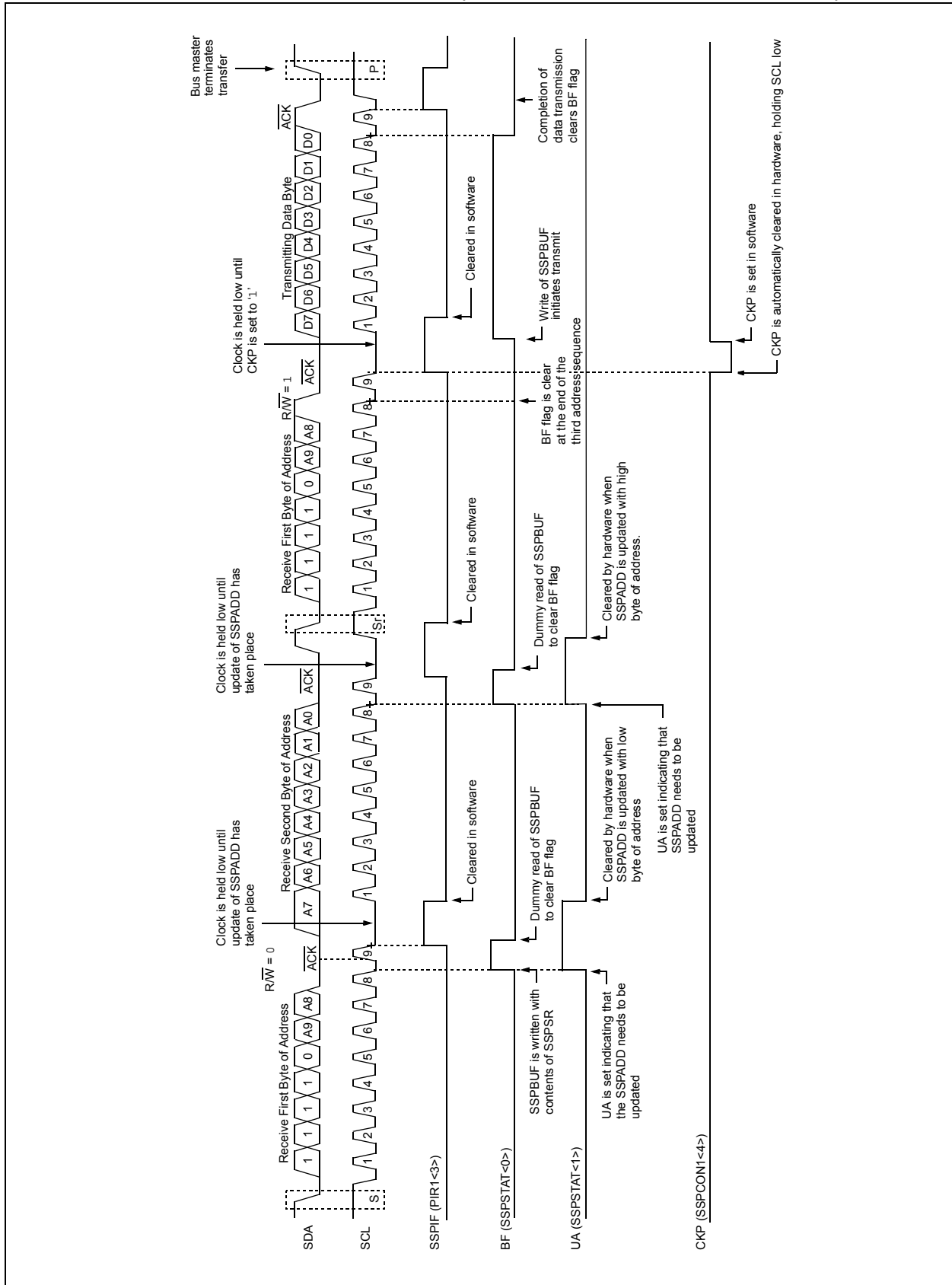
The Timer1 oscillator is also available as a clock source in power-managed modes. By setting the System Clock Select bits, SCS<1:0> (OSCCON<1:0>), to '01', the device switches to SEC_RUN mode; both the CPU and peripherals are clocked from the Timer1 oscillator. If the IDLEN bit (OSCCON<7>) is cleared and a SLEEP instruction is executed, the device enters SEC_IDLE mode. Additional details are available in **Section 4.0 "Power-Managed Modes"**.

Whenever the Timer1 oscillator is providing the clock source, the Timer1 system clock status flag, T1RUN (T1CON<6>), is set. This can be used to determine the controller's current clocking mode. It can also indicate the clock source being currently used by the Fail-Safe Clock Monitor. If the Fail-Safe Clock Monitor is enabled and the Timer1 oscillator fails while providing the clock, polling the T1RUN bit will indicate whether the clock is being provided by the Timer1 oscillator or another source.

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NOTES:

FIGURE 17-13: I²C™ SLAVE MODE TIMING (TRANSMISSION, 10-BIT ADDRESSING)



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17.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

- A low level is sampled on SDA when SCL goes from a low level to a high level.
- SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', see Figure 17-31). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (see Figure 17-32).

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 17-31: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

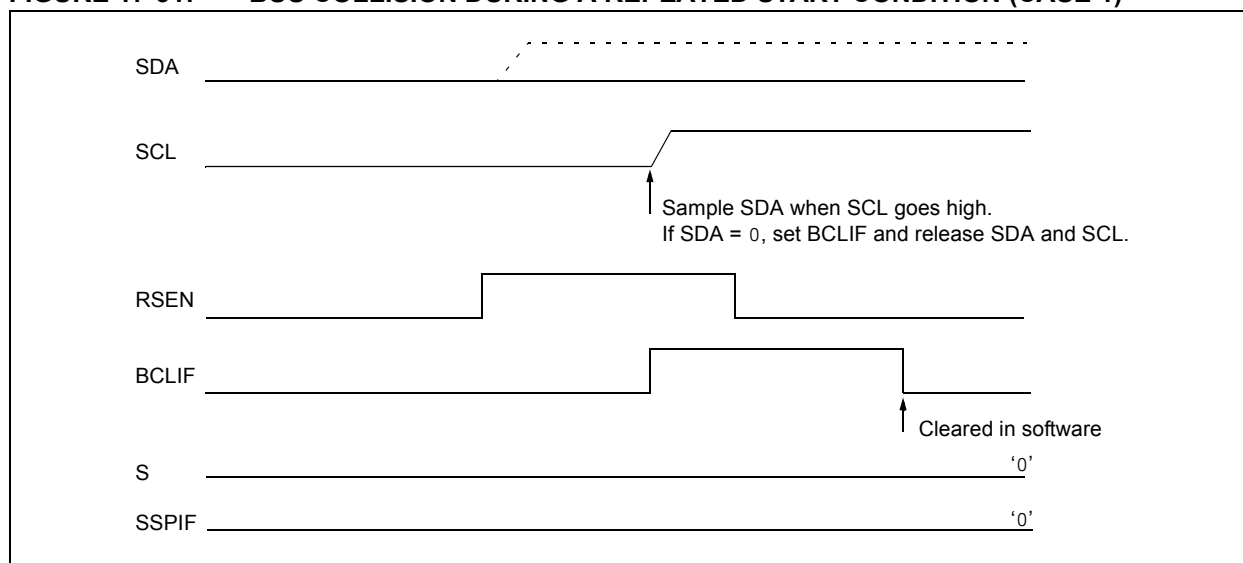
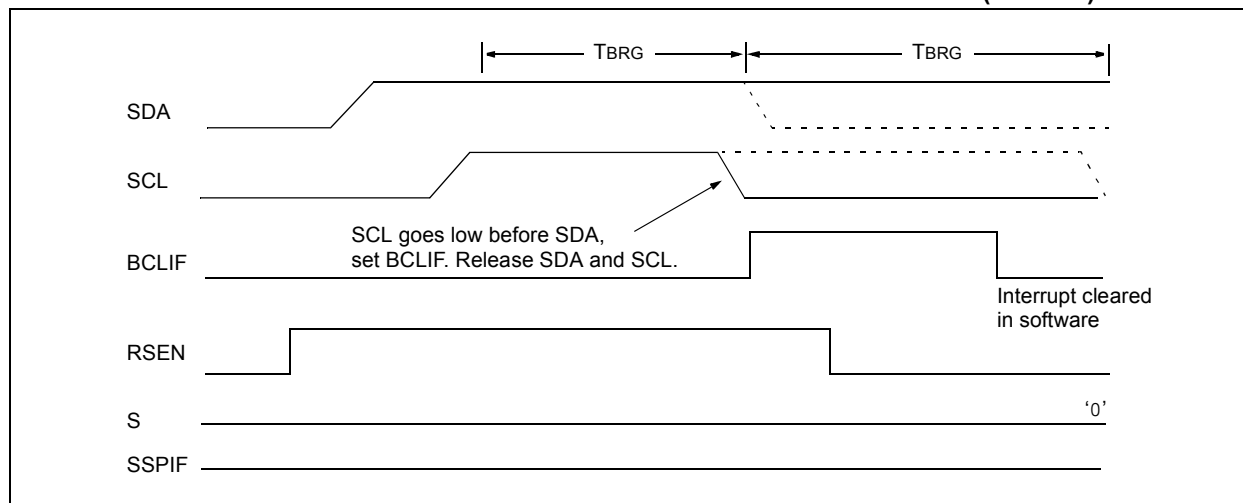


FIGURE 17-32: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



18.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

PIC18F85J11 family devices have three serial I/O modules: the MSSP module, discussed in the previous chapter and two Universal Synchronous Asynchronous Receiver Transmitter (USART) modules. (Generically, the USART is also known as a Serial Communications Interface or SCI.) The EUSART can be configured as a full-duplex, asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers. It can also be configured as a half-duplex, synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc.

There are two distinct implementations of the USART module in these devices: the Enhanced USART (EUSART) discussed here and the Addressable USART discussed in the next chapter. For this device family, USART1 always refers to the EUSART, while USART2 is always the AUSART.

The EUSART and AUSART modules implement the same core features for serial communications; their basic operation is essentially the same. The EUSART module provides additional features, including Automatic Baud Rate Detection and calibration, automatic wake-up on Sync Break reception and 12-bit Break character transmit. These features make it ideally suited for use in Local Interconnect Network bus (LIN/J2602 bus) systems.

The EUSART can be configured in the following modes:

- Asynchronous (full-duplex) with:
 - Auto-wake-up on character reception
 - Auto-baud calibration
 - 12-bit Break character transmission
- Synchronous – Master (half-duplex) with selectable clock polarity
- Synchronous – Slave (half-duplex) with selectable clock polarity

The pins of the EUSART are multiplexed with the functions of PORTC (RC6/TX1/CK1 and RC7/RX1/DT1). In order to configure these pins as a EUSART:

- SPEN bit (RCSTA1<7>) must be set (= 1)
- TRISC<7> bit must be set (= 1)
- TRISC<6> bit must be set (= 1)

Note: The EUSART control will automatically reconfigure the pin from input to output as needed.

The driver for the TX1 output pin can also be optionally configured as an open-drain output. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor, and allows the output to communicate with external circuits without the need for additional level shifters.

The open-drain output option is controlled by the U1OD bit (LATG<6>). Setting the bit configures the pin for open-drain operation.

18.1 Control Registers

The operation of the Enhanced USART module is controlled through three registers:

- Transmit Status and Control Register 1 (TXSTA1)
- Receive Status and Control Register 1 (RCSTA1)
- Baud Rate Control Register 1 (BAUDCON1)

The registers are described in Register 18-1, Register 18-2 and Register 18-3.

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REGISTER 18-1: TXSTA1: EUSART TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN ⁽¹⁾	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)
- bit 6 **TX9:** 9-Bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission
- bit 5 **TXEN:** Transmit Enable bit⁽¹⁾
1 = Transmit is enabled
0 = Transmit is disabled
- bit 4 **SYNC:** AUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode
- bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care.
- bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode.
- bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR is empty
0 = TSR is full
- bit 0 **TX9D:** 9th Bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

PIC18F85J11 FAMILY

REGISTER 18-2: RCSTA1: EUSART RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **SPEN:** Serial Port Enable bit
1 = Serial port is enabled
0 = Serial port is disabled (held in Reset)
- bit 6 **RX9:** 9-Bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception
- bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
Don't care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave:
Don't care.
- bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit, CREN, is cleared (CREN overrides SREN)
0 = Disables continuous receive
- bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode 9-Bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection; all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 9-Bit (RX9 = 0):
Don't care.
- bit 2 **FERR:** Framing Error bit
1 = Framing error (can be cleared by reading the RCREG1 register and receiving the next valid byte)
0 = No framing error
- bit 1 **OERR:** Overrun Error bit
1 = Overrun error (can be cleared by clearing bit, CREN)
0 = No overrun error
- bit 0 **RX9D:** 9th Bit of Received Data
This can be an address/data bit or a parity bit and must be calculated by user firmware.

PIC18F85J11 FAMILY

EXAMPLE 18-1: CALCULATING BAUD RATE ERROR

For a device with FOSC of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

Desired Baud Rate = $F_{OSC}/(64 ([SPBRGH1:SPBRG1] + 1))$

Solving for SPBRGH1:SPBRG1:

$X = ((F_{OSC}/\text{Desired Baud Rate})/64) - 1$

$= ((16000000/9600)/64) - 1$

$= [25.042] = 25$

Calculated Baud Rate = $16000000/(64 (25 + 1))$

$= 9615$

Error = $(\text{Calculated Baud Rate} - \text{Desired Baud Rate})/\text{Desired Baud Rate}$

$= (9615 - 9600)/9600 = 0.16\%$

TABLE 18-2: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	59
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	59
BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	60
SPBRGH1	EUSART Baud Rate Generator Register High Byte								60
SPBRG1	EUSART Baud Rate Generator Register Low Byte								59

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the BRG.

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19.2 AUSART Baud Rate Generator (BRG)

The BRG is a dedicated, 8-bit generator that supports both the Asynchronous and Synchronous modes of the AUSART.

The SPBRG2 register controls the period of a free-running timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, BRGH is ignored. Table 19-1 shows the formula for computation of the baud rate for different AUSART modes, which only apply in Master mode (internally generated clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG2 register can be calculated using the formulas in Table 19-1. From this, the error in baud rate can be determined. An example calculation is shown in Example 19-1. Typical baud rates and error values for the various Asynchronous modes are shown

in Table 19-2. It may be advantageous to use the high baud rate (BRGH = 1) to reduce the baud rate error, or achieve a slow baud rate for a fast oscillator frequency.

Writing a new value to the SPBRG2 register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

19.2.1 OPERATION IN POWER-MANAGED MODES

The device clock is used to generate the desired baud rate. When one of the power-managed modes is entered, the new clock source may be operating at a different frequency. This may require an adjustment to the value in the SPBRG2 register.

19.2.2 SAMPLING

The data on the RX2 pin is sampled three times by a majority detect circuit to determine if a high or low level is present at the RX2 pin.

TABLE 19-1: BAUD RATE FORMULAS

Configuration Bits		BRG/AUSART Mode	Baud Rate Formula
SYNC	BRGH		
0	0	Asynchronous	$F_{osc}/[64 (n + 1)]$
0	1	Asynchronous	$F_{osc}/[16 (n + 1)]$
1	x	Synchronous	$F_{osc}/[4 (n + 1)]$

Legend: x = Don't care, n = Value of SPBRG2 register

EXAMPLE 19-1: CALCULATING BAUD RATE ERROR

For a device with Fosc of 16 MHz, desired baud rate of 9600, Asynchronous mode, BRGH = 0:

Desired Baud Rate = $F_{osc}/(64 ([SPBRG2] + 1))$

Solving for SPBRG2:

$$\begin{aligned} X &= ((F_{osc}/\text{Desired Baud Rate})/64) - 1 \\ &= ((16000000/9600)/64) - 1 \\ &= [25.042] = 25 \end{aligned}$$

Calculated Baud Rate = $16000000/(64 (25 + 1))$
= 9615

Error = $(\text{Calculated Baud Rate} - \text{Desired Baud Rate})/\text{Desired Baud Rate}$
= $(9615 - 9600)/9600 = 0.16\%$

TABLE 19-2: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	61
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	61
SPBRG2	AUSART Baud Rate Generator Register								61

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by the BRG.

FIGURE 19-5: ASYNCHRONOUS RECEPTION

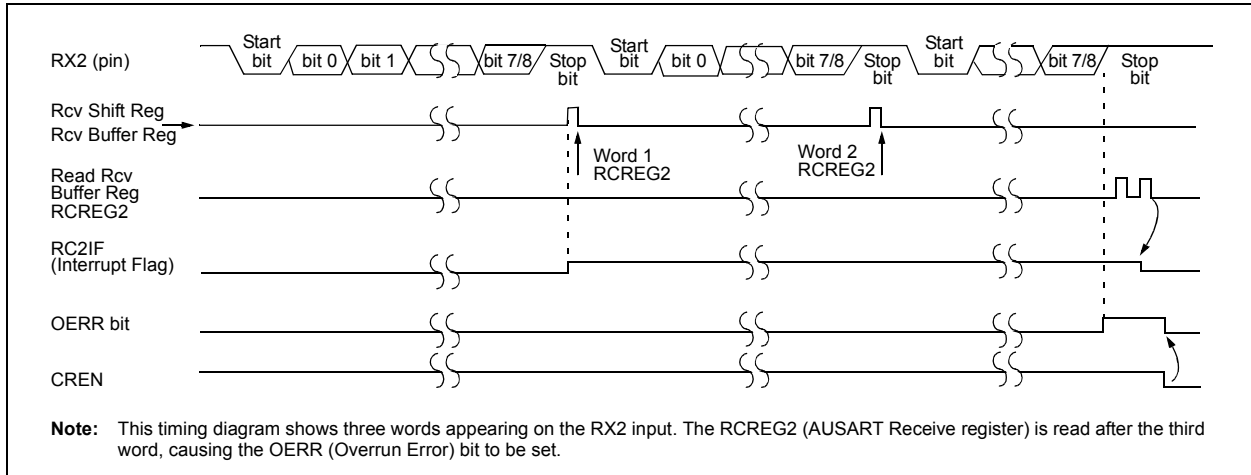


TABLE 19-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR3	—	—	RC2IF	TX2IF	—	CCP2IF	CCP1IF	—	59
PIE3	—	—	RC2IE	TX2IE	—	CCP2IE	CCP1IE	—	59
IPR3	—	—	RC2IP	TX2IP	—	CCP2IP	CCP1IP	—	59
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	61
RCREG2	AUSART Receive Register								61
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	61
SPBRG2	AUSART Baud Rate Generator Register								61

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

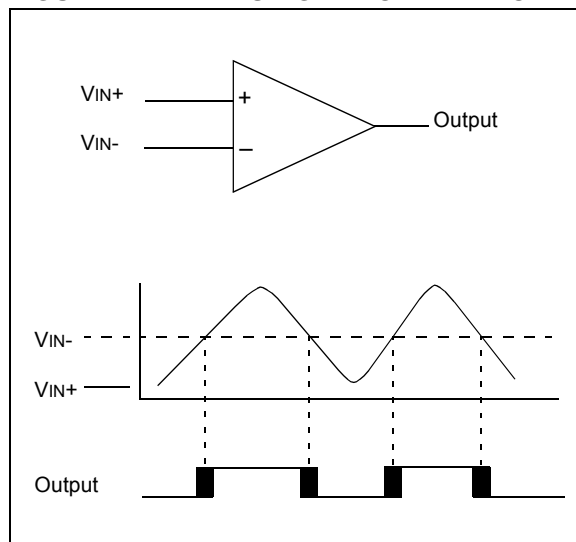
21.2 Comparator Operation

A single comparator is shown in Figure 21-2, along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN+} is less than the analog input V_{IN-} , the output of the comparator is a digital low level. When the analog input at V_{IN+} is greater than the analog input V_{IN-} , the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 21-2 represent the uncertainty due to input offsets and response time.

21.3 Comparator Reference

Depending on the comparator operating mode, either an external or internal voltage reference may be used. The analog signal present at V_{IN-} is compared to the signal at V_{IN+} and the digital output of the comparator is adjusted accordingly (Figure 21-2).

FIGURE 21-2: SINGLE COMPARATOR



21.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between V_{SS} and V_{DD} and can be applied to either pin of the comparator(s).

21.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference from the comparator voltage reference module. This module is described in more detail in **Section 22.0 “Comparator Voltage Reference Module”**.

The internal reference is only available in the mode where four inputs are multiplexed to two comparators ($CM<2:0> = 110$). In this mode, the internal voltage reference is applied to the V_{IN+} pin of both comparators.

21.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (see **Section 26.0 “Electrical Characteristics”**).

21.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RF1 and RF2 I/O pins. When enabled, multiplexors in the output path of the RF1 and RF2 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 21-3 shows the comparator output block diagram.

The TRISF bits will still function as output enables/disables for the RF1 and RF2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits ($CMCON<5:4>$).

- Note 1:** When reading the PORT register, all pins configured as analog inputs will read as ‘0’. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
- 2:** Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

25.0 INSTRUCTION SET SUMMARY

The PIC18F85J11 family of devices incorporate the standard set of 75 PIC18 core instructions, as well as an extended set of 8 new instructions for the optimization of code that is recursive or that utilizes a software stack. The extended set is discussed later in this section.

25.1 Standard Instruction Set

The standard PIC18 instruction set adds many enhancements to the previous PIC[®] MCU instruction sets, while maintaining an easy migration from these PIC MCU instruction sets. Most instructions are a single program memory word (16 bits), but there are four instructions that require two program memory locations.

Each single-word instruction is a 16-bit word divided into an opcode, which specifies the instruction type, and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- **Byte-Oriented** operations
- **Bit-Oriented** operations
- **Literal** operations
- **Control** operations

The PIC18 instruction set summary in Table 25-2 lists **byte-oriented**, **bit-oriented**, **literal** and **control** operations. Table 25-1 shows the opcode field descriptions.

Most **byte-oriented** instructions have three operands:

1. The File Select Register (specified by 'f').
2. The destination of the result (specified by 'd').
3. The accessed memory (specified by 'a').

The File Select Register designator, 'f', specifies which File Select Register is to be used by the instruction. The destination designator, 'd', specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the WREG register. If 'd' is one, the result is placed in the File Select Register specified in the instruction.

All **bit-oriented** instructions have three operands:

1. The File Select Register (specified by 'f').
2. The bit in the File Select Register (specified by 'b').
3. The accessed memory (specified by 'a').

The bit field designator, 'b', selects the number of the bit affected by the operation, while the File Select Register designator, 'f', represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

- A literal value to be loaded into a File Select Register (specified by 'k').
- The desired FSR register to load the literal value into (specified by 'f').
- No operand required (specified by '—').

The **control** instructions may use some of the following operands:

- A program memory address (specified by 'n').
- The mode of the **CALL** or **RETURN** instructions (specified by 's').
- The mode of the table read and table write instructions (specified by 'm').
- No operand required (specified by '—').

All instructions are a single word, except for four double-word instructions. These instructions were made double-word to contain the required information in 32 bits. In the second word, the 4 MSBs are '1's. If this second word is executed as an instruction (by itself), it will execute as a **NOP**.

All single-word instructions are executed in a single instruction cycle unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a **NOP**.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s. Two-word branch instructions (if true) would take 3 μ s.

Figure 25-1 shows the general formats that the instructions can have. All examples use the convention 'nnh' to represent a hexadecimal number.

The instruction set summary, shown in Table 25-2, lists the standard instructions recognized by the Microchip MPASM[™] Assembler.

Section 25.1.1 "Standard Instruction Set" provides a description of each instruction.

PIC18F85J11 FAMILY

MOVLW Move Literal to W

Syntax: MOVLW k

Operands: $0 \leq k \leq 255$

Operation: $k \rightarrow W$

Status Affected: None

Encoding:

0000	1110	kkkk	kkkk
------	------	------	------

Description: The eight-bit literal 'k' is loaded into W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: MOVLW 5Ah

After Instruction
W = 5Ah

MOVWF Move W to f

Syntax: MOVWF f {,a}

Operands: $0 \leq f \leq 255$
 $a \in [0, 1]$

Operation: $(W) \rightarrow f$

Status Affected: None

Encoding:

0110	111a	ffff	ffff
------	------	------	------

Description: Move data from W to register 'f'.
Location 'f' can be anywhere in the 256-byte bank.

If 'a' is '0', the Access Bank is selected.
If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See

Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: MOVWF REG, 0

Before Instruction

W = 4Fh
REG = FFh

After Instruction

W = 4Fh
REG = 4Fh

PIC18F85J11 FAMILY

26.2 DC Characteristics: Power-Down and Supply Current PIC18F85J11 Family (Industrial) (Continued)

PIC18F85J11 Family (Industrial)		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature		-40°C ≤ TA ≤ +85°C for industrial			
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ⁽²⁾						
	All devices	2.8	3.8	mA	-40°C	VDD = 2.0V, VDDCORE = 2.0V ⁽⁴⁾	FOSC = 4 MHz, 16 MHz internal (PRI_RUN mode, HSPLL oscillator)
		3.02	3.8	mA	+25°C		
		3.01	4.5	mA	+85°C		
	All devices	4.5	5.4	mA	-40°C	VDD = 2.5V, VDDCORE = 2.5V ⁽⁴⁾	FOSC = 4 MHz, 16 MHz internal (PRI_RUN mode, HSPLL oscillator)
		4.8	5.6	mA	+25°C		
		4.54	5.6	mA	+85°C		
	All devices	5.72	6.7	mA	-40°C	VDD = 3.3V ⁽⁵⁾	FOSC = 4 MHz, 16 MHz internal (PRI_RUN mode, HSPLL oscillator)
		5.55	6.5	mA	+25°C		
		5.3	6.5	mA	+85°C		
	All devices	7.4	8.5	mA	-40°C	VDD = 2.5V, VDDCORE = 2.5V ⁽⁴⁾	FOSC = 10 MHz, 40 MHz internal (PRI_RUN mode, HSPLL oscillator)
		7.23	8.5	mA	+25°C		
		6.55	7.5	mA	+85°C		
	All devices	9.74	11.6	mA	-40°C	VDD = 3.3V ⁽⁵⁾	FOSC = 10 MHz, 40 MHz internal (PRI_RUN mode, HSPLL oscillator)
		9.43	11.6	mA	+25°C		
		8.89	10.5	mA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} , and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;

MCLR = V_{DD} ; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to $+70^{\circ}\text{C}$. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG tied to V_{SS}).

5: Voltage regulator enabled (ENVREG tied to V_{DD}).

PIC18F85J11 FAMILY

FIGURE 26-6: PROGRAM MEMORY FETCH TIMING DIAGRAM (8-BIT)

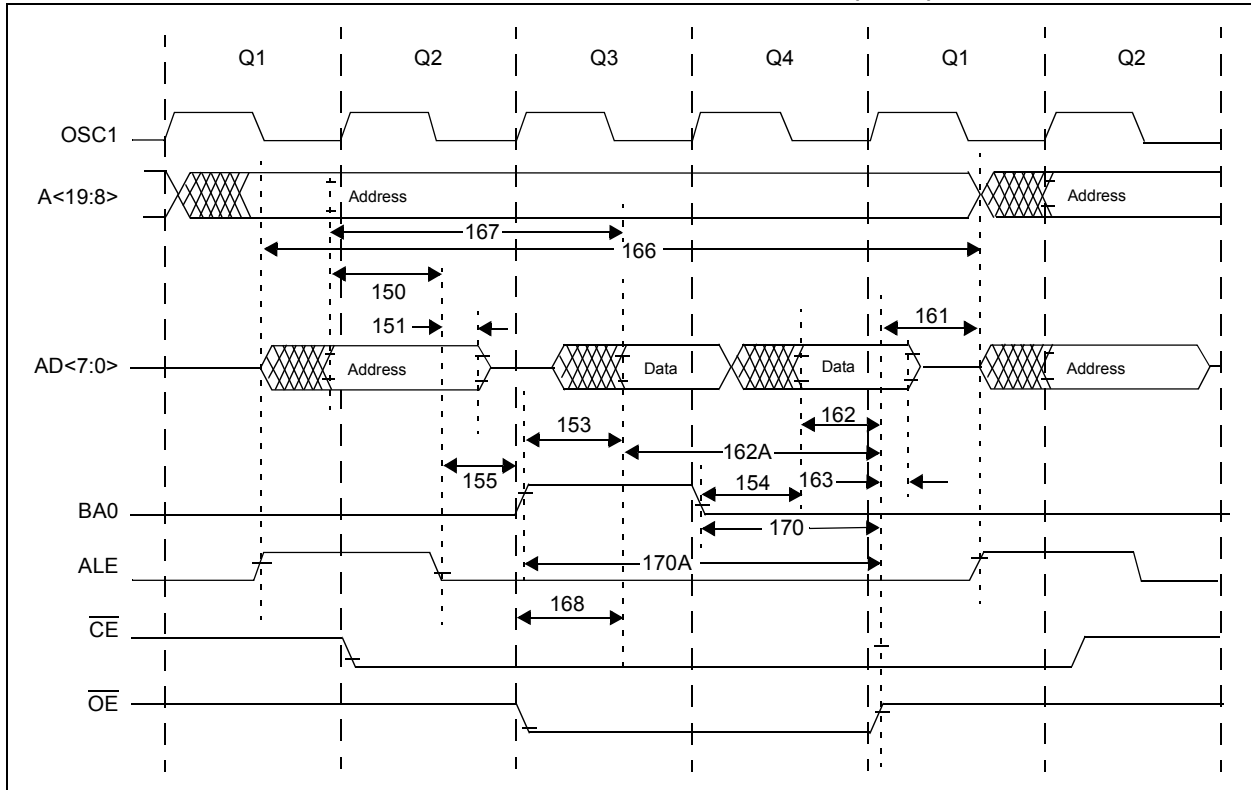


TABLE 26-7: PROGRAM MEMORY FETCH TIMING REQUIREMENTS (8-BIT)

Param No	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2aIL	Address Out Valid to ALE ↓ (address setup time)	0.25 Tcy – 10	—	—	ns
151	TaIL2adI	ALE ↓ to Address Out Invalid (address hold time)	5	—	—	ns
153	BA01	BA0 ↑ to Most Significant Data Valid	0.125 Tcy	—	—	ns
154	BA02	BA0 ↓ to Least Significant Data Valid	0.125 Tcy	—	—	ns
155	TaIL2oeL	ALE ↓ to OE ↓	0.125 Tcy	—	—	ns
161	ToeH2adD	OE ↑ to A/D Driven	0.125 Tcy – 5	—	—	ns
162	TadV2oeH	Least Significant Data Valid Before OE ↑ (data setup time)	20	—	—	ns
162A	TadV2oeH	Most Significant Data Valid Before OE ↑ (data setup time)	0.25 Tcy + 20	—	—	ns
163	ToeH2adI	OE ↑ to Data in Invalid (data Hold Time)	0	—	—	ns
166	TaIH2aIH	ALE ↑ to ALE ↑ (cycle time)	—	Tcy	—	ns
167	TACC	Address Valid to Data Valid	0.5 Tcy – 10	—	—	ns
168	Toe	OE ↓ to Data Valid	—	—	0.125 Tcy + 5	ns
170	TubH2oeH	BA0 = 0 Valid Before OE ↑	0.25 Tcy	—	—	ns
170A	TubL2oeH	BA0 = 1 Valid Before OE ↑	0.5 Tcy	—	—	ns