What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f83j11t-i-pt

TABLE 1-3: PIC18F6XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTG is a bidirectional I/O port.
RG0	3	I/O	ST	Digital I/O.
RG1/TX2/CK2	4			
RG1		I/O	ST	Digital I/O.
TX2		O	—	AUSART asynchronous transmit.
CK2		I/O	ST	AUSART synchronous clock (see related RX2/DT2).
RG2/RX2/DT2	5			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	AUSART asynchronous receive.
DT2		I/O	ST	AUSART synchronous data (see related TX2/CK2).
RG3	6	I/O	ST	Digital I/O.
RG4	8	I/O	ST	Digital I/O.
V_{SS}	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
V_{DD}	26, 38, 57	P	—	Positive supply for logic and I/O pins.
AV_{SS}	20	P	—	Ground reference for analog modules.
AV_{DD}	19	P	—	Positive supply for analog modules.
ENVREG	18	I	ST	Enable for on-chip voltage regulator.
V_{DDCORE}/V_{CAP}	10			Core logic power or external filter capacitor connection.
V_{DDCORE}		P	—	Positive supply for microcontroller core logic (regulator disabled).
V_{CAP}		P	—	External filter capacitor connection (regulator enabled).

Legend: TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; I^2C™ = I^2C/SMBus; CMOS = CMOS compatible input or output; Analog = Analog input; O = Output; OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

TABLE 1-4: PIC18F8XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTG is a bidirectional I/O port.
RG0	5	I/O	ST	Digital I/O.
RG1/TX2/CK2	6			
RG1		I/O	ST	Digital I/O.
TX2		O	—	AUSART asynchronous transmit.
CK2		I/O	ST	AUSART synchronous clock (see related RX2/DT2).
RG2/RX2/DT2	7			
RG2		I/O	ST	Digital I/O.
RX2		I	ST	AUSART asynchronous receive.
DT2		I/O	ST	AUSART synchronous data (see related TX2/CK2).
RG3	8	I/O	ST	Digital I/O.
RG4	10	I/O	ST	Digital I/O.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); I²C™ = I²C/SMBus

Note 1: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared (80-pin devices, Extended Microcontroller mode only).

2: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

3: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as V_{DD}, V_{SS}, AV_{DD} and AV_{SS}, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF.

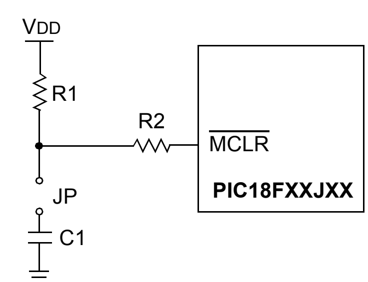
2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to V_{DD} may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS



Note 1: R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.

2: R2 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin V_{IH} and V_{IL} specifications are met.

REGISTER 3-2: OSCTUNE: OSCILLATOR TUNING REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTSRC	PLLEN(1)	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **INTSRC:** Internal Oscillator Low-Frequency Source Select bit
1 = 31.25 kHz device clock derived from 8 MHz INTOSC source (divide-by-256 enabled)
0 = 31 kHz device clock derived from INTRC 31 kHz oscillator

bit 6 **PLLEN:** Frequency Multiplier PLL Enable bit(1)
1 = PLL is enabled
0 = PLL is disabled

bit 5-0 **TUN<5:0>:** Fast RC Oscillator (INTOSC) Frequency Tuning bits
011111 = Maximum frequency
• •
• •
000001
000000 = Center frequency. Fast RC oscillator is running at the calibrated frequency.
111111
• •
• •
100000 = Minimum frequency

Note 1: Available only for ECPLL and HSPLL oscillator configurations; otherwise, this bit is unavailable and reads as ‘0’.

3.3 Clock Sources and Oscillator Switching

Essentially, PIC18F85J11 family devices have three independent clock sources:

- Primary oscillators
- Secondary oscillators
- Internal oscillator

The **primary oscillators** can be thought of as the main device oscillators. These are any external oscillators connected to the OSC1 and OSC2 pins, and include the External Crystal and Resonator modes and the External Clock modes. In some circumstances, the internal oscillator block may be considered a primary oscillator. The particular mode is defined by the FOSC Configuration bits. The details of these modes are covered in **Section 3.4 “External Oscillator Modes”**.

The **secondary oscillators** are external clock sources that are not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power-managed mode. PIC18F85J11 family devices offer the Timer1 oscillator as a secondary oscillator source. This oscillator, in all power-managed modes, is often the time base for functions such as a Real-Time Clock. The Timer1 oscillator is discussed in greater detail in **Section 13.3 “Timer1 Oscillator”**

In addition to being a primary clock source in some circumstances, the **internal oscillator** is available as a power-managed mode clock source. The INTRC source is also used as the clock source for several special features, such as the WDT and Fail-Safe Clock Monitor. The internal oscillator block is discussed in more detail in **Section 3.5 “Internal Oscillator Block”**.

The PIC18F85J11 family includes features that allow the device clock source to be switched from the main oscillator, chosen by device configuration, to one of the alternate clock sources. When an alternate clock source is enabled, various power-managed operating modes are available.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{MCLR}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
TOSU	PIC18F6XJ11	PIC18F8XJ11	---0 0000	---0 0000	---0 uuuu(1)
TOSH	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu(1)
TOSL	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu(1)
STKPTR	PIC18F6XJ11	PIC18F8XJ11	uu-0 0000	00-0 0000	uu-u uuuu(1)
PCLATU	PIC18F6XJ11	PIC18F8XJ11	---0 0000	---0 0000	---u uuuu
PCLATH	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu
PCL	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	PC + 2(2)
TBLPTRU	PIC18F6XJ11	PIC18F8XJ11	--00 0000	--00 0000	--uu uuuu
TBLPTRH	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu
TABLAT	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu
PRODH	PIC18F6XJ11	PIC18F8XJ11	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	PIC18F6XJ11	PIC18F8XJ11	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	PIC18F6XJ11	PIC18F8XJ11	0000 000x	0000 000u	uuuu uuuu(3)
INTCON2	PIC18F6XJ11	PIC18F8XJ11	1111 1111	1111 1111	uuuu uuuu(3)
INTCON3	PIC18F6XJ11	PIC18F8XJ11	1100 0000	1100 0000	uuuu uuuu(3)
INDF0	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
POSTINC0	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
POSTDEC0	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
PREINC0	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
PLUSW0	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
FSR0H	PIC18F6XJ11	PIC18F8XJ11	---- xxxx	---- uuuu	---- uuuu
FSR0L	PIC18F6XJ11	PIC18F8XJ11	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	PIC18F6XJ11	PIC18F8XJ11	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
POSTINC1	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
POSTDEC1	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
PREINC1	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A
PLUSW1	PIC18F6XJ11	PIC18F8XJ11	N/A	N/A	N/A

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as ‘0’, q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

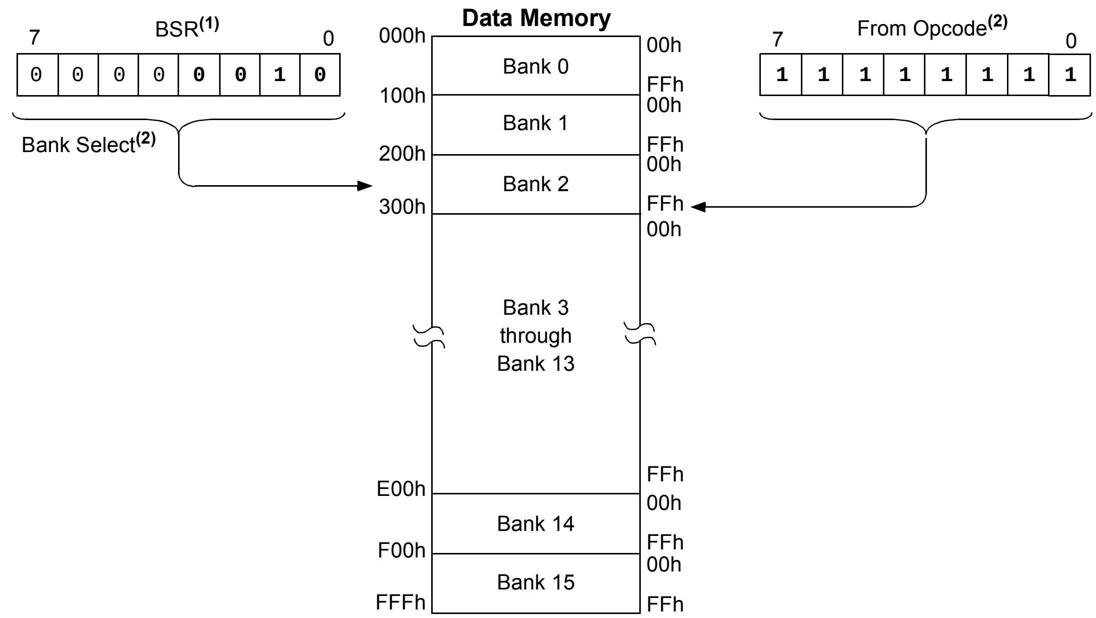
2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read as ‘0’.

FIGURE 6-9: USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)



Note 1: The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.

2: The `MOVFF` instruction embeds the entire 12-bit address in the instruction.

6.3.2 ACCESS BANK

While the use of the BSR with an embedded 8-bit address allows users to address the entire range of data memory, it also means that the user must always ensure that the correct bank is selected. Otherwise, data may be read from, or written to, the wrong location. This can be disastrous if a GPR is the intended target of an operation, but an SFR is written to instead. Verifying and/or changing the BSR for each read or write to data memory can become very inefficient.

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (00h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Bank 15. The lower half is known as the "Access RAM" and is composed of GPRs. The upper half is where the device's SFRs are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed in a linear fashion by an 8-bit address (Figure 6-7).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the 'a' parameter in the instruction). When 'a' is equal to '`1`', the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When 'a' is '`0`', however, the instruction is forced to use the Access Bank address map; the current value of the BSR is ignored entirely.

Using this "forced" addressing allows the instruction to operate on a data address in a single cycle without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables. Access RAM also allows for faster and more code efficient context saving and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = `1`). This is discussed in more detail in **Section 6.6.3 "Mapping the Access Bank in Indexed Literal Offset Mode"**.

6.3.3 GENERAL PURPOSE REGISTER FILE

PIC18 devices may have banked memory in the GPR area. This is data RAM which is available for use by all instructions. GPRs start at the bottom of Bank 0 (address 000h) and grow upwards towards the bottom of the SFR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

8.6.2 16-BIT WORD WRITE MODE

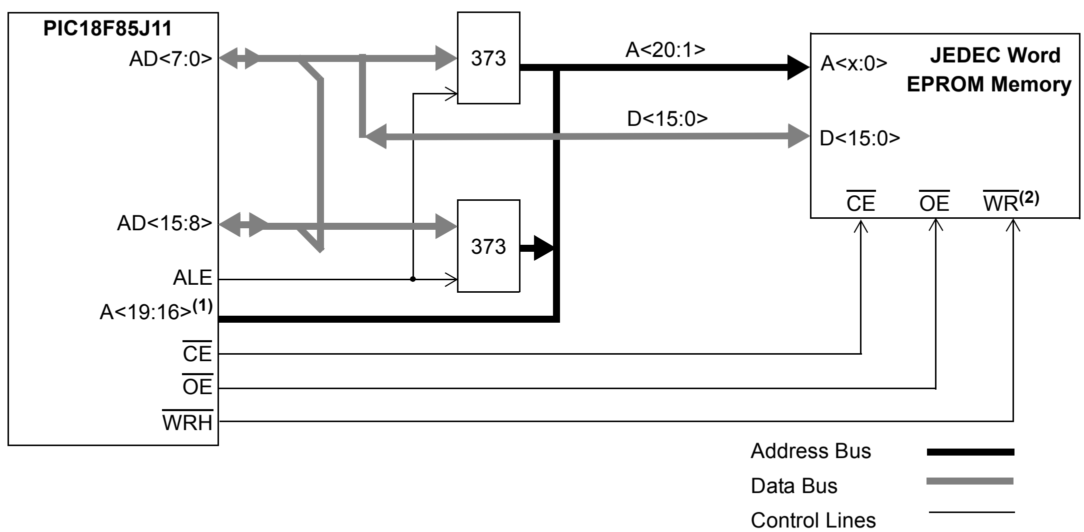
Figure 8-2 shows an example of 16-Bit Word Write mode for PIC18F85J11 family devices. This mode is used for word-wide memories which include some of the EPROM and Flash-type memories. This mode allows opcode fetches and table reads from all forms of 16-bit memory and table writes to any type of word-wide external memories. This method makes a distinction between `TBLWT` cycles to even or odd addresses.

During a `TBLWT` cycle to an even address (TBLPTR<0> = `0`), the TABLAT data is transferred to a holding latch and the external address data bus is tri-stated for the data portion of the bus cycle. No write signals are activated.

During a `TBLWT` cycle to an odd address (TBLPTR<0> = `1`), the TABLAT data is presented on the upper byte of the AD<15:0> bus. The contents of the holding latch are presented on the lower byte of the AD<15:0> bus.

The $\overline{\text{WRH}}$ signal is strobed for each write cycle; the $\overline{\text{WRL}}$ pin is unused. The signal on the BA0 pin indicates the LSb of the TBLPTR, but it is left unconnected. Instead, the $\overline{\text{UB}}$ and $\overline{\text{LB}}$ signals are active to select both bytes. The obvious limitation to this method is that the table write must be done in pairs on a specific word boundary to correctly write a word location.

FIGURE 8-2: 16-BIT WORD WRITE MODE EXAMPLE



Note 1: The upper order address lines are used only for 20-bit address widths.

2: This signal only applies to table writes. See **Section 7.1 "Table Reads and Table Writes"**.

11.10 PORTJ, TRISJ and LATJ Registers

Note:	PORTJ is available only on 80-pin devices.

PORTJ is an 8-bit wide, bidirectional port. The corresponding Data Direction and Output Latch registers are TRISJ and LATJ. All pins on PORTJ are digital only and tolerate voltages up to 5.5V.

All pins on PORTJ are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note:	These pins are configured as digital inputs on any device Reset.

Each of the PORTJ pins has a weak internal pull-up. The pull-ups are provided to keep the inputs at a known state for the external memory interface while powering up. A single control bit can turn off all the pull-ups. This is performed by clearing bit, RJPU (PORTG<5>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on any device Reset.

When the external memory interface is enabled, all of the PORTJ pins function as control outputs for the interface. This occurs automatically when the interface is enabled by clearing the EBDIS control bit (MEMCON<7>). The TRISJ bits are also overridden.

EXAMPLE 11-9: INITIALIZING PORTJ

```
CLRF    PORTJ   ; Initialize PORTJ by
                ; clearing output latches
CLRF    LATJ    ; Alternate method
                ; to clear output latches
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISJ   ; Set RJ3:RJ0 as inputs
                ; RJ5:RJ4 as output
                ; RJ7:RJ6 as inputs
```


17.3.2 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON1<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSPBUF register. Then, the Buffer Full detect bit, BF (SSPSTAT<0>), and the MSSP Interrupt Flag bit, SSPIF, are set. This double-buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision detect bit, WCOL (SSPCON1<7>), will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. The Buffer Full bit, BF (SSPSTAT<0>), indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 17-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPBUF register. Additionally, the SSPSTAT register indicates the various status conditions.

Note:	To avoid lost data in Master mode, a read of the SSPBUF must be performed to clear the Buffer Full (BF) detect bit (SSPSTAT<0>) between each transmission.

EXAMPLE 17-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
LOOP    BTFSS   SSPSTAT, BF     ;Has data been received (transmit complete)?
        BRA     LOOP            ;No
        MOVF    SSPBUF, W       ;WREG reg = contents of SSPBUF
        MOVWF   RXDATA          ;Save in user RAM, if data is meaningful
        MOVF    TXDATA, W       ;W reg = contents of TXDATA
        MOVWF   SSPBUF          ;New data to xmit
```


17.3.7 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit (SSPCON1<4>).

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from Sleep.

17.3.8 SLAVE SELECT SYNCHRONIZATION

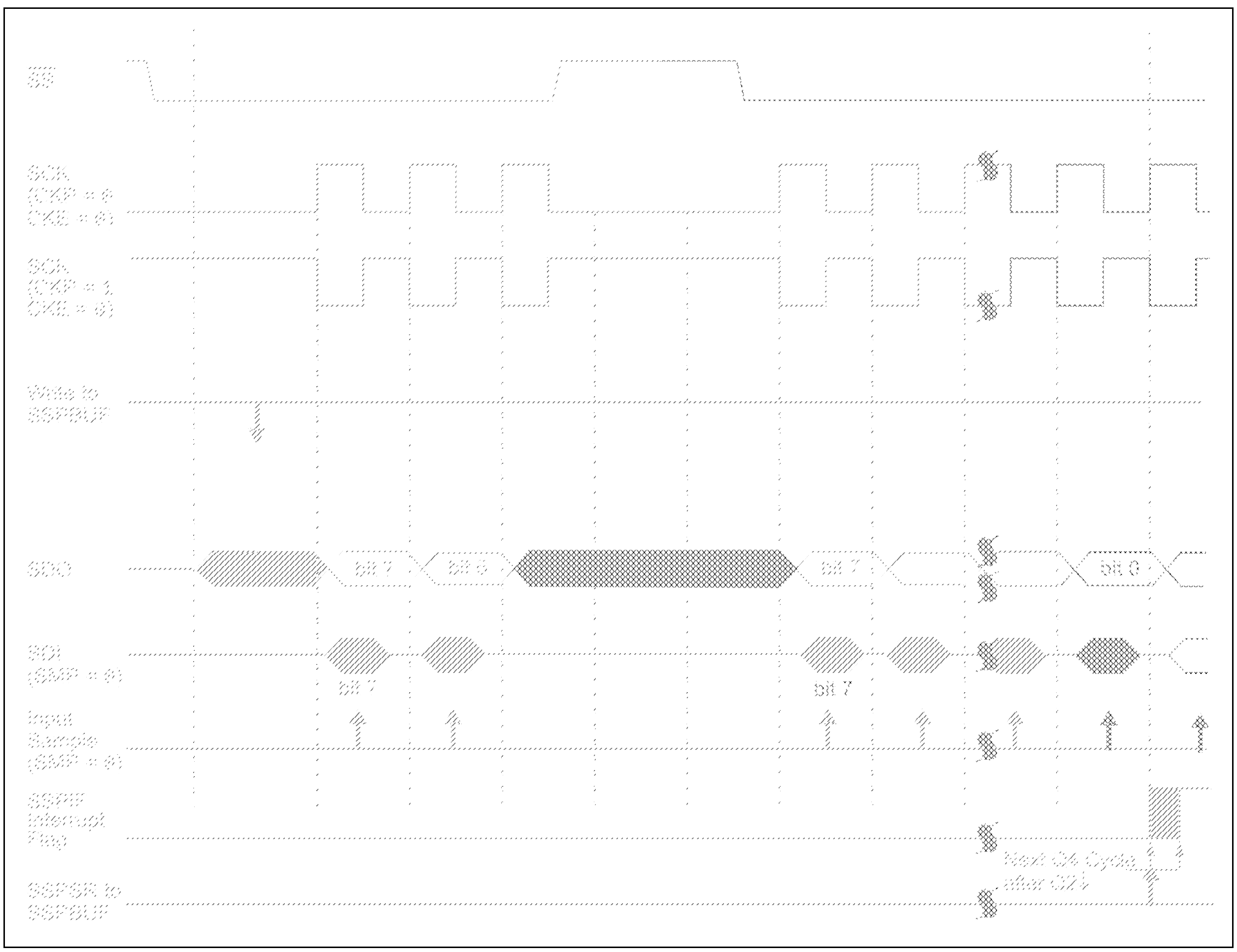
The $\overline{\text{SS}}$ pin allows a Synchronous Slave mode. The SPI must be in Slave mode with $\overline{\text{SS}}$ pin control enabled (SSPCON1<3:0> = 04h). When the $\overline{\text{SS}}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{\text{SS}}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1:	When the SPI is in Slave mode with $\overline{\text{SS}}$ pin control enabled (SSPCON1<3:0> = `0100`), the SPI module will reset if the $\overline{\text{SS}}$ pin is set to VDD.
2:	If the SPI is used in Slave mode with CKE set, then the $\overline{\text{SS}}$ pin control must be enabled.

When the SPI module resets, the bit counter is forced to ‘`0`’. This can be done by either forcing the $\overline{\text{SS}}$ pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

FIGURE 17-4: SLAVE SYNCHRONIZATION WAVEFORM



19.2 AUSART Baud Rate Generator (BRG)

The BRG is a dedicated, 8-bit generator that supports both the Asynchronous and Synchronous modes of the AUSART.

The SPBRG2 register controls the period of a free-running timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, BRGH is ignored. Table 19-1 shows the formula for computation of the baud rate for different AUSART modes, which only apply in Master mode (internally generated clock).

Given the desired baud rate and FOSC, the nearest integer value for the SPBRG2 register can be calculated using the formulas in Table 19-1. From this, the error in baud rate can be determined. An example calculation is shown in Example 19-1. Typical baud rates and error values for the various Asynchronous modes are shown in Table 19-2. It may be advantageous to use the high baud rate (BRGH = 1) to reduce the baud rate error, or achieve a slow baud rate for a fast oscillator frequency.

Writing a new value to the SPBRG2 register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

19.2.1 OPERATION IN POWER-MANAGED MODES

The device clock is used to generate the desired baud rate. When one of the power-managed modes is entered, the new clock source may be operating at a different frequency. This may require an adjustment to the value in the SPBRG2 register.

19.2.2 SAMPLING

The data on the RX2 pin is sampled three times by a majority detect circuit to determine if a high or low level is present at the RX2 pin.

TABLE 19-1: BAUD RATE FORMULAS

Configuration Bits		BRG/AUSART Mode	Baud Rate Formula
SYNC	BRGH		
0	0	Asynchronous	FOSC/[64 (n + 1)]
0	1	Asynchronous	FOSC/[16 (n + 1)]
1	x	Synchronous	FOSC/[4 (n + 1)]

Legend: x = Don't care, n = Value of SPBRG2 register

EXAMPLE 19-1: CALCULATING BAUD RATE ERROR

For a device with FOSC of 16 MHz, desired baud rate of 9600, Asynchronous mode, BRGH = 0:

Desired Baud Rate = FOSC/(64 ([SPBRG2] + 1))

Solving for SPBRG2:

X = ((FOSC/Desired Baud Rate)/64) – 1
= ((16000000/9600)/64) – 1
= [25.042] = 25

Calculated Baud Rate = 16000000/(64 (25 + 1))
= 9615

Error = (Calculated Baud Rate – Desired Baud Rate)/Desired Baud Rate
= (9615 – 9600)/9600 = 0.16%

TABLE 19-2: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	61
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	61
SPBRG2	AUSART Baud Rate Generator Register								61

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by the BRG.

FIGURE 19-7: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

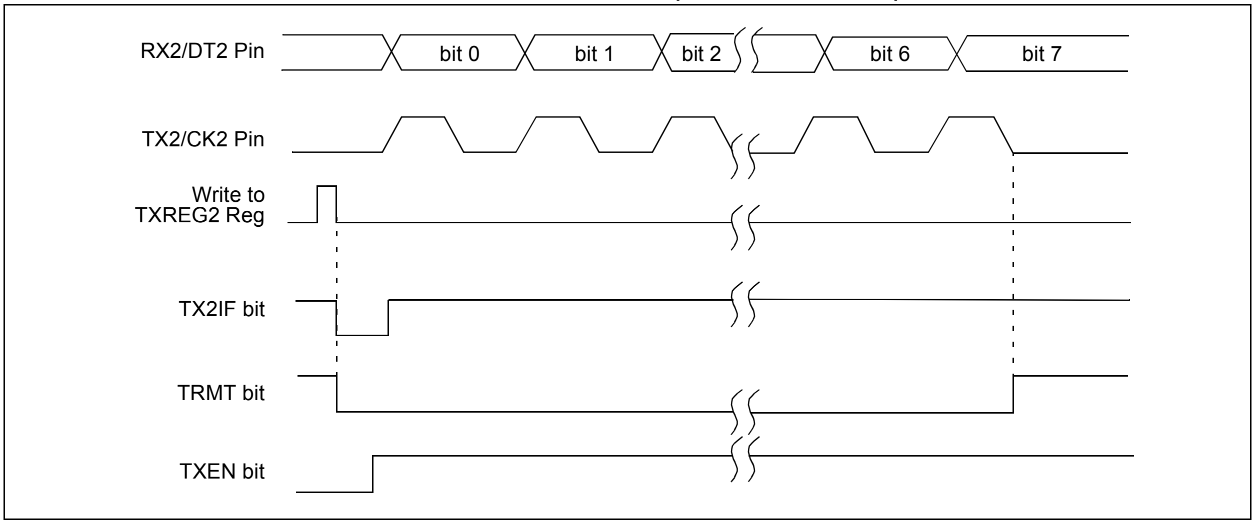


TABLE 19-6: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR3	—	—	RC2IF	TX2IF	—	CCP2IF	CCP1IF	—	59
PIE3	—	—	RC2IE	TX2IE	—	CCP2IE	CCP1IE	—	59
IPR3	—	—	RC2IP	TX2IP	—	CCP2IP	CCP1IP	—	59
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	61
TXREG2	AUSART Transmit Register								61
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	61
SPBRG2	AUSART Baud Rate Generator Register								61
LATG	U2OD	U1OD	—	LATG4	LATG3	LATG2	LATG1	LATG0	60

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

20.2 Selecting and Configuring Automatic Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/$\overline{\text{DONE}}$ bit is set.

When the GO/$\overline{\text{DONE}}$ bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/$\overline{\text{DONE}}$ bit. This occurs when the ACQT<2:0> bits (ADCON2<5:3>) remain in their Reset state ('000') and is compatible with devices that do not offer programmable acquisition times.

If desired, the ACQT bits can be set to select a programmable acquisition time for the A/D module. When the GO/$\overline{\text{DONE}}$ bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/$\overline{\text{DONE}}$ bit.

In either case, when the conversion is completed, the GO/$\overline{\text{DONE}}$ bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

20.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD (see parameter 130 in Table 26-26 for more information).

Table 20-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 20-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS<2:0>	
2 TOSC	`000`	2.86 MHz
4 TOSC	`100`	5.71 MHz
8 TOSC	`001`	11.43 MHz
16 TOSC	`101`	22.86 MHz
32 TOSC	`010`	40.0 MHz
64 TOSC	`110`	40.0 MHz
RC(1)	`x11`	1.00 MHz(2)

Note 1: The RC source has a typical TAD time of 4 μs.

2: For device frequencies above 1 MHz, the device must be in Sleep mode for the entire conversion or the A/D accuracy may be out of specification.

20.4 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will be accurately converted.

2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

RLNCF	Rotate Left f (No Carry)

Syntax: RLNCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0, 1]$
$a \in [0, 1]$

Operation: $(f<n>) \rightarrow dest<n + 1>$,
$(f<7>) \rightarrow dest<0>$

Status Affected: N, Z

Encoding:

`0100`	`01da`	`ffff`	`ffff`

Description: The contents of register ‘f’ are rotated one bit to the left. If ‘d’ is ‘`0`’, the result is placed in W. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.

If ‘a’ is ‘`0`’, the Access Bank is selected. If ‘a’ is ‘`1`’, the BSR is used to select the GPR bank.

If ‘a’ is ‘`0`’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 25.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode”** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write to destination

Example: `RLNCF REG, 1, 0`

```
Before Instruction
    REG    =   1010 1011
After Instruction
    REG    =   0101 0111
```

RRCF	Rotate Right f through Carry

Syntax: RRCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0, 1]$
$a \in [0, 1]$

Operation: $(f<n>) \rightarrow dest<n - 1>$,
$(f<0>) \rightarrow C$,
$(C) \rightarrow dest<7>$

Status Affected: C, N, Z

Encoding:

`0011`	`00da`	`ffff`	`ffff`

Description: The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘`0`’, the result is placed in W. If ‘d’ is ‘`1`’, the result is placed back in register ‘f’.

If ‘a’ is ‘`0`’, the Access Bank is selected. If ‘a’ is ‘`1`’, the BSR is used to select the GPR bank.

If ‘a’ is ‘`0`’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 25.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode”** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write to destination

Example: `RRCF REG, 0, 0`

```
Before Instruction
    REG    =   1110 0110
    C      =   0
After Instruction
    REG    =   1110 0110
    W      =   0111 0011
    C      =   0
```

XORWF	**Exclusive OR W with f**
Syntax:	XORWF f {,d {,a}}
Operands:	$0 \leq f \leq 255$ $d \in [0, 1]$ $a \in [0, 1]$
Operation:	(W) .XOR. (f) $\rightarrow$ dest
Status Affected:	N, Z
Encoding:	`0001` `10da` `ffff` `ffff`
Description:	Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register 'f'. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `XORWF REG, 1, 0`

Before Instruction
- REG = AFh
- W = B5h

After Instruction
- REG = 1Ah
- W = B5h

SUBFSR **Subtract Literal from FSR**

Syntax:	SUBFSR f, k
Operands:	$0 \le k \le 63$ $f \in [\ 0, 1, 2\ ]$
Operation:	FSRf – k → FSRf
Status Affected:	None
Encoding:	`1110` `1001` `ffkk` `kkkk`
Description:	The 6-bit literal, 'k', is subtracted from the contents of the FSR specified by 'f'.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `SUBFSR 2, 23h`

Before Instruction
FSR2 = 03FFh
After Instruction
FSR2 = 03DCh

SUBULNK **Subtract Literal from FSR2 and Return**

Syntax:	SUBULNK k
Operands:	$0 \le k \le 63$
Operation:	FSR2 – k → FSR2, (TOS) → PC
Status Affected:	None
Encoding:	`1110` `1001` `11kk` `kkkk`
Description:	The 6-bit literal, 'k', is subtracted from the contents of the FSR2. A `RETURN` is then executed by loading the PC with the TOS. The instruction takes two cycles to execute; a `NOP` is performed during the second cycle. This may be thought of as a special case of the `SUBFSR` instruction, where f = 3 (binary '`11`'); it operates only on FSR2.
Words:	1
Cycles:	2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination
No Operation	No Operation	No Operation	No Operation

Example: `SUBULNK 23h`

Before Instruction
FSR2 = 03FFh
PC = 0100h
After Instruction
FSR2 = 03DCh
PC = (TOS)

ADDWF — **ADD W to Indexed (Indexed Literal Offset mode)**

Syntax:	ADDWF [k] {,d}
Operands:	$0 \leq k \leq 95$ $d \in [0, 1]$
Operation:	(W) + ((FSR2) + k) → dest
Status Affected:	N, OV, C, DC, Z
Encoding:	`0010` `01d0` `kkkk` `kkkk`
Description:	The contents of W are added to the contents of the register indicated by FSR2, offset by the value, 'k'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process Data	Write to destination

Example: `ADDWF [OFST] ,0`

Before Instruction
- W = 17h
- OFST = 2Ch
- FSR2 = 0A00h
- Contents of 0A2Ch = 20h

After Instruction
- W = 37h
- Contents of 0A2Ch = 20h

BSF — **Bit Set Indexed (Indexed Literal Offset mode)**

Syntax:	BSF [k], b
Operands:	$0 \leq f \leq 95$ $0 \leq b \leq 7$
Operation:	1 → ((FSR2) + k)<b>
Status Affected:	None
Encoding:	`1000` `bbb0` `kkkk` `kkkk`
Description:	Bit 'b' of the register indicated by FSR2, offset by the value, 'k', is set.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `BSF [FLAG_OFST], 7`

Before Instruction
- FLAG_OFST = 0Ah
- FSR2 = 0A00h
- Contents of 0A0Ah = 55h

After Instruction
- Contents of 0A0Ah = D5h

SETF — **Set Indexed (Indexed Literal Offset mode)**

Syntax:	SETF [k]
Operands:	$0 \leq k \leq 95$
Operation:	FFh → ((FSR2) + k)
Status Affected:	None
Encoding:	`0110` `1000` `kkkk` `kkkk`
Description:	The contents of the register indicated by FSR2, offset by 'k', are set to FFh.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read 'k'	Process Data	Write register

Example: `SETF [OFST]`

Before Instruction
- OFST = 2Ch
- FSR2 = 0A00h
- Contents of 0A2Ch = 00h

After Instruction
- Contents of 0A2Ch = FFh

25.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB® IDE TOOLS

The latest versions of Microchip's software tools have been designed to fully support the extended instruction set for the PIC18F85J11 family. This includes the MPLAB C18 C Compiler, MPASM assembly language and MPLAB Integrated Development Environment (IDE).

When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is '1', enabling the extended instruction set and Indexed Literal Offset Addressing. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

- A menu option or dialog box within the environment that allows the user to configure the language tool and its settings for the project
- A command line option
- A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.

TABLE 26-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	E_P	Cell Endurance	100	1k	—	E/W	-40°C to +85°C
D131	V_{PR}	V_{DD} for Read	V_{MIN}	—	3.6	V	V_{MIN} = Minimum operating voltage
D132	V_{PEW}	Voltage for Self-Timed Erase or Write					
		V_{DD}	2.35	—	3.6	V	ENVREG tied to V_{DD}
		V_{DDCORE}	2.25	—	2.7	V	ENVREG tied to V_{SS}
D133A	T_{IW}	Self-Timed Write Cycle Time	—	2.8	—	ms	
D133B	T_{IE}	Self-Timed Block Erase Cycle Time	—	33	—	ms	
D134	T_{RETD}	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	I_{DDP}	Supply Current during Programming	—	3	7	mA	
D1xxx	T_{WE}	Writes per Erase Cycle	—	—	1		Per one physical word address

† Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.