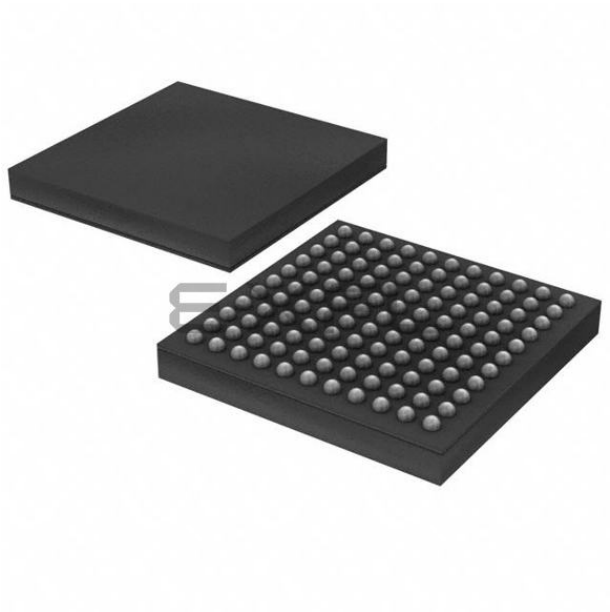

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 93 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.85V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-VFBGA |
| Supplier Device Package | 120-BGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg295f1024-bga120 |

available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 2.1.19 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

### 2.1.20 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

### 2.1.21 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 2.1.22 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.23 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.24 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

### 2.1.25 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 2.1.26 Operational Amplifier (OPAMP)

The EFM32GG295 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

| Module | Configuration | Pin Connections |
|---|---|---|
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in Table 4.3 (p. 63) |

## 2.3 Memory Map

The *EFM32GG295* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

***Figure 2.2. EFM32GG295 Memory Map with largest RAM and Flash sizes***

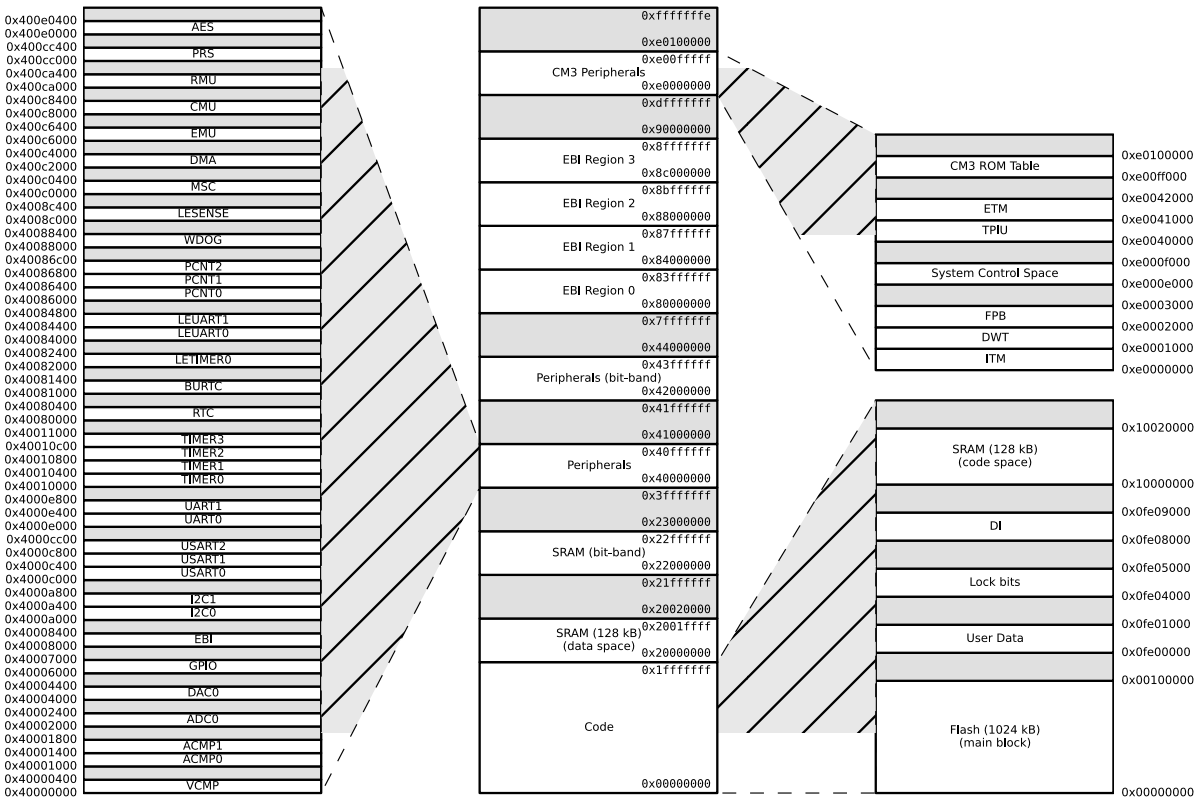
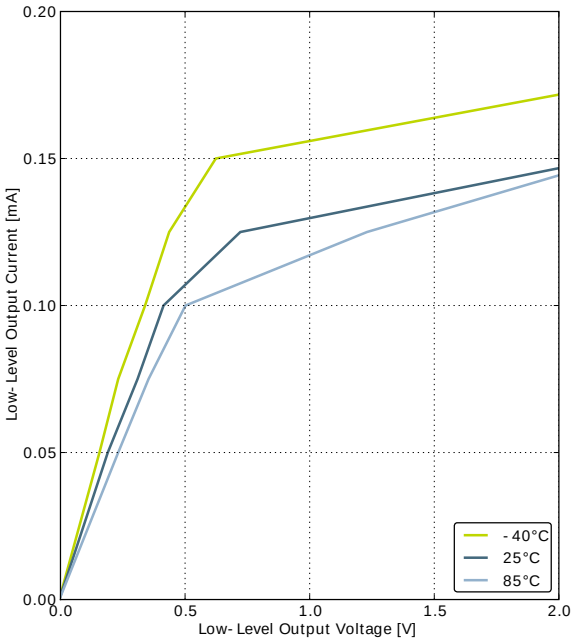
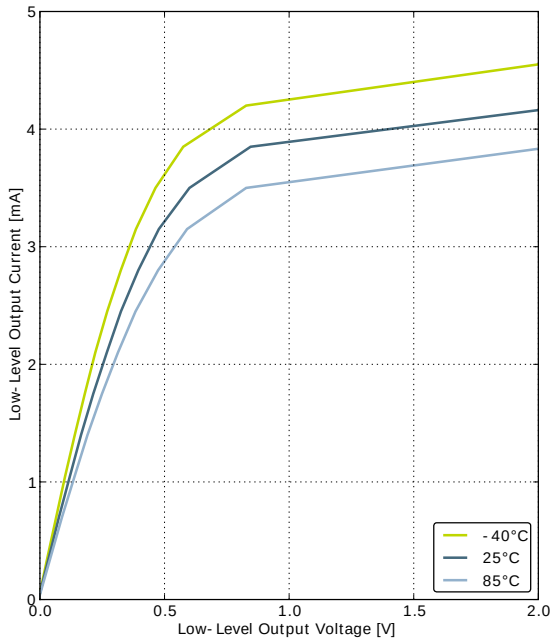


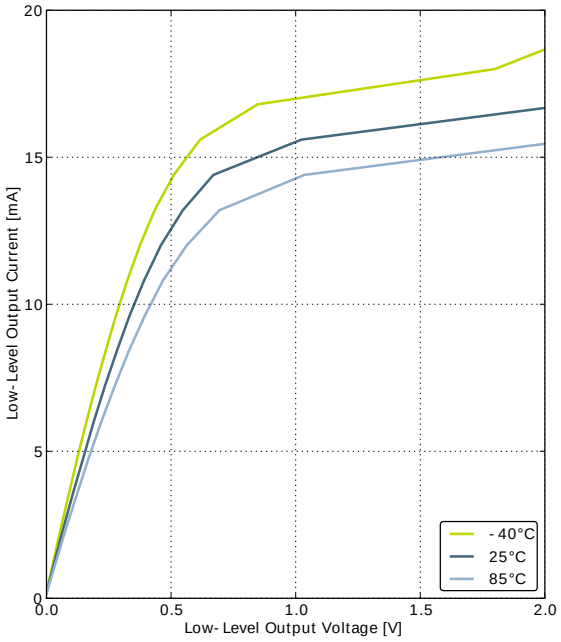
***Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage***



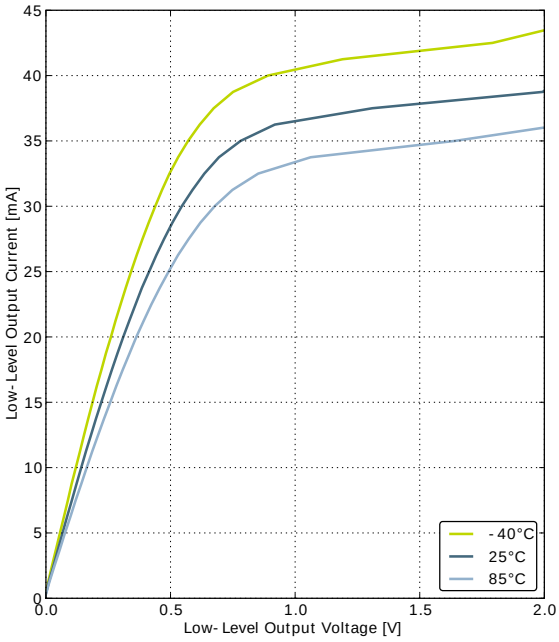

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

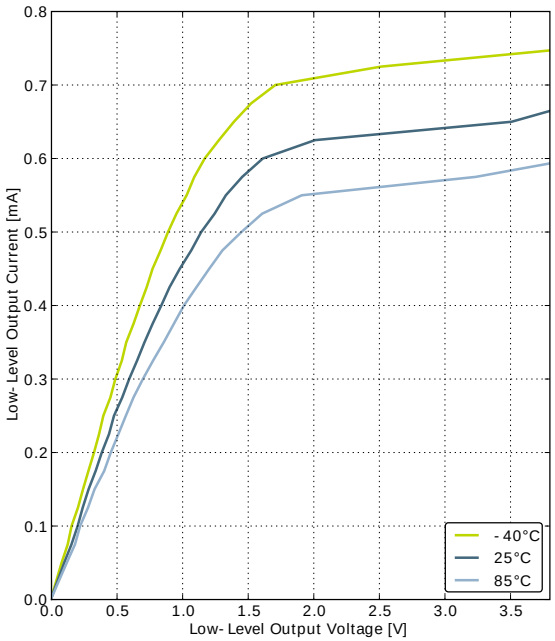



GPIO_Px_CTRL DRIVEMODE = STANDARD

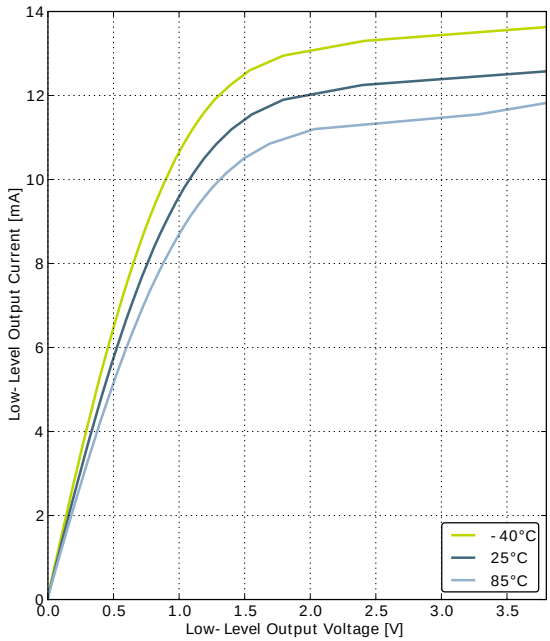



GPIO_Px_CTRL DRIVEMODE = HIGH

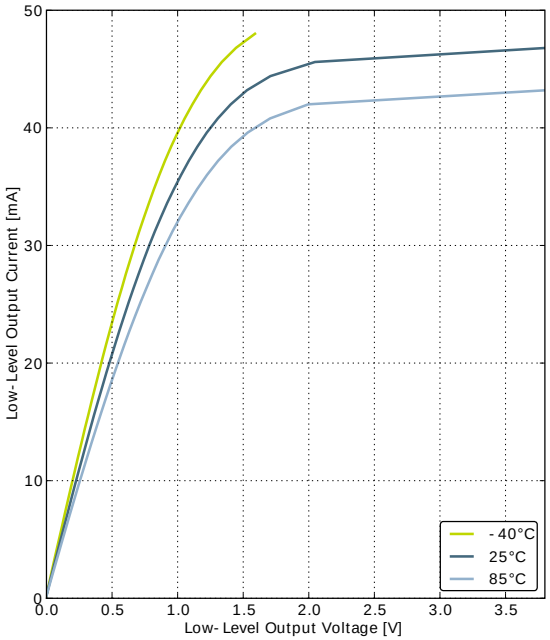
***Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage***



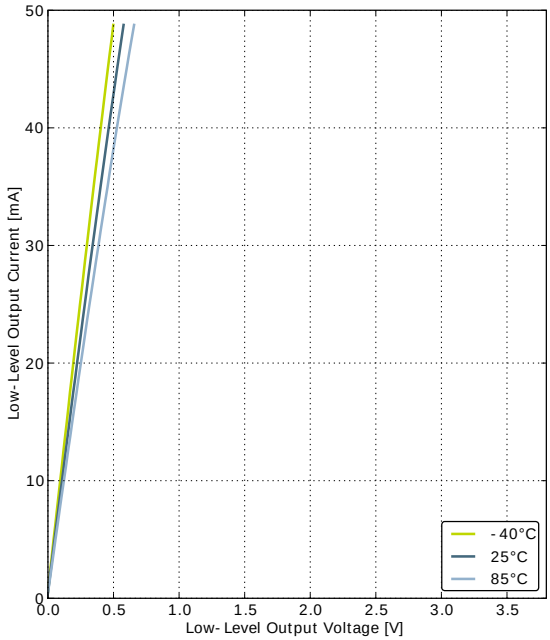

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

***Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature***

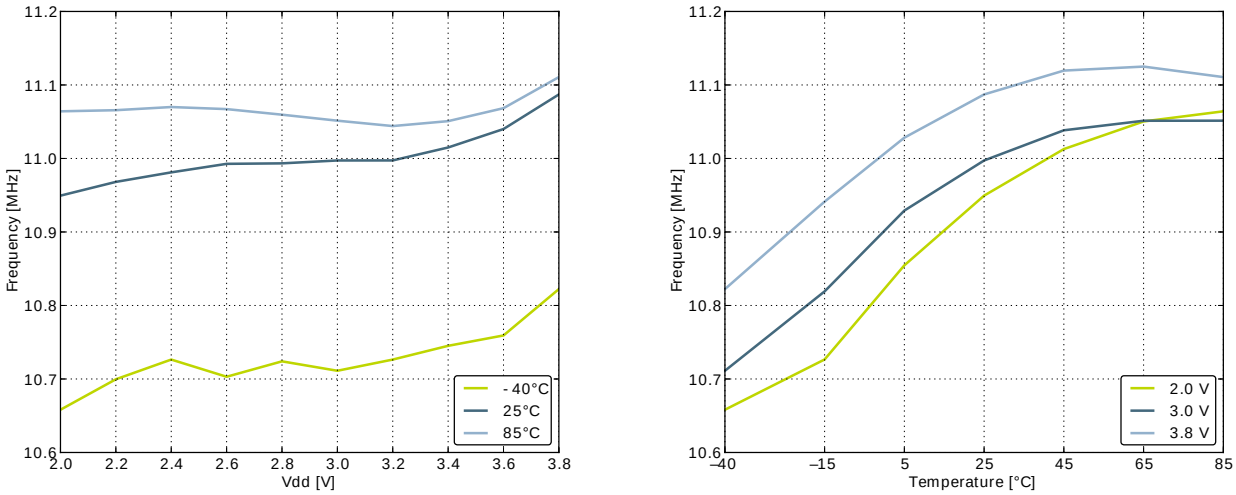



***Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature***

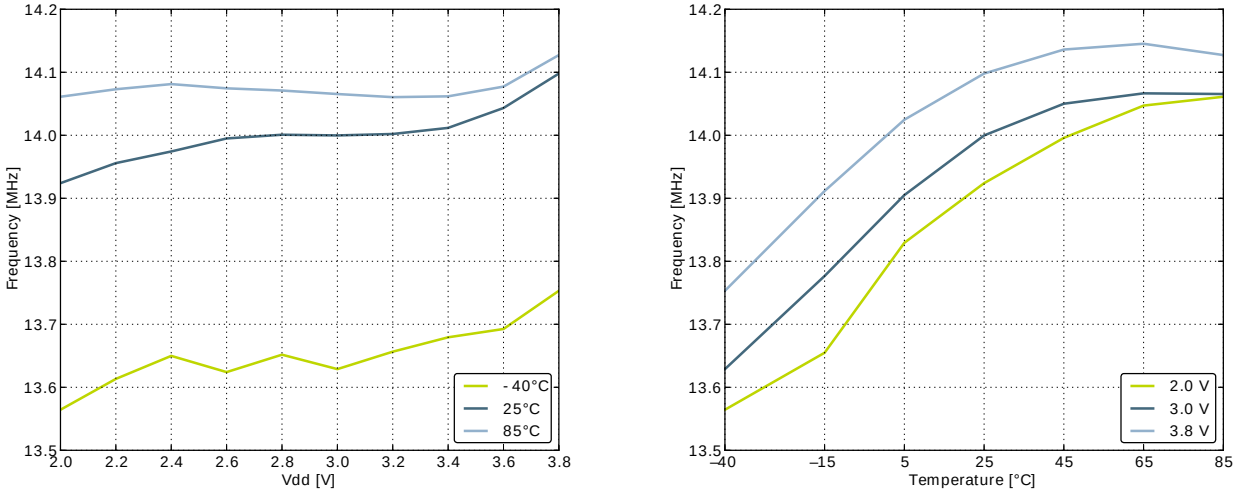



***Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature***

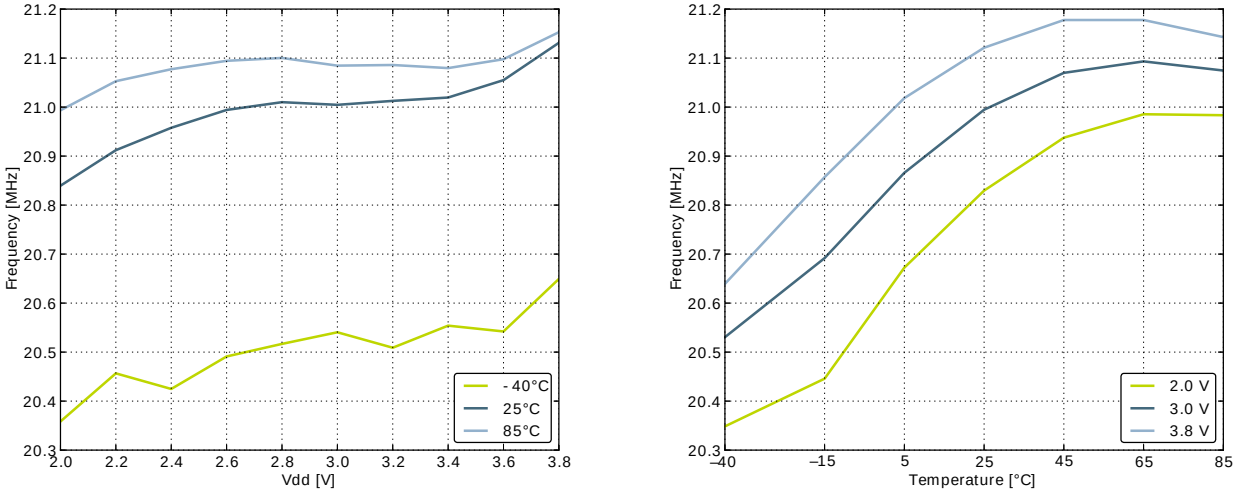
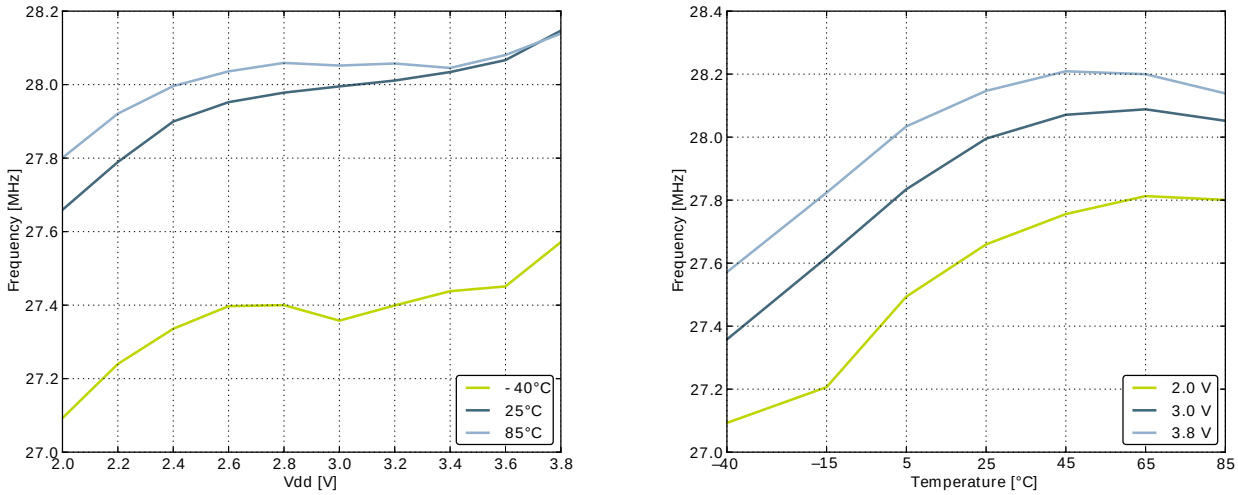


*Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature*




## 3.9.5 AUXHFRCO

*Table 3.12. AUXHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48[1] | 6.60[1] | 6.72[1] | MHz |
| | | 1 MHz frequency band | 1.15[2] | 1.20[2] | 1.25[2] | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $DC_{AUXHFRCO}$ | Duty cycle | $f_{AUXHFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[3] | | % |

[1]For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2]For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3]The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

***Figure 3.33. EBI Read Enable Related Output Timing***

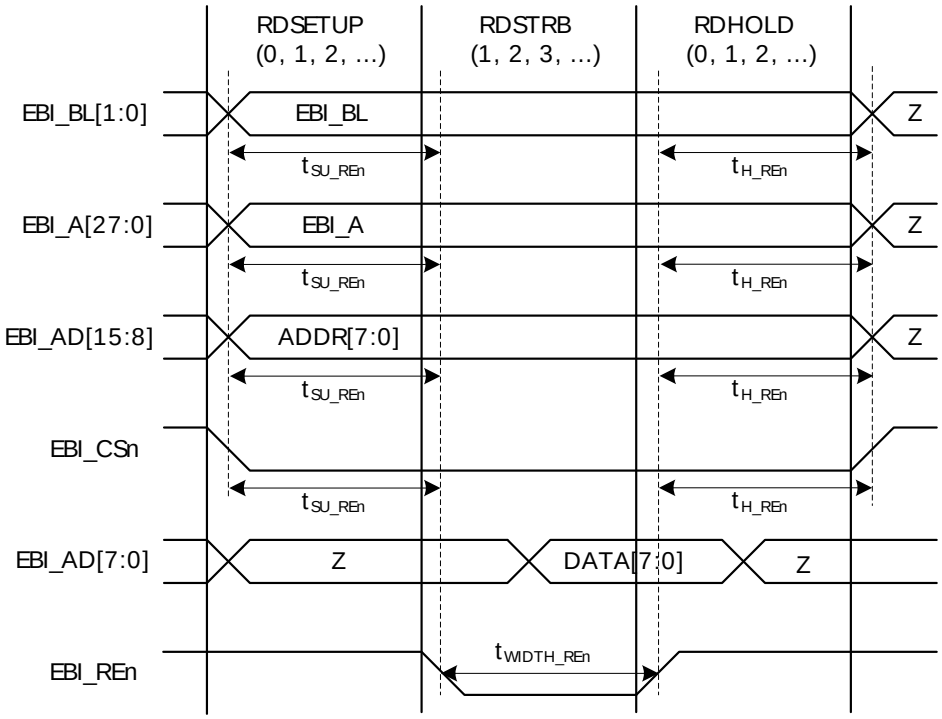



***Table 3.21. EBI Read Enable Related Output Timing***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OH\_REn}$ [1 2 3 4] | Output hold time, from trailing EBI_REn/ EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | -10.00 + (RDHOLD * $t_{HFCORECLK}$) | | | ns |
| $t_{OSU\_REn}$ [1 2 3 4 5] | Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn/EBI_NANDREn edge | -10.00 + (RDSETUP * $t_{HFCORECLK}$) | | | ns |
| $t_{WIDTH\_REn}$ [1 2 3 4 5 6] | EBI_REn pulse width | -9.00 + ((RD-STRB+1) * $t_{HFCORE-CLK}$) | | | ns |

[1]Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)

[2]Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

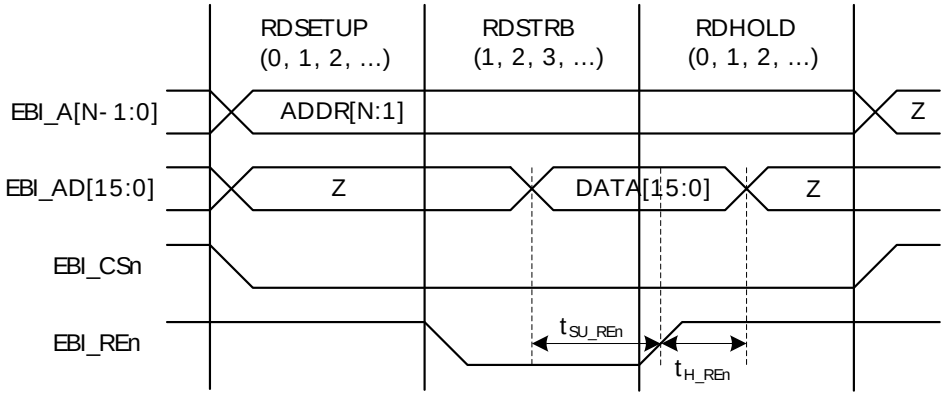
[3]Applies for all polarities (figure only shows active low signals)

[4]Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

[5]The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of $t_{WIDTH\_REn}$ and increases the length of $t_{OSU\_REn}$ by 1/2 * $t_{HFCLKNODIV}$.

[6]When page mode is used, RDSTRB is replaced by RDPA for page hits.

### Figure 3.34. EBI Read Enable Related Timing Requirements

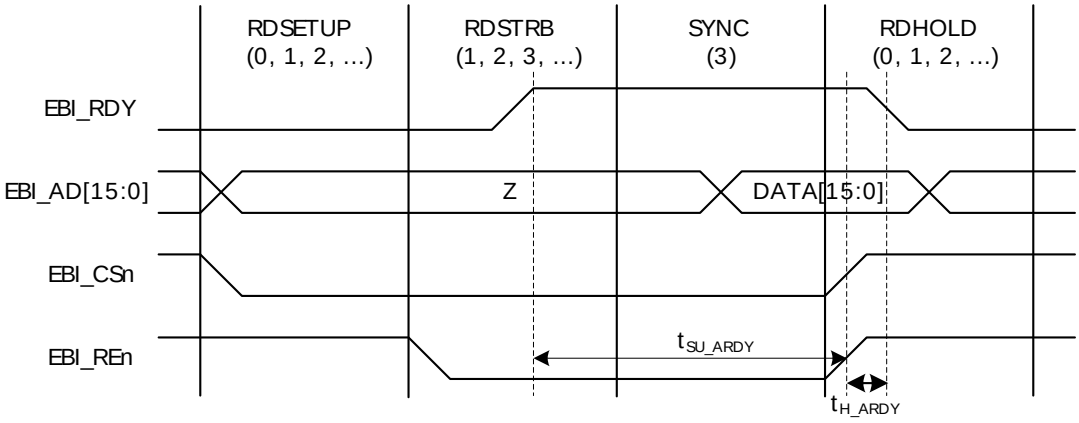



### Table 3.22. EBI Read Enable Related Timing Requirements

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SU\_REn}$ [1 2 3 4] | Setup time, from EBI_AD valid to trailing EBI_REn edge | 37 | | | ns |
| $t_{H\_Ren}$ [1 2 3 4] | Hold time, from trailing EBI_REn edge to EBI_AD invalid | -1 | | | ns |

[1]Applies for all addressing modes (figure only shows D16A8).
[2]Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)
[3]Applies for all polarities (figure only shows active low signals)
[4]Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

### Figure 3.35. EBI Ready/Wait Related Timing Requirements




### Table 3.23. EBI Ready/Wait Related Timing Requirements

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SU\_ARDY}$ [1 2 3 4] | Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge | 37 + (3 * $t_{HFCORECLK}$) | | | ns |

***Figure 3.37. SPI Slave Timing***

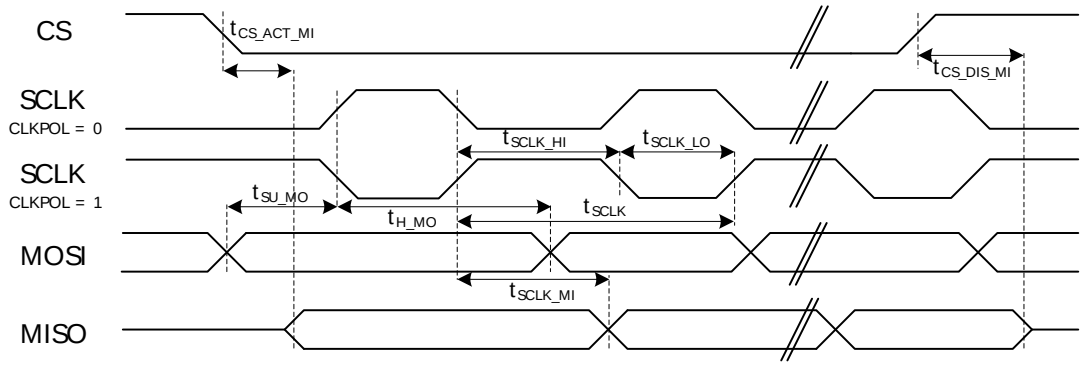



***Table 3.28. SPI Slave Timing***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SCLK\_sl}$ [1] [2] | SCKL period | 2 * $t_{HFPER-CLK}$ | | | ns |
| $t_{SCLK\_hi}$ [1] [2] | SCLK high period | 3 * $t_{HFPER-CLK}$ | | | ns |
| $t_{SCLK\_lo}$ [1] [2] | SCLK low period | 3 * $t_{HFPER-CLK}$ | | | ns |
| $t_{CS\_ACT\_MI}$ [1] [2] | CS active to MISO | 4.00 | | 30.00 | ns |
| $t_{CS\_DIS\_MI}$ [1] [2] | CS disable to MISO | 4.00 | | 30.00 | ns |
| $t_{SU\_MO}$ [1] [2] | MOSI setup time | 4.00 | | | ns |
| $t_{H\_MO}$ [1] [2] | MOSI hold time | 2 + 2* $t_{HF-PERCLK}$ | | | ns |
| $t_{SCLK\_MI}$ [1] [2] | SCLK to MISO | 9 + $t_{HFPER-CLK}$ | | 36 + 2*$t_{HF-PERCLK}$ | ns |

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

# 3.18 Digital Peripherals

***Table 3.29. Digital Peripherals***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{USART}$ | USART current | USART idle current, clock enabled | | 4.9 | | µA/MHz |
| $I_{UART}$ | UART current | UART idle current, clock enabled | | 3.4 | | µA/MHz |
| $I_{LEUART}$ | LEUART current | LEUART idle current, clock enabled | | 140 | | nA |
| $I_{I2C}$ | I2C current | I2C idle current, clock enabled | | 6.1 | | µA/MHz |
| $I_{TIMER}$ | TIMER current | TIMER_0 idle current, clock enabled | | 6.9 | | µA/MHz |
| $I_{LETIMER}$ | LETIMER current | LETIMER idle current, clock enabled | | 119 | | nA |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C11 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| C12 | PC14 | ACMP1_CH6<br>DAC0_OUT1ALT #2/<br>OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3<br>TIM1_CC1 #0<br>PCNT0_S1IN #0 | US0_CS #3<br>U0_TX #3 | LES_CH14 #0 |
| C13 | PC15 | ACMP1_CH7<br>DAC0_OUT1ALT #3/<br>OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3<br>TIM1_CC2 #0 | US0_CLK #3<br>U0_RX #3 | LES_CH15 #0<br>DBG_SWO #1 |
| D1 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| D2 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D11 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| D12 | PC12 | ACMP1_CH4<br>DAC0_OUT1ALT #0/<br>OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1<br>LES_CH12 #0 |
| D13 | PC13 | ACMP1_CH5<br>DAC0_OUT1ALT #1/<br>OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3<br>TIM1_CC0 #0<br>TIM1_CC2 #4<br>PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| E1 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| E2 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| E3 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| E11 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| E12 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| E13 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| F1 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| F2 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F3 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| F11 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| F12 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| F13 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| G1 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| G2 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| G3 | IOVDD_2 | Digital IO power supply 2. | | | | |
| G11 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| G12 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| G13 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| H1 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| H2 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| H3 | VSS | Ground. | | | | |
| H11 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| | | | | PCNT1_S0IN #0 | | |
| M3 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| M4 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| M5 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| M6 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| M7 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| M8 | AVSS_1 | Analog ground 1. | | | | |
| M9 | AVDD_2 | Analog power supply 2. | | | | |
| M10 | AVDD_1 | Analog power supply 1. | | | | |
| M11 | AVSS_0 | Analog ground 0. | | | | |
| M12 | PD3 | ADC0_CH3<br>OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| M13 | PD6 | ADC0_CH6<br>OPAMP_P1 | | LETIM0_OUT0 #0<br>TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| N1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| N2 | PC5 | ACMP0_CH5<br>OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| N3 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| N4 | PA11 | | EBI_HSNC #0/1/2 | | | |
| N5 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| N6 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | | LETIM0_OUT0 #1<br>TIM1_CC2 #3 | I2C1_SDA #1 | |
| N7 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| N8 | AVSS_2 | Analog ground 2. | | | | |
| N9 | PB13 | HFXTAL_P | | | US0_CLK #4/5<br>LEU0_TX #1 | |
| N10 | PB14 | HFXTAL_N | | | US0_CS #4/5<br>LEU0_RX #1 | |
| N11 | AVDD_0 | Analog power supply 0. | | | | |
| N12 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| N13 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 58). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

***Note***

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| OPAMP_OUT1 | | | | | | | | OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |

The BGA120 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx.

# 5 PCB Layout and Soldering

## 5.1 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

# 7 Revision History

## 7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for $INL_{ADC}$ and $DNL_{ADC}$ parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with FULLBIAS=1 and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

## 7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

Updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

## 7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

## 7.7 Revision 0.98

May 25th, 2012

Corrected BGA solder balls material description.

Corrected EM3 current consumption in the Electrical Characteristics section.

## 7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected BGA120 package drawing.

Updated PCB land pattern, solder mask and stencil design.

## 7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance ($C_{LFXOL}$) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected BGA120 package drawing.

Updated PCB land pattern, solder mask and stencil design.

# B Contact Information

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Please visit the Silicon Labs Technical Support web page:
http://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

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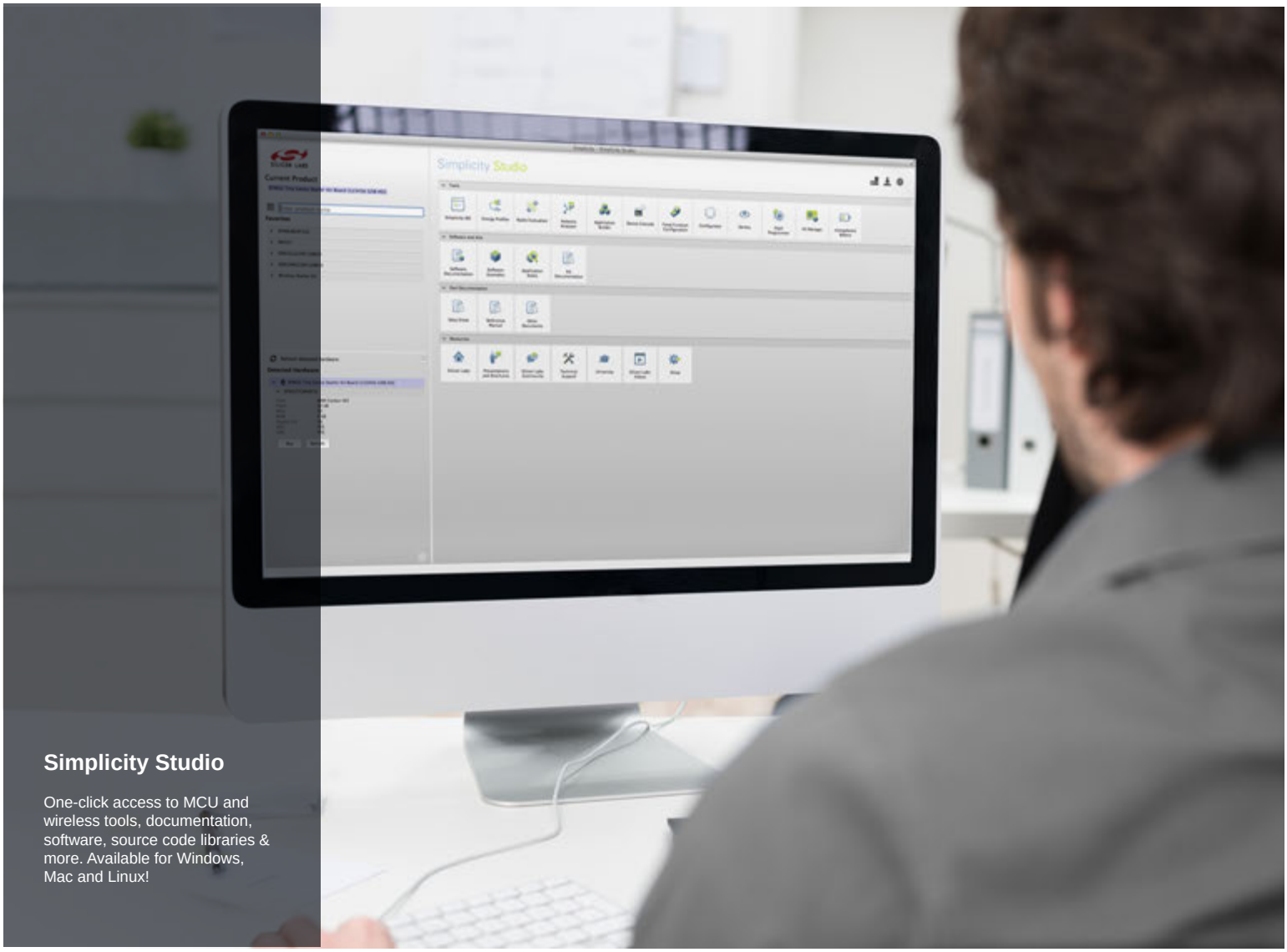


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