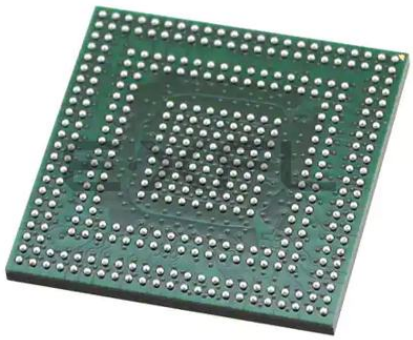

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8306cvmabdca

1 Overview

The MPC8306 incorporates the e300c3 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8306 also includes two DMA engines and a 16-bit DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8306. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8306 is shown in the following figure.

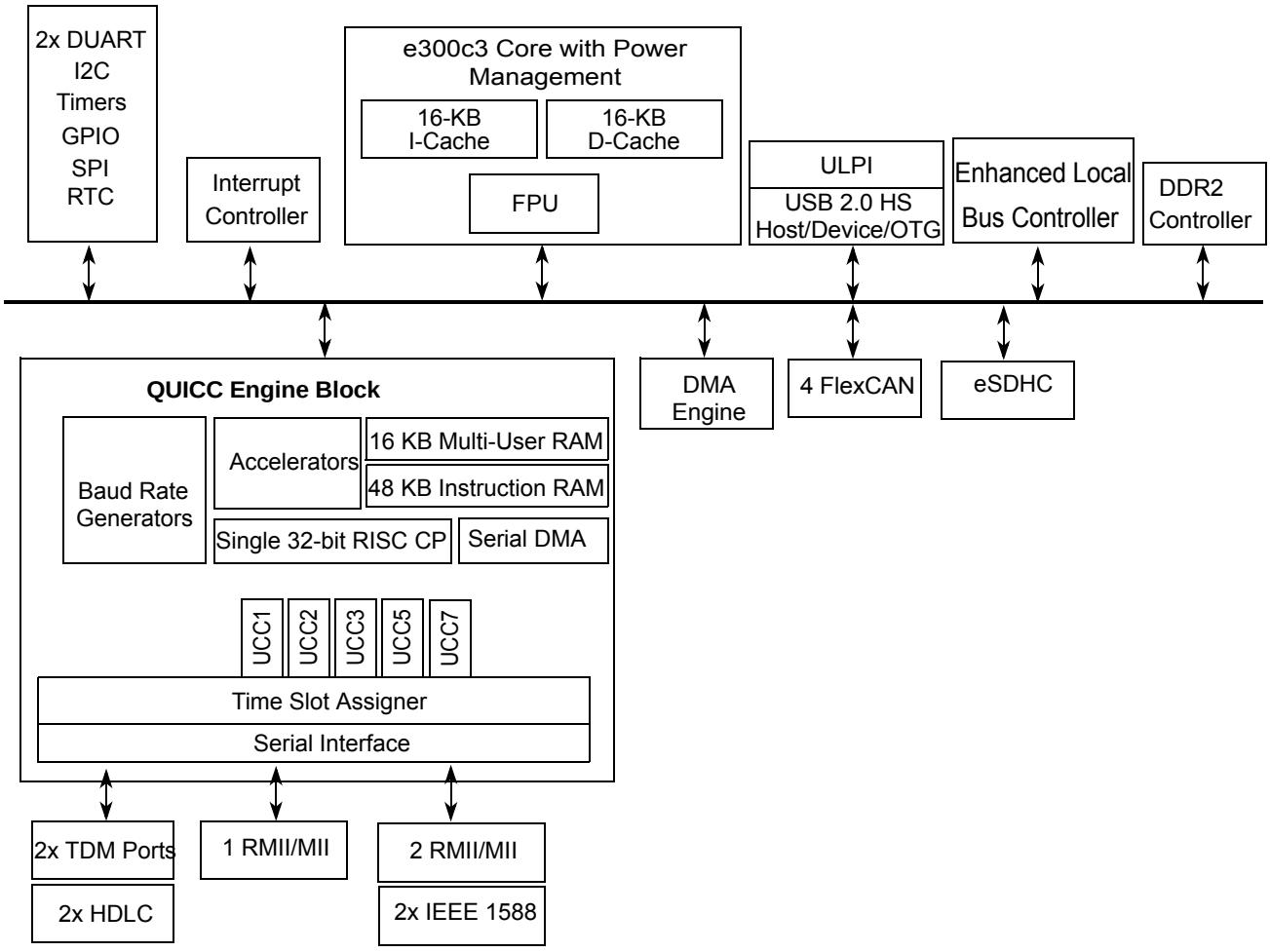


Figure 1. MPC8306 Block Diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, IEEE-1588, HDLC and TDM.

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage (V)
Local bus interface utilities signals	42	OV_{DD} = 3.3
DDR2 signal	18	GV_{DD} = 1.8
DUART, system control, I2C, SPI, JTAG	42	OV_{DD} = 3.3
GPIO signals	42	OV_{DD} = 3.3

2.1.4 Input Capacitance Specification

The following table describes the input capacitance for the SYS_CLK_IN pin in the MPC8306.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input capacitance for all pins except SYS_CLK_IN and QE_CLK_IN	C_I	6	8	pF	—
Input capacitance for SYS_CLK_IN and QE_CLK_IN	C_{ICLK_IN}	10	—	pF	1

Note:
1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and I/O supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

NOTE

There is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

The following table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306 reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8306. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8306 when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MVREF is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.100 V, f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM (GV_{DD}(typ) = 1.8 V).

Table 14. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.25	V	—
AC input high voltage	V_{IH}	MVREF + 0.25	—	V	—

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 15. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2

Table 16. DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
$\overline{MCS}$ output hold with respect to MCK 266 MHz	t_{DDKHCX}	 2.5	 —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MDM output setup with respect to MDQS 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.9	 —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100	 —	ps	5
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjusts in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. t_{DDKHMP} follows the symbol conventions described in note 1.

7 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8306.

7.1 Local Bus DC Electrical Characteristics

The following table provides the DC electrical characteristics for the local bus interface.

Table 17. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	μA

7.2 Local Bus AC Electrical Specifications

The following table describes the general timing parameters of the local bus interface of the MPC8306.

Table 18. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Table 19. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(max) to V_{IH}(min)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(min) to V_{IL}(max)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII receive AC timing diagram.

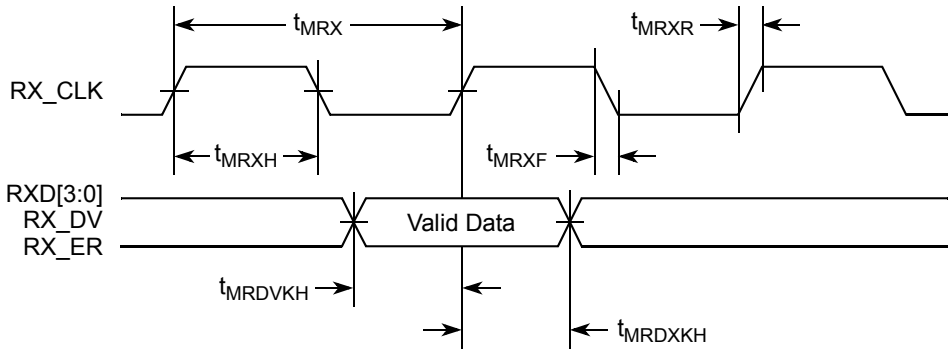


Figure 13. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII Transmit AC Timing Specifications

The following table provides the RMII transmit AC timing specifications.

Table 22. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	13	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

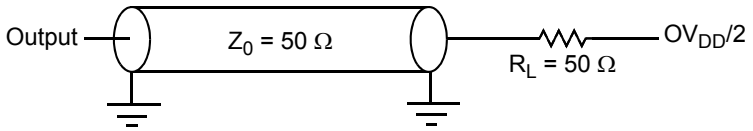


Figure 14. AC Test Load

The following figure shows the RMII receive AC timing diagram.

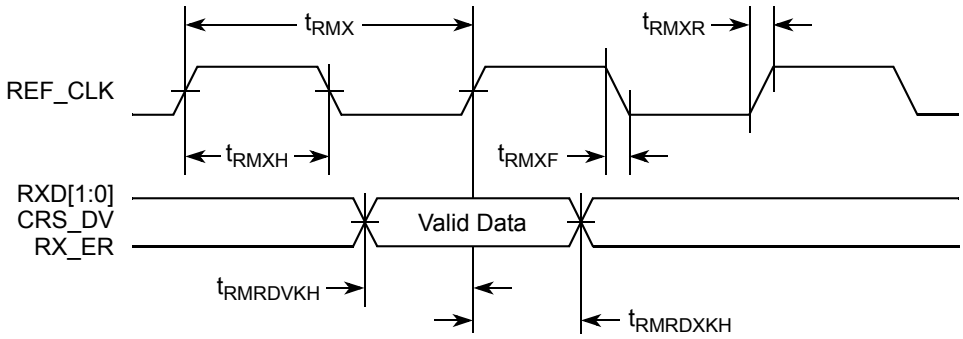


Figure 16. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

The following table provides the MII management AC timing specifications.

Table 25. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

9.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 29. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

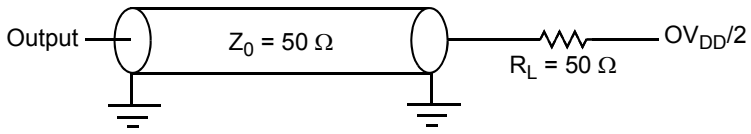
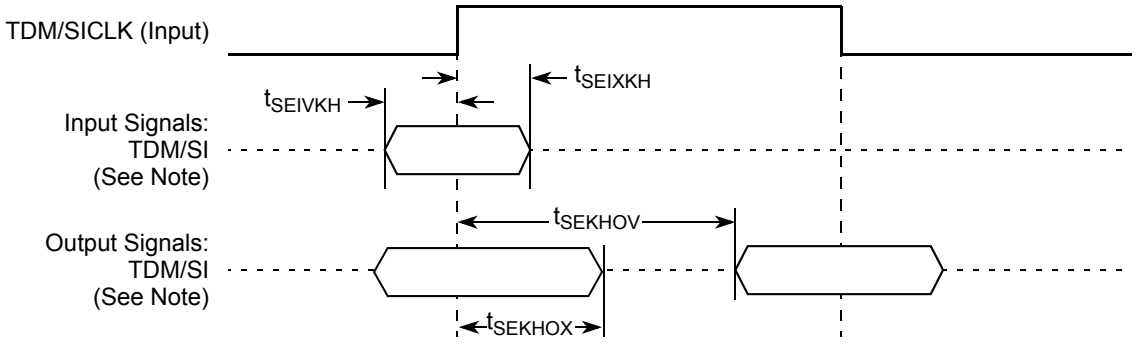


Figure 20. TDM/SI AC Test Load

The following figure represents the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

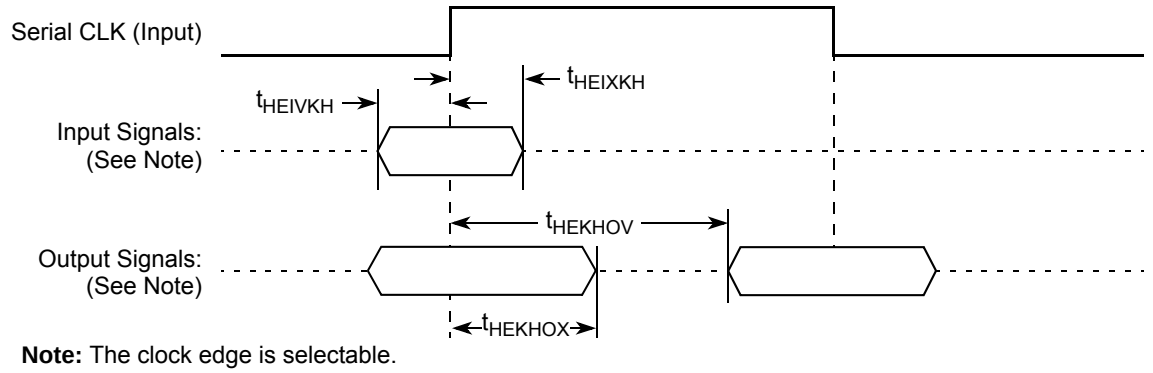
Figure 21. TDM/SI AC Timing (External Clock) Diagram

10 HDLC

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), of the MPC8306.

Figure 23 and Figure 24 represent the AC timing from Table 31. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

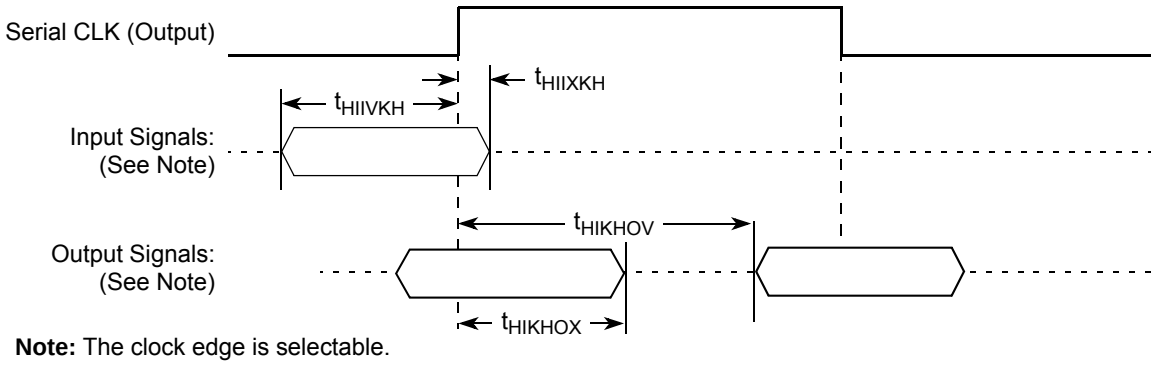
The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 23. AC Timing (External Clock) Diagram

The following figure shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 24. AC Timing (Internal Clock) Diagram

13 eSDHC

This section describes the DC and AC electrical specifications for the eSDHC interface of the device.

13.1 eSDHC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the eSDHC interface.

Table 36. eSDHC Interface DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × OV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 μA at OV_{DD} min	0.75 × OV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 μA at OV_{DD} min	—	0.125 × OV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 mA	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	μA	—

Notes:
1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2..
2. Open drain mode for MMC cards only.

13.2 eSDHC AC Timing Specifications

The following table provides the eSDHC AC timing specifications as defined in Figure 27 and Figure 28.

Table 37. eSDHC AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SHSCK}	0	25/33.25 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	4

Table 48. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

19.2 SPI AC Timing Specifications

The following table and provide the SPI input and output AC timing specifications.

Table 49. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. All units of output delay must be enabled for 8306 output port spimosi (SPI Master Mode)
4. delay units must not be enabled for Slave Mode.

The following figure provides the AC test load for the SPI.

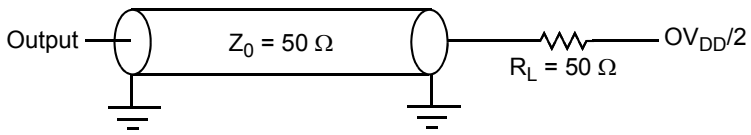
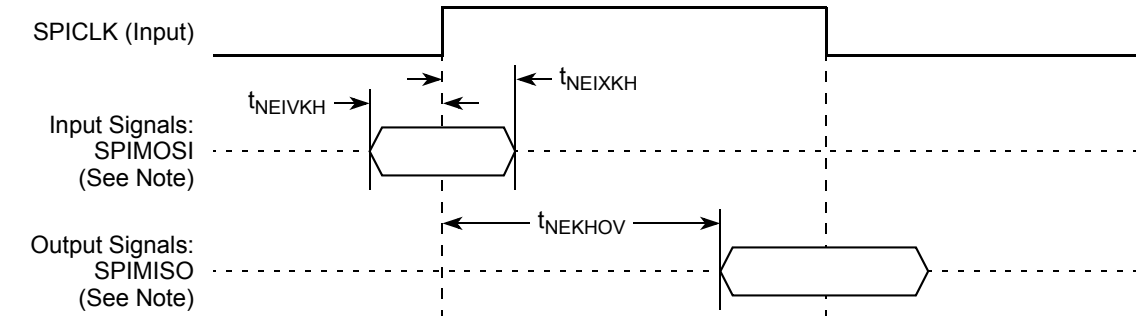


Figure 33. SPI AC Test Load

Figure 34 and Figure 35 represent the AC timing from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

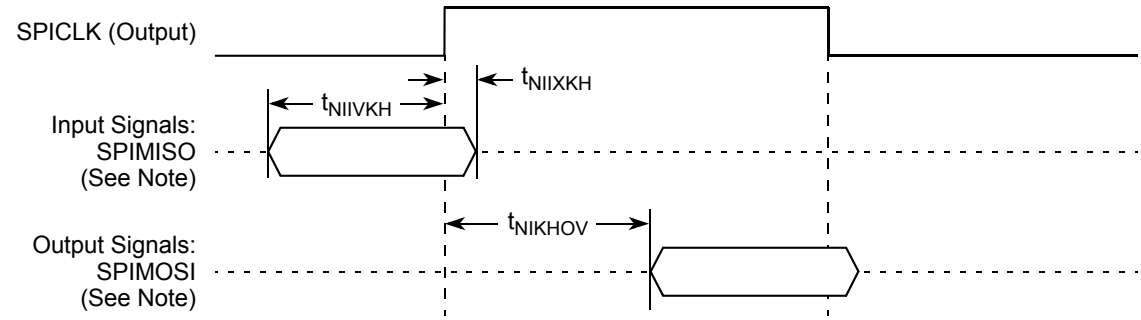
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8306.

20.1 JTAG DC Electrical Characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306.

Table 50. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

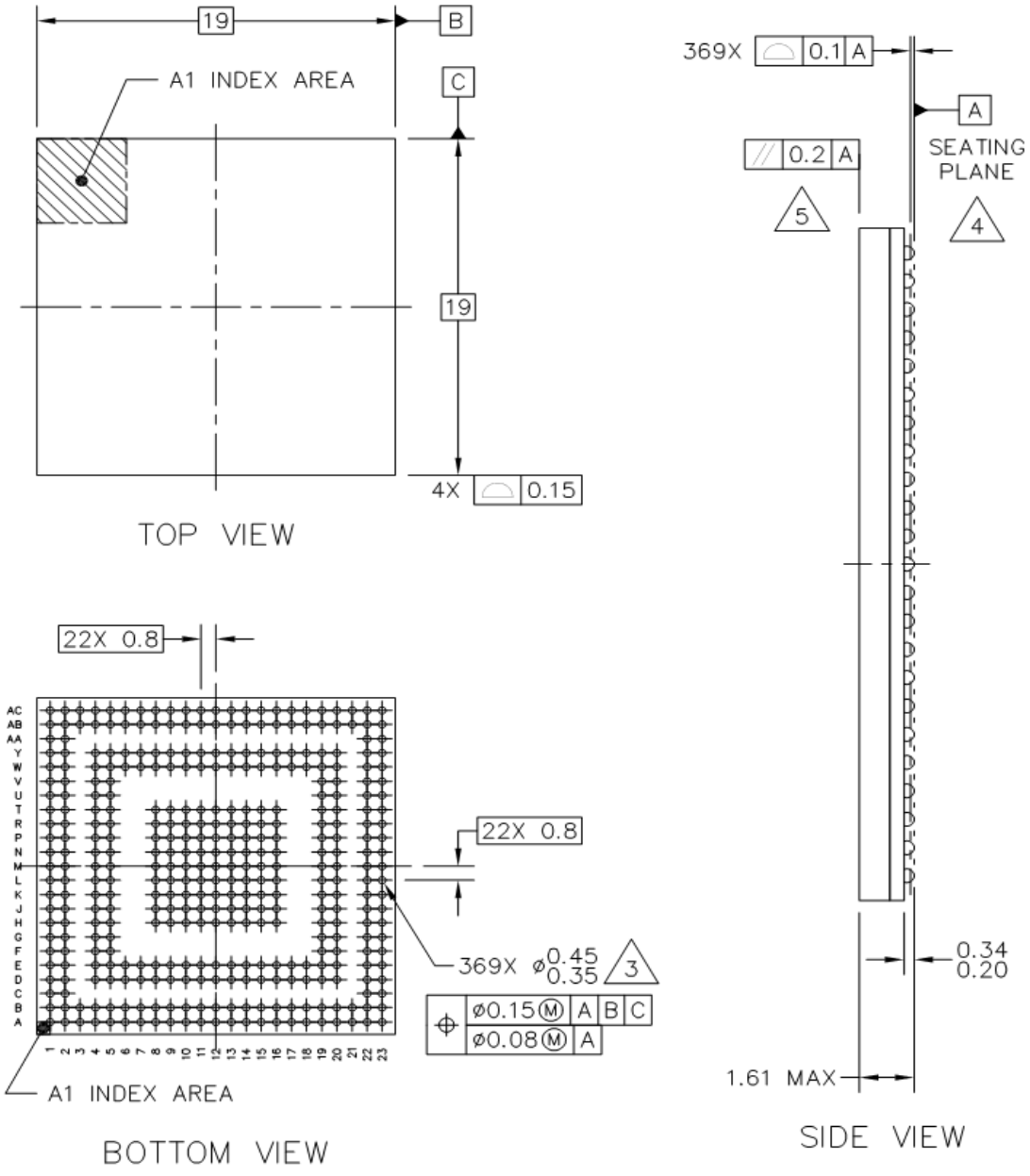


Figure 41. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8306 MAPBGA

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MA[8]	T1	O	GV_{DD}	—
MEMC_MA[9]	P4	O	GV_{DD}	—
MEMC_MA[10]	L4	O	GV_{DD}	—
MEMC_MA[11]	T2	O	GV_{DD}	—
MEMC_MA[12]	U1	O	GV_{DD}	—
MEMC_MA[13]	U2	O	GV_{DD}	—
MEMC_MWE_B	K1	O	GV_{DD}	—
MEMC_MRAS_B	K2	O	GV_{DD}	—
MEMC_MCAS_B	J1	O	GV_{DD}	—
MEMC_MCS_B[0]	J4	O	GV_{DD}	—
MEMC_MCS_B[1]	H1	O	GV_{DD}	—
MEMC_MCKE[0]	U4	O	GV_{DD}	—
MEMC_MCK[0]	V1	O	GV_{DD}	—
MEMC_MCK_B[0]	W1	O	GV_{DD}	—
MEMC_MODT[0]	H2	O	GV_{DD}	—
MEMC_MODT[1]	H4	O	GV_{DD}	—
MEMC_MVREF	L8		GV_{DD}	—
Local Bus Controller Interface				
LAD[0]	B7	IO	OV_{DD}	—
LAD[1]	D9	IO	OV_{DD}	—
LAD[2]	A6	IO	OV_{DD}	—
LAD[3]	B8	IO	OV_{DD}	—
LAD[4]	A7	IO	OV_{DD}	—
LAD[5]	A8	IO	OV_{DD}	—
LAD[6]	A9	IO	OV_{DD}	—
LAD[7]	D10	IO	OV_{DD}	—
LAD[8]	B10	IO	OV_{DD}	—
LAD[9]	A10	IO	OV_{DD}	—
LAD[10]	B11	IO	OV_{DD}	—
LAD[11]	D12	IO	OV_{DD}	—
LAD[12]	D11	IO	OV_{DD}	—
LAD[13]	A11	IO	OV_{DD}	—
LAD[14]	A12	IO	OV_{DD}	—
LAD[15]	B13	IO	OV_{DD}	—
LA[16]	A13	IO	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[17]	B14	O	OV_{DD}	—
LA[18]	A14	O	OV_{DD}	—
LA[19]	A15	O	OV_{DD}	—
LA[20]	A16	O	OV_{DD}	—
LA[21]	B16	O	OV_{DD}	—
LA[22]	A17	O	OV_{DD}	—
LA[23]	B17	O	OV_{DD}	—
LA[24]	A18	O	OV_{DD}	—
LA[25]	B19	O	OV_{DD}	—
LCS_B[0]	A19	O	OV_{DD}	3
LCS_B[1]	B20	O	OV_{DD}	3
LCS_B[2]	A20	O	OV_{DD}	3
LCS_B[3]	A21	O	OV_{DD}	3
LCLK[0]	D13	O	OV_{DD}	—
LGPL[0]/LFCLE	B22	O	OV_{DD}	—
LGPL[1]/LFALE	D16	O	OV_{DD}	—
LGPL[2]/LOE_B/LFRE_B	D19	O	OV_{DD}	—
LGPL[3]/LFWP_B	D17	O	OV_{DD}	—
LGPL[4]/LGTA_B/LUPWAIT/LFRB_B	E18	IO	OV_{DD}	—
LGPL[5]	E19	O	OV_{DD}	—
LWE_B[0]/LFWE_B[0]/LBS_B[0]	D15	O	OV_{DD}	—
LWE_B[1]/LBS_B[1]	D14	O	OV_{DD}	—
LBCTL	A22	O	OV_{DD}	—
LALE	B23	O	OV_{DD}	—
JTAG				
TCK	A3	I	OV_{DD}	—
TDI	B5	I	OV_{DD}	3
TDO	D7	O	OV_{DD}	—
TMS	A4	I	OV_{DD}	3
TRST_B	D8	I	OV_{DD}	3
Test Interface				
TEST_MODE	A5	I	OV_{DD}	—
System Control Signals				
HRESET_B	U20	IO	OV_{DD}	1
PORESET_B	V20	I	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USBDR_TXDRXD[7]/GPIO[37]/QE_BRG[11]	Y5	IO	OV_{DD}	—
DUART				
UART1_SOUT[1]/LSRCID4/LCS_B[4]	C23	O	OV_{DD}	—
UART1_SIN[1]/LDVAL/LCS_B[5]	F19	IO	OV_{DD}	—
UART1_SOUT[2]/UART1_RTS_B1/LCS_B[6]	D23	O	OV_{DD}	—
UART1_SIN[2]/UART1_CTS_B[1]/LCS_B[7]	D22	IO	OV_{DD}	—
Interrupts				
IRQ_B0_MCP_IN_B/CE_PI_0	E20	IO	OV_{DD}	—
IRQ_B1/MCP_OUT_B	E23	IO	OV_{DD}	—
IRQ_B2/CKSTOP_OUT_B	E22	IO	OV_{DD}	—
IRQ_B3/CKSTOP_IN_B	F20	I	OV_{DD}	—
I2C / SPI				
IIC_SDA1	G20	IO	OV_{DD}	2
IIC_SCL1	J20	IO	OV_{DD}	2
LCLK1/IIC_SCL2/CKSTOP_IN_B	H20	IO	OV_{DD}	2
SPISEL_BOOT/IIC_SDA2/CKSTOP_OUT_B	F23	O	OV_{DD}	2
SPIMOSI/LSRCID[2]	G22	IO	OV_{DD}	—
SPIMISO/LSRCID[3]	K20	IO	OV_{DD}	—
SPICLK/LSRCID[0]	G23	IO	OV_{DD}	—
SPISEL/LSRCID[1]	H22	I	OV_{DD}	—
FEC Management				
FEC_MDC	H23	O	OV_{DD}	—
FEC_MDIO	L20	IO	OV_{DD}	—
FEC1/GTM/GPIO				
FEC1_COL/GTM1_TIN[1]/GPIO[16]	AB20	IO	OV_{DD}	—
FEC1_CRS/GTM1_TGATE1_B/GPIO[17]	AC21	IO	OV_{DD}	—
FEC1_RX_CLK/GPIO[18]	Y17	IO	OV_{DD}	—
FEC1_RX_DV/GTM1_TIN[2]/GPIO[19]	Y18	IO	OV_{DD}	—
FEC1_RX_ER/GTM1_TGATE[2]_B/GPIO[20]	AB19	IO	OV_{DD}	—
FEC1_RXD0/GPIO[21]	AC20	IO	OV_{DD}	—
FEC1_RXD1/GTM1_TIN[3]/GPIO[22]	AC19	IO	OV_{DD}	—
FEC1_RXD2/GTM1_TGATE[3]_B/GPIO[23]	AC18	IO	OV_{DD}	—
FEC1_RXD3/GPIO[24]	AB17	IO	OV_{DD}	—
FEC1_TX_CLK/GTM1_TIN4/GPIO[25]	Y15	IO	OV_{DD}	—
FEC1_TX_EN/GTM1_TGATE[4]_B/GPIO[26]	Y16	IO	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FEC3_TXD0/FEC_TMR_PP2/GPIO[60]	R20	IO	OV_{DD}	—
FEC3_TXD1/FEC_TMR_PP3/GPIO[61]	T22	IO	OV_{DD}	—
FEC3_TXD2/FEC_TMR_ALARM1/GPIO[62]	T23	IO	OV_{DD}	—
FEC3_TXD3/FEC_TMR_ALARM2/GPIO[63]	T20	IO	OV_{DD}	—
HDLC/GPIO/TDM				
HDLC1_RXCLK/TDM1_RCK/GPIO[1]	U23	IO	OV_{DD}	—
HDLC1_RXD/TDM1_RD/GPIO[3]	U22	IO	OV_{DD}	—
HDLC1_TXCLK/GPIO[0]/TDM1_TCK/ QE_BRG[5]	AC22	IO	OV_{DD}	—
HDLC1_TXD/GPIO[2]/TDM1_TD/ CFG_RESET_SOURCE[0]	W18	IO	OV_{DD}	—
HDLC1_CD_B/GPIO[4]/TDM1_TFS	W19	IO	OV_{DD}	—
HDLC1_CTS_B/GPIO[5]/TDM1_RFS	Y20	IO	OV_{DD}	—
HDLC1_RTS_B/GPIO[6]/TDM1_STROBE_B/ CFG_RESET_SOURCE[1]	AB22	IO	OV_{DD}	—
HDLC2_TXCLK/GPIO[16]/TDM2_TCK/ QE_BRG[7]	AB23	IO	OV_{DD}	—
HDLC2_RXCLK/GPIO[17]/TDM2_RCK/ QE_BRG[8]	AA23	IO	OV_{DD}	—
HDLC2_TXD/GPIO[18]/TDM2_TD/ CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	—
HDLC2_RXD/GPIO[19]/TDM2_RD	Y23	IO	OV_{DD}	—
HDLC2_CD_B/GPIO[20]/TDM2_TFS	Y22	IO	OV_{DD}	—
HDLC2_CTS_B/GPIO[21]/TDM2_RFS	W23	IO	OV_{DD}	—
HDLC2_RTS_B/GPIO[22]/TDM2_STROBE_B/ CFG_RESET_SOURCE[3]	W22	IO	OV_{DD}	—
Power				
AV_{DD1}	L16	—	—	—
AV_{DD2}	M16	—	—	—
AV_{DD3}	N8	—	—	—
GV_{DD}	G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5	—	—	—
OV_{DD}	E7,E8,E9,E10,E11,E12, E13,E14, E15, E16,E17,G19,H19,J19,K 19,L19,M19, N19,P19,R19,T19,U19, W7,W8,W9, W10,W11, W12,W13, W14,W15, W16, W17	—	—	—

26 Document Revision History

The following table provides a revision history for this document.

Table 65. Document Revision History

Rev. No.	Date	Substantive Change(s)
3	12/2014	• In Table 20 an Table 21, V_{IL}(min) is replaced with V_{IL}(max) and V_{IH}(max) is replaced with V_{IL}(min) • Removed following signals from Table 52: – FEC1_TMR_TX_ESFD – FEC1_TMR_RX_ESFD – FEC2_TMR_TX_ESFD – FEC2_TMR_RX_ESFD • Updated following signal names in Table 52: – LGPL[0] to LGPL[0]/LFCLE – LGPL[1] to LGPL[1]/LFALE – LGPL[2] to LGPL[2]/LOE_B/LFRE_B – LGPL[3] to LGPL[3]/LFWP_B – LGPL[4] to LGPL[4]/LGTA_B/LUPWAIT/LFRB_B – LWE_B[0] to LWE_B[0]/LFWE_B[0]/LBS_B[0] – LWE_B[1] to LWE_B[1]/LBS_B[1]
2	09/2011	• Added Power numbers for core frequency of 333 MHz in Table 5. • Added new PLL configurations as per new core frequency in Table 60. • Added AF to indicate 333 MHz in Table 63.
1	06/2011	• Updated QE frequency in Table 5. • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 54. • Updated CEMF and CEDF as per new QE frequency in Table 60. • In Part Nomenclature field for QUICC Engine frequency, C now denotes 233 MHz. Updated Table 63. • Added SPISEL_BOOT in MPC8306 Pin out Listing Table 52. • Corrected SPISEL Pin Type in Table 52.
0	03/2011	Initial Release