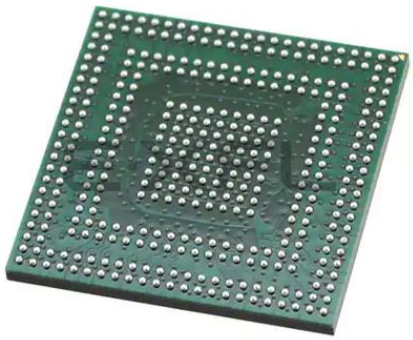

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8306cvmafdca

  - Asynchronous HDLC (bit rate up to 2 Mbps)
  - Two TDM interfaces supporting up to 128 QUICC multichannel controller channels, each running at 64 kbps

  For more information on QUICC Engine sub-modules, see *QUICC Engine Block Reference Manual with Protocol Interworking*.

- DDR SDRAM memory controller
  - Programmable timing supporting DDR2 SDRAM
  - Integrated SDRAM clock generation
  - 16-bit data interface, up to 266-MHz data rate
  - 14 address lines
  - The following SDRAM configurations are supported:
    - Up to two physical banks (chip selects), 256-Mbyte per chip select for 16 bit data interface.
    - 64-Mbit to 2-Gbit devices with x8/x16 data ports (no direct x4 support)
    - One 16-bit device or two 8-bit devices on a 16-bit bus,
  - Support for up to 16 simultaneous open pages for DDR2
  - One clock pair to support up to 4 DRAM devices
  - Supports auto refresh
  - On-the-fly power management using CKE
- Enhanced local bus controller (eLBC)
  - Multiplexed 26-bit address and 8-/16-bit data operating at up to 66 MHz
  - Eight chip selects supporting eight external slaves
    - Four chip selects dedicated
    - Four chip selects offered as multiplexed option
  - Supports boot from parallel NOR Flash and parallel NAND Flash
  - Supports programmable clock ratio dividers
  - Up to eight-beat burst transfers
  - 16- and 8-bit ports, separate $\overline{\text{LWE}}$ for each 8 bit
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Variable memory block sizes for FCM, GPCM, and UPM mode
  - Default boot ROM chip select with configurable bus width (8 or 16)
  - Provides two Write Enable signals to allow single byte write access to external 16-bit eLBC slave devices
- Integrated programmable interrupt controller (IPIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for external and internal discrete interrupt sources

  - Programmable highest priority request
  - Six groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Unique vector number for each interrupt source
- Enhanced secure digital host controller (eSDHC)
  - Compatible with the *SD Host Controller Standard Specification Version 2.0* with test event register support
  - Compatible with the *MMC System Specification Version 4.2*
  - Compatible with the *SD Memory Card Specification Version 2.0* and supports the high capacity SD memory card
  - Compatible with the *SD Input/Output (SDIO) Card Specification, Version 2.0*
  - Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, and RS-MMC cards
  - Card bus clock frequency up to 33.33 MHz.
  - Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    - Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  - Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
  - Up to 64 flexible message buffers of zero to eight bytes data length
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - Selectable backwards compatibility with previous FlexCAN module version
  - Programmable loop-back mode supporting self-test operation
  - Global network time, synchronized by a specific message
  - Independent of the transmission medium (an external transceiver is required)
  - Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8306. The MPC8306 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1} AV_{DD2} AV_{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.98	V	—
Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN, USB and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	2
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

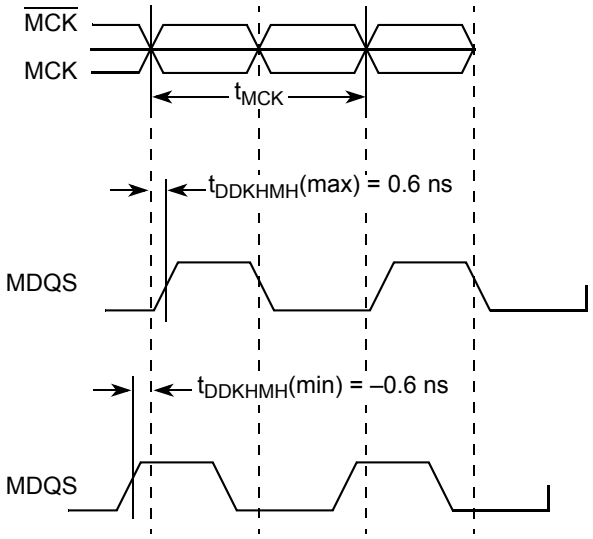


Figure 5. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

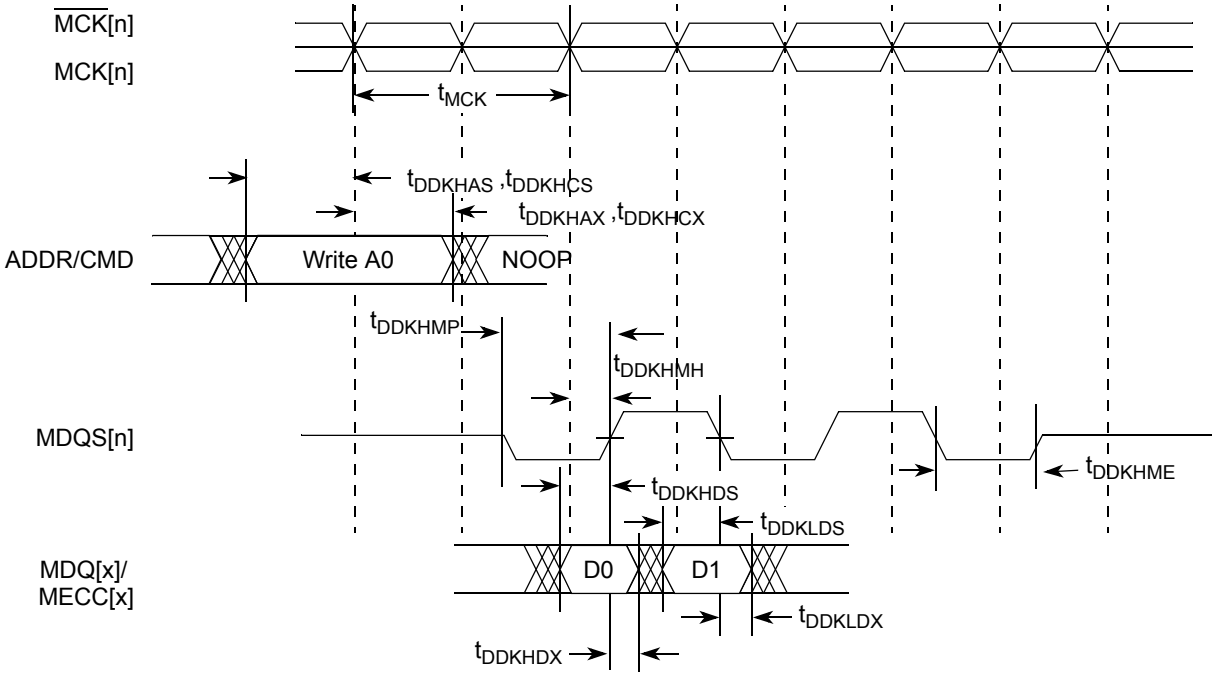


Figure 6. DDR2 SDRAM Output Timing Diagram

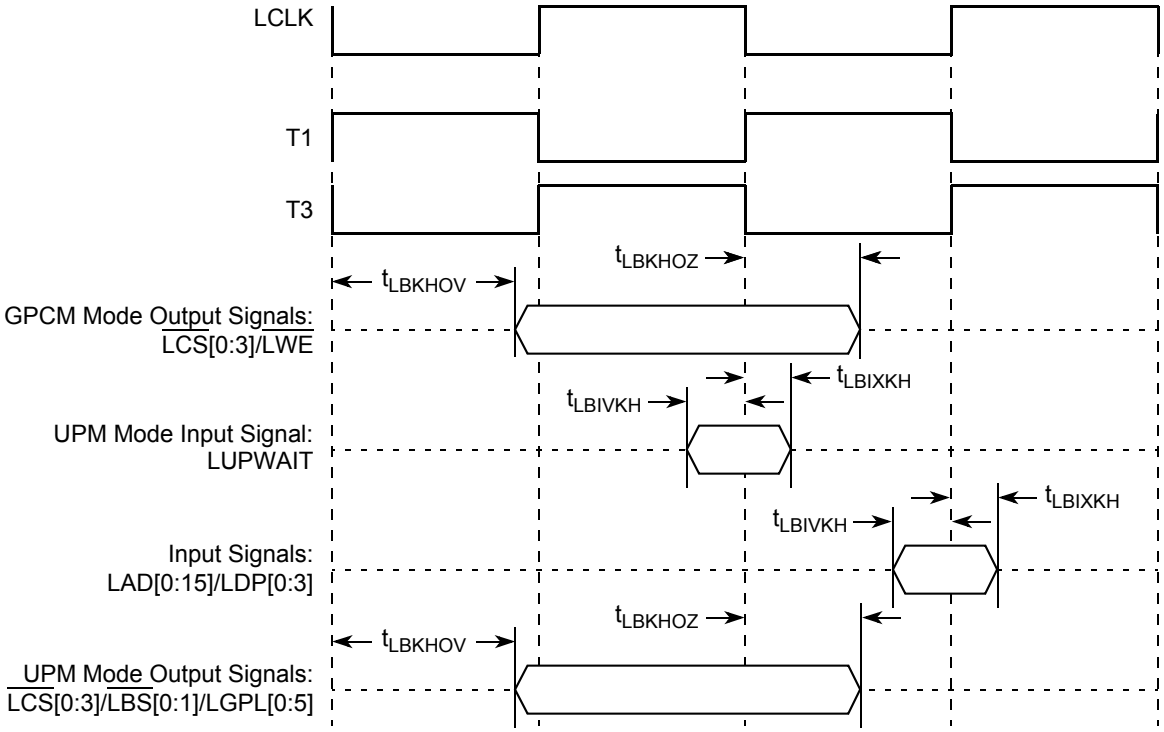


Figure 9. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

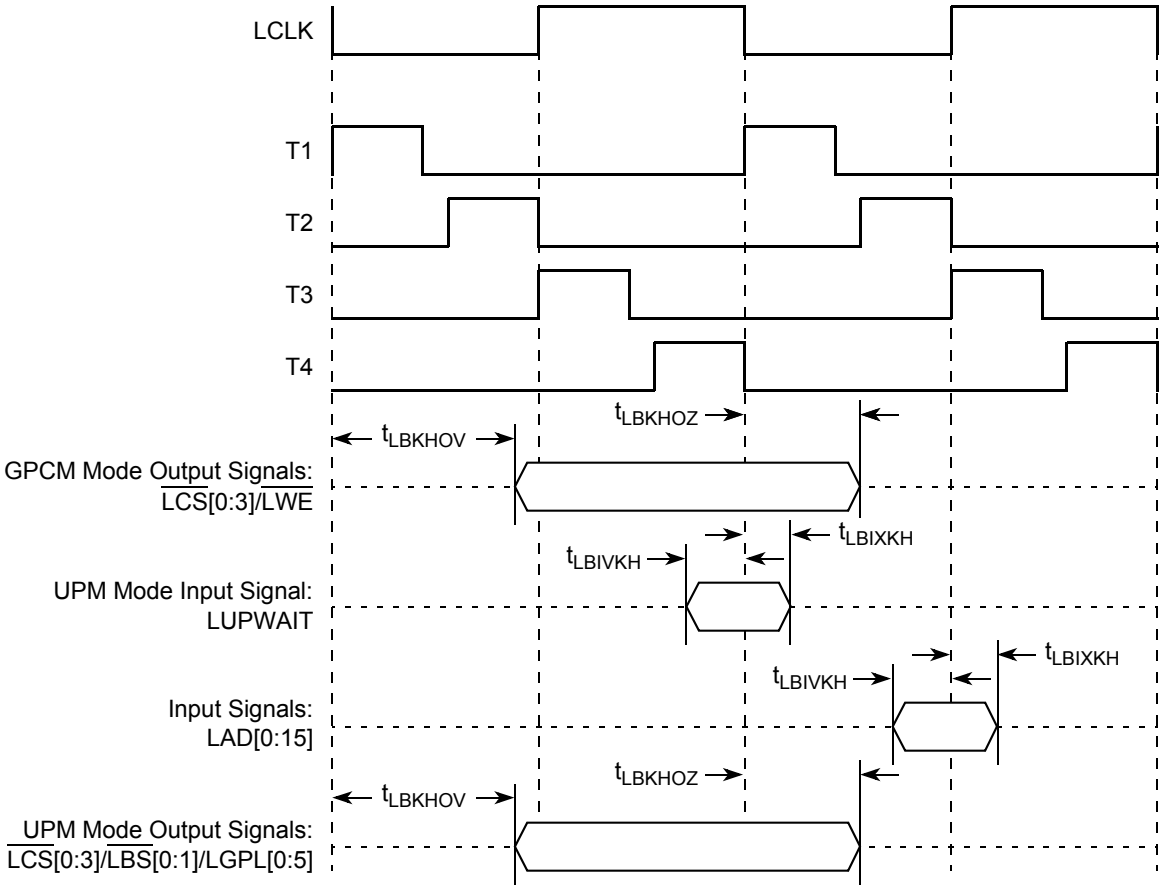


Figure 10. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet interfaces.

8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC (management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, “Ethernet Management Interface Electrical Characteristics.”

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in The following table.

9.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 29. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

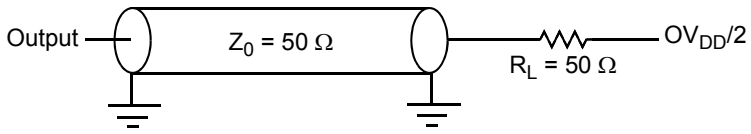
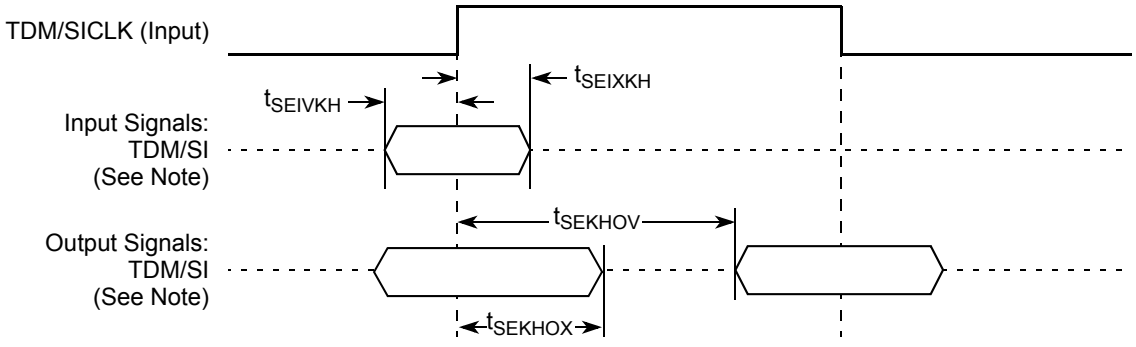


Figure 20. TDM/SI AC Test Load

The following figure represents the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 21. TDM/SI AC Timing (External Clock) Diagram

10 HDLC

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), of the MPC8306.

12 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8306.

12.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface of the MPC8306.

Table 34. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

12.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface of the MPC8306.

Table 35. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

Table 37. eSDHC AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–33.25 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

The following figure provides the eSDHC clock input timing diagram.

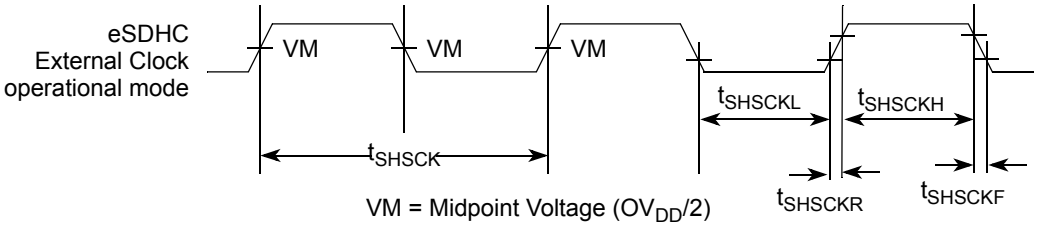


Figure 27. eSDHC Clock Input Timing Diagram

The following figure provides the data and command input/output timing diagram.

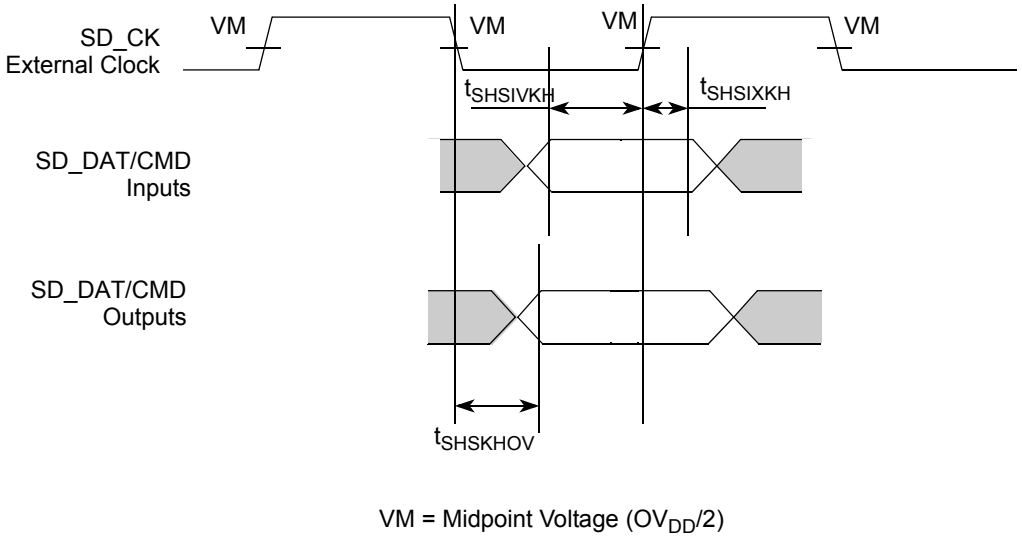


Figure 28. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

14 FlexCAN

This section describes the DC and AC electrical specifications for the FlexCAN interface.

14.1 FlexCAN DC Electrical Characteristics

The following table provides the DC electrical characteristics for the FlexCAN interface.

Table 38. FlexCAN DC Electrical Characteristics (3.3V)

For recommended operating conditions, see Table 2

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2.
2. OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

14.2 FlexCAN AC Timing Specifications

The following table provides the AC timing specifications for the FlexCAN interface.

Table 39. FlexCAN AC Timing Specifications

For recommended operating conditions, see Table 2

Parameter	Min	Max	Unit	Notes
Baud rate	10	1000	Kbps	—

Table 41. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 40).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8306 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

The following figure provides the AC test load for the I²C.

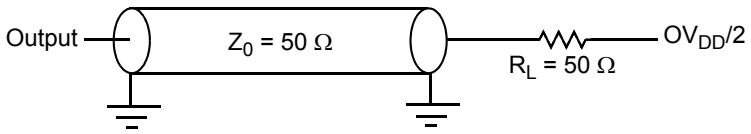


Figure 29. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

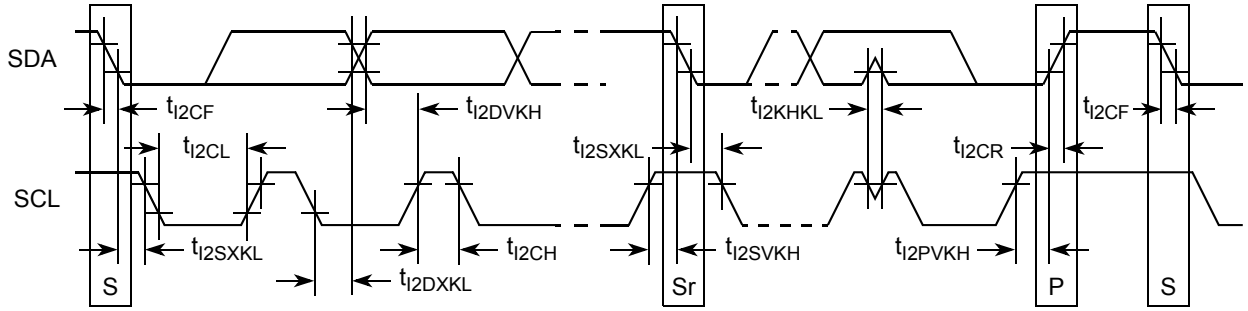


Figure 30. I²C Bus AC Timing Diagram

18 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8306.

18.1 IPIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins of the MPC8306.

Table 46. IPIC DC Electrical Characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output High Voltage	V_{OH}	I_{OL} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$, $\overline{\text{MCP\_OUT}}$, and QE ports Interrupts.
2. $\overline{\text{MCP\_OUT}}$ is open drain pins, thus V_{OH} is not relevant for those pins.

18.2 IPIC AC Timing Specifications

The following table provides the IPIC input and output AC timing specifications.

Table 47. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

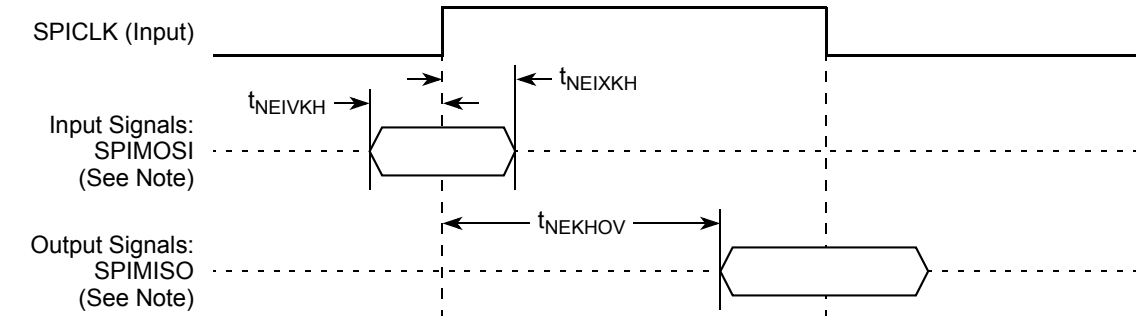
19 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8306.

19.1 SPI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306 SPI.

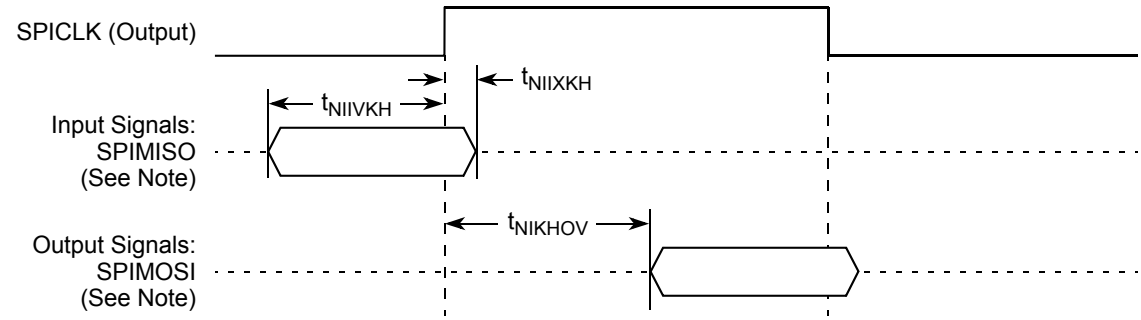
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8306.

20.1 JTAG DC Electrical Characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306.

Table 50. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 51. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	 5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	 5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 36). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

The following figure provides the AC test load for TDO and the boundary-scan outputs of the MPC8306.

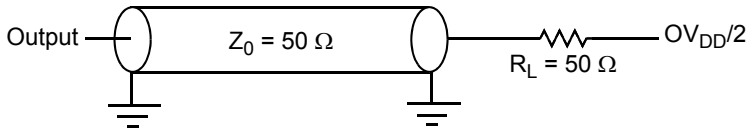


Figure 36. AC Test Load for the JTAG Interface

The following figure provides the JTAG clock input timing diagram.

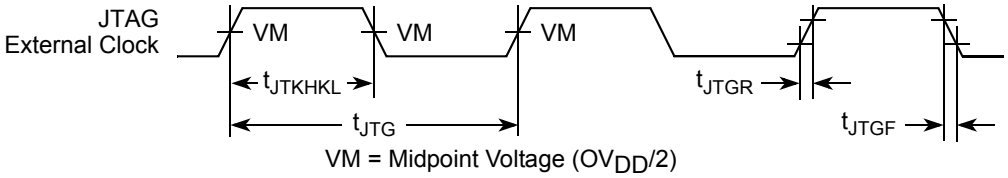


Figure 37. JTAG Clock Input Timing Diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

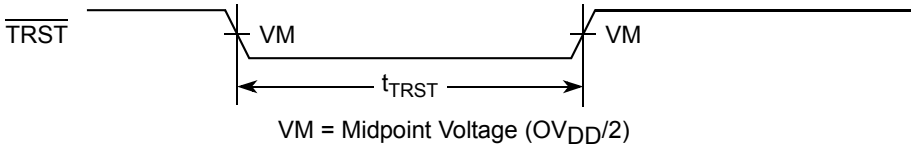


Figure 38. $\overline{\text{TRST}}$ Timing Diagram

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[17]	B14	O	OV_{DD}	—
LA[18]	A14	O	OV_{DD}	—
LA[19]	A15	O	OV_{DD}	—
LA[20]	A16	O	OV_{DD}	—
LA[21]	B16	O	OV_{DD}	—
LA[22]	A17	O	OV_{DD}	—
LA[23]	B17	O	OV_{DD}	—
LA[24]	A18	O	OV_{DD}	—
LA[25]	B19	O	OV_{DD}	—
LCS_B[0]	A19	O	OV_{DD}	3
LCS_B[1]	B20	O	OV_{DD}	3
LCS_B[2]	A20	O	OV_{DD}	3
LCS_B[3]	A21	O	OV_{DD}	3
LCLK[0]	D13	O	OV_{DD}	—
LGPL[0]/LFCLE	B22	O	OV_{DD}	—
LGPL[1]/LFALE	D16	O	OV_{DD}	—
LGPL[2]/LOE_B/LFRE_B	D19	O	OV_{DD}	—
LGPL[3]/LFWP_B	D17	O	OV_{DD}	—
LGPL[4]/LGTA_B/LUPWAIT/LFRB_B	E18	IO	OV_{DD}	—
LGPL[5]	E19	O	OV_{DD}	—
LWE_B[0]/LFWE_B[0]/LBS_B[0]	D15	O	OV_{DD}	—
LWE_B[1]/LBS_B[1]	D14	O	OV_{DD}	—
LBCTL	A22	O	OV_{DD}	—
LALE	B23	O	OV_{DD}	—
JTAG				
TCK	A3	I	OV_{DD}	—
TDI	B5	I	OV_{DD}	3
TDO	D7	O	OV_{DD}	—
TMS	A4	I	OV_{DD}	3
TRST_B	D8	I	OV_{DD}	3
Test Interface				
TEST_MODE	A5	I	OV_{DD}	—
System Control Signals				
HRESET_B	U20	IO	OV_{DD}	1
PORESET_B	V20	I	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USBDR_TXDRXD[7]/GPIO[37]/QE_BRG[11]	Y5	IO	OV_{DD}	—
DUART				
UART1_SOUT[1]/LSRCID4/LCS_B[4]	C23	O	OV_{DD}	—
UART1_SIN[1]/LDVAL/LCS_B[5]	F19	IO	OV_{DD}	—
UART1_SOUT[2]/UART1_RTS_B1/LCS_B[6]	D23	O	OV_{DD}	—
UART1_SIN[2]/UART1_CTS_B[1]/LCS_B[7]	D22	IO	OV_{DD}	—
Interrupts				
IRQ_B0_MCP_IN_B/CE_PI_0	E20	IO	OV_{DD}	—
IRQ_B1/MCP_OUT_B	E23	IO	OV_{DD}	—
IRQ_B2/CKSTOP_OUT_B	E22	IO	OV_{DD}	—
IRQ_B3/CKSTOP_IN_B	F20	I	OV_{DD}	—
I2C / SPI				
IIC_SDA1	G20	IO	OV_{DD}	2
IIC_SCL1	J20	IO	OV_{DD}	2
LCLK1/IIC_SCL2/CKSTOP_IN_B	H20	IO	OV_{DD}	2
SPISEL_BOOT/IIC_SDA2/CKSTOP_OUT_B	F23	O	OV_{DD}	2
SPIMOSI/LSRCID[2]	G22	IO	OV_{DD}	—
SPIMISO/LSRCID[3]	K20	IO	OV_{DD}	—
SPICLK/LSRCID[0]	G23	IO	OV_{DD}	—
SPISEL/LSRCID[1]	H22	I	OV_{DD}	—
FEC Management				
FEC_MDC	H23	O	OV_{DD}	—
FEC_MDIO	L20	IO	OV_{DD}	—
FEC1/GTM/GPIO				
FEC1_COL/GTM1_TIN[1]/GPIO[16]	AB20	IO	OV_{DD}	—
FEC1_CRS/GTM1_TGATE1_B/GPIO[17]	AC21	IO	OV_{DD}	—
FEC1_RX_CLK/GPIO[18]	Y17	IO	OV_{DD}	—
FEC1_RX_DV/GTM1_TIN[2]/GPIO[19]	Y18	IO	OV_{DD}	—
FEC1_RX_ER/GTM1_TGATE[2]_B/GPIO[20]	AB19	IO	OV_{DD}	—
FEC1_RXD0/GPIO[21]	AC20	IO	OV_{DD}	—
FEC1_RXD1/GTM1_TIN[3]/GPIO[22]	AC19	IO	OV_{DD}	—
FEC1_RXD2/GTM1_TGATE[3]_B/GPIO[23]	AC18	IO	OV_{DD}	—
FEC1_RXD3/GPIO[24]	AB17	IO	OV_{DD}	—
FEC1_TX_CLK/GTM1_TIN4/GPIO[25]	Y15	IO	OV_{DD}	—
FEC1_TX_EN/GTM1_TGATE[4]_B/GPIO[26]	Y16	IO	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FEC1_TX_ER/GTM1_TOUT[4]_B/GPIO[27]	AC17	IO	OV_{DD}	—
FEC1_TXD0/GTM1_TOUT[1]_B/GPIO[28]	AB16	IO	OV_{DD}	—
FEC1_TXD1/GTM1_TOUT[2]_B/GPIO[29]	AC16	IO	OV_{DD}	—
FEC1_TXD2/GTM1_TOUT[3]_B/GPIO[30]	AC15	IO	OV_{DD}	—
FEC1_TXD3/GPIO[31]	AB14	IO	OV_{DD}	—
FEC2/GPIO				
FEC2_COL/GPIO[32]	AC14	IO	OV_{DD}	—
FEC2_CRS/GPIO[33]	AB13	IO	OV_{DD}	—
FEC2_RX_CLK/GPIO[34]	Y14	IO	OV_{DD}	—
FEC2_RX_DV/GPIO[35]	AC13	IO	OV_{DD}	—
FEC2_RX_ER/GPIO[36]	Y13	IO	OV_{DD}	—
FEC2_RXD0/GPIO[37]	AC12	IO	OV_{DD}	—
FEC2_RXD1/GPIO[38]	AB11	IO	OV_{DD}	—
FEC2_RXD2/GPIO[39]	AC11	IO	OV_{DD}	—
FEC2_RXD3/GPIO[40]	AB10	IO	OV_{DD}	—
FEC2_TX_CLK/GPIO[41]	Y12	IO	OV_{DD}	—
FEC2_TX_EN/GPIO[42]	AC10	IO	OV_{DD}	—
FEC2_TX_ER/GPIO[43]	AC9	IO	OV_{DD}	—
FEC2_TXD0/GPIO[44]	AC8	IO	OV_{DD}	—
FEC2_TXD1/GPIO[45]	Y11	IO	OV_{DD}	—
FEC2_TXD2/GPIO[46]	AC7	IO	OV_{DD}	—
FEC2_TXD3/GPIO[47]	Y10	IO	OV_{DD}	—
FEC3/GPIO				
FEC3_COL/GPIO[48]	J23	IO	OV_{DD}	—
FEC3_CRS/GPIO[49]	K23	IO	OV_{DD}	—
FEC3_RX_CLK/GPIO[50]	M20	IO	OV_{DD}	—
FEC3_RX_DV/GPIO[51]	K22	IO	OV_{DD}	—
FEC3_RX_ER/GPIO[52]	L22	IO	OV_{DD}	—
FEC3_RXD0/GPIO[53]	L23	IO	OV_{DD}	—
FEC3_RXD1GPIO[54]	M23	IO	OV_{DD}	—
FEC3_RXD2/FEC_TMR_TRIG1/GPIO[55]	N22	IO	OV_{DD}	—
FEC3_RXD3/FEC_TMR_TRIG2/GPIO[56]	N23	IO	OV_{DD}	—
FEC3_TX_CLK/FEC_TMR_CLK/GPIO[57]	N20	IO	OV_{DD}	—
FEC3_TX_EN/FEC_TMR_GCLK/GPIO[58]	P20	IO	OV_{DD}	—
FEC3_TX_ER/FEC_TMR_PP1/GPIO[59]	P22	IO	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	H8,H9,H10,H11,H12,H13,H14,H15,H16,J8,J16,K8,K16,M8,N16,P8,P16,R8,R16,T8,T9,T10,T11,T12,T13,T14,T15,T16	—	—	—
VSS	A1,B4,B6,B9,B12,B15,B18,B21,C22,D2,D5,D18,D20,F2,F22,J2,J9,J10,J11,J12,J13,J14,J15,J22,K4,K9,K10,K11,K12,K13,K14,K15,L9,L10,L11,L12,L13,L14,L15,M2,M9,M10,M11,M12,M13,M14,M15,M22,N9,N10,N11,N12,N13,N14,N15,P9,P10,P11,P12,P13,P14,P15,R2,R9,R10,R11,R12,R13,R14,R15,R22,T4,V2,V19,V22,W4,Y19,AA2,AA22,AB4,AB6,AB9,AB12,AB15,AB18,AB21,AC1,AC23	—	—	—
NC	A23	—	—	—

Notes
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2-10 kΩ) should be placed on this pin to OV_{DD}
3. This pin has weak pull-up that is always enabled.

22.1 System Clock Domains

As shown in Figure 42, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create four major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*qe_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lbc_clk*)

The *csb_clk* frequency is derived from the following equation:

$$\textbf{\textit{csb\_clk}} = \text{SYS\_CLK\_IN} \times \text{SPMF} \qquad \textbf{Eqn. 1}$$

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset Configuration chapter in the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

The *qe_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF]) and the QUICC Engine PLL division factor (RCWL[CEPDF]) as the following equation:

$$\text{qe\_clk} = (\text{QE\_CLK\_IN} \times \text{CEPMF}) \div (1 + \text{CEPDF}) \qquad \textbf{Eqn. 2}$$

$$\textbf{\textit{qe\_clk} = (QE\_CLK\_IN} \times \textbf{CEPMF)} \div \textbf{(1 + CEPDF)} \qquad \textbf{Eqn. 3}$$

For more information, see the QUICC Engine PLL Multiplication Factor section and the “QUICC Engine PLL Division Factor” section in the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LCLK). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. For more information, see the LBC Bus Clock and Clock Ratios section in the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

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