E·XFL

# NXP Semiconductors - MPC8306VMACDCA Datasheet



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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 200MHz |
| Co-Processors/DSP | Communications; QUICC Engine |
| RAM Controllers | DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (3) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 1.8V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 369-LFBGA |
| Supplier Device Package | 369-PBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8306vmacdca |

— Programmable highest priority request
— Six groups of interrupts with programmable priority
— External and internal interrupts directed to host processor
— Unique vector number for each interrupt source

- Enhanced secure digital host controller (eSDHC)
  — Compatible with the *SD Host Controller Standard Specification Version 2.0* with test event register support
  — Compatible with the *MMC System Specification Version 4.2*
  — Compatible with the *SD Memory Card Specification Version 2.0* and supports the high capacity SD memory card
  — Compatible with the *SD Input/Output (SDIO) Card Specification, Version 2.0*
  — Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, and RS-MMC cards
  — Card bus clock frequency up to 33.33 MHz.
  — Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    – Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  — Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  — Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  — Supports operation as a stand-alone USB host controller
  — Supports operation as a stand-alone USB device
  — Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  — Full implementation of the CAN protocol specification version 2.0B
  — Up to 64 flexible message buffers of zero to eight bytes data length
  — Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  — Selectable backwards compatibility with previous FlexCAN module version
  — Programmable loop-back mode supporting self-test operation
  — Global network time, synchronized by a specific message
  — Independent of the transmission medium (an external transceiver is required)
  — Short latency time due to an arbitration scheme for high-priority messages
- Dual $I^2C$ interfaces
  — Two-wire interface
  — Multiple-master support
  — Master or slave $I^2C$ mode support
  — On-chip digital filtering rejects spikes on the bus
  — $I^2C1$ can be used as the boot sequencer

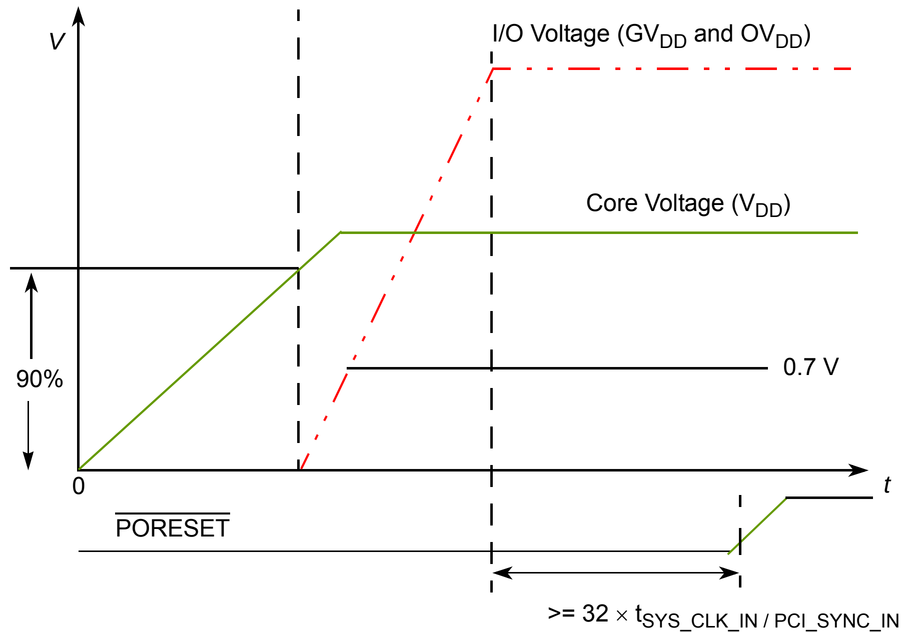



**Figure 3. MPC8306 Power-Up Sequencing Example**

# 3 Power Characteristics

The typical power dissipation for this family of MPC8306 devices is shown in the following table.

**Table 5. MPC8306 Power Dissipation**

| Core Frequency (MHz) | QUICC Engine Frequency (MHz) | CSB Frequency (MHz) | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| 133 | 133 | 133 | 0.272 | 0.618 | W | 1, 2, 3 |
| 200 | 233 | 133 | 0.291 | 0.631 | W | 1, 2, 3 |
| 266 | 233 | 133 | 0.451 | 0.925 | W | 1, 2, 3 |
| 333 | 233 | 133 | 0.471 | 0.950 | W | 1, 2, 3 |

**Notes:**

1. The values do not include I/O supply power ($OV_{DD}$ and $GV_{DD}$), but it does include $V_{DD}$ and $AV_{DD}$ power. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of $V_{DD}$ = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.
3. Maximum power is based on a voltage of $V_{DD}$ = 1.05 V, WC process, a junction $T_J$ = 105°C, and a smoke test code.

## 4.2 AC Electrical Characteristics

The primary clock source for the MPC8306 is SYS_CLK_IN. The following table provides the clock input (SYS_CLK_IN) AC timing specifications for the MPC8306. These specifications are also applicable for QE_CLK_IN.

**Table 8. SYS_CLK_IN AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SYS_CLK_IN frequency | $f_{SYS\_CLK\_IN}$ | 24 | — | 66.67 | MHz | 1 |
| SYS_CLK_IN cycle time | $t_{SYS\_CLK\_IN}$ | 15 | — | 41.6 | ns | — |
| SYS_CLK_IN rise and fall time | $t_{KH}$, $t_{KL}$ | 1.1 | — | 2.8 | ns | 2 |
| SYS_CLK_IN duty cycle | $t_{KHK}/t_{SYS\_CLK\_IN}$ | 40 | — | 60 | % | 3 |
| SYS_CLK_IN jitter | — | — | — | ±150 | ps | 4, 5 |

**Notes:**
1. **Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

# 5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8306. The following table provides the reset initialization AC timing specifications for the reset component(s).

**Table 9. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Note |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow | 32 | — | $t_{SYS\_CLK\_IN}$ | 1 |
| Required assertion time of PORESET with stable clock applied to SYS_CLK_IN | 32 | — | $t_{SYS\_CLK\_IN}$ | 1 |
| $\overline{\text{HRESET}}$ assertion (output) | 512 | — | $t_{SYS\_CLK\_IN}$ | 1 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$ | 4 | — | $t_{SYS\_CLK\_IN}$ | 1, 2 |
| Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | 1, 2 |

**Notes:**
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
2. POR configuration signals consist of CFG_RESET_SOURCE[0:3].

**Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V (continued)**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Output high current ($V_{OUT}$ = 1.35 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**

1. $GV_{DD}$ is expected to be within 50 mV of the DRAM $GV_{DD}$ at all times.
2. MVREF is expected to be equal to 0.5 × $GV_{DD}$, and to track $GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ $GV_{DD}$.

The following table provides the DDR2 capacitance when $GV_{DD}$(typ) = 1.8 V.

**Table 13. DDR2 SDRAM Capacitance for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**

1. This parameter is sampled. $GV_{DD}$ = 1.8 V ± 0.100 V, f = 1 MHz, $T_A$ = 25 °C, $V_{OUT}$ = $GV_{DD}$ ÷ 2, $V_{OUT}$ (peak-to-peak) = 0.2 V.

## 6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

### 6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM ($GV_{DD}$(typ) = 1.8 V).

**Table 14. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with $GV_{DD}$ of 1.8 V± 100mV.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | MVREF – 0.25 | V | — |
| AC input high voltage | $V_{IH}$ | MVREF + 0.25 | — | V | — |

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

**Table 15. DDR2 SDRAM Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8V ± 100mV.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Controller skew for MDQS—MDQ/MDM | $t_{CISKEW}$ | | | ps | 1, 2 |

**Table 15. DDR2 SDRAM Input AC Timing Specifications (continued)**

At recommended operating conditions with $GV_{DD}$ of 1.8V ± 100mV.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| 266 MHz | | –750 | 750 | | |

**Notes:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$. This can be determined by the equation: $t_{DISKEW}$ = ±(T/4 – abs($t_{CISKEW}$)) where T is the clock period and abs($t_{CISKEW}$) is the absolute value of $t_{CISKEW}$.

The following figure shows the input timing diagram for the DDR controller.

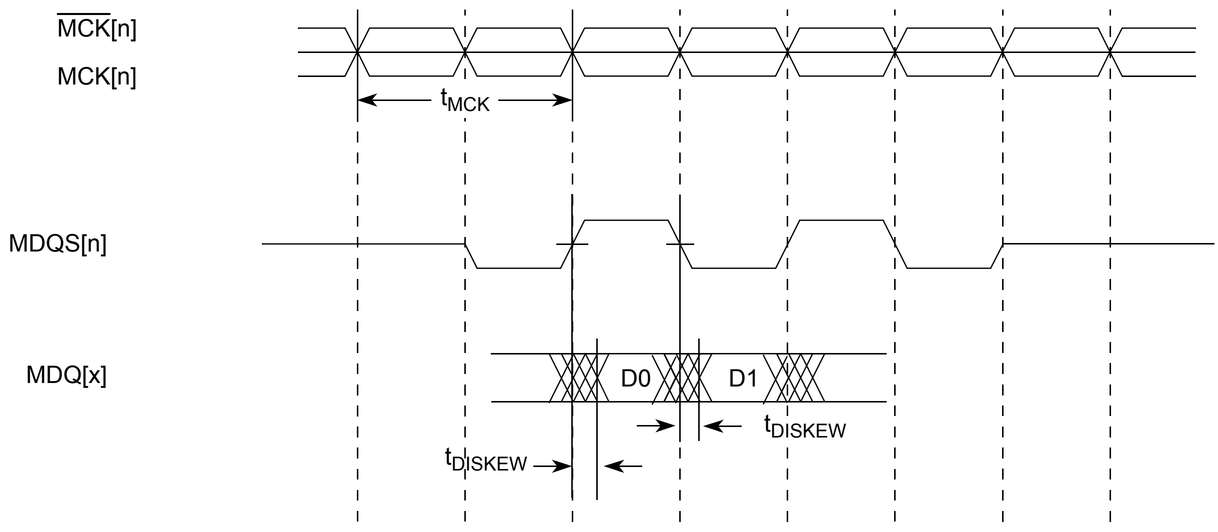



**Figure 4. DDR Input Timing Diagram**

## 6.2.2 DDR2 SDRAM Output AC Timing Specifications

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

**Table 16. DDR2 SDRAM Output AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8V ± 100mV.

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| MCK cycle time, (MCK/$\overline{\text{MCK}}$ crossing) | $t_{MCK}$ | 5.988 | 8 | ns | 2 |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$ | | | ns | 3 |
| 266 MHz | | 2.5 | — | | |
| ADDR/CMD output hold with respect to MCK | $t_{DDKHAX}$ | | | ns | 3 |
| 266 MHz | | 2.5 | — | | |
| $\overline{\text{MCS}}$ output setup with respect to MCK | $t_{DDKHCS}$ | | | ns | 3 |
| 266 MHz | | 2.5 | — | | |

The following figure provides the AC test load for the local bus.

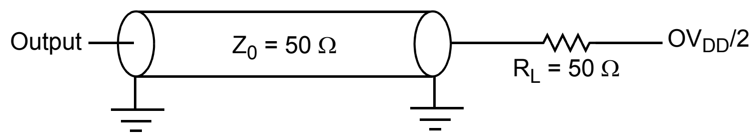



**Figure 7. Local Bus AC Test Load**

The following figures show the local bus signals. These figures has been given indicate timing parameters only and do not reflect actual functional operation of interface.

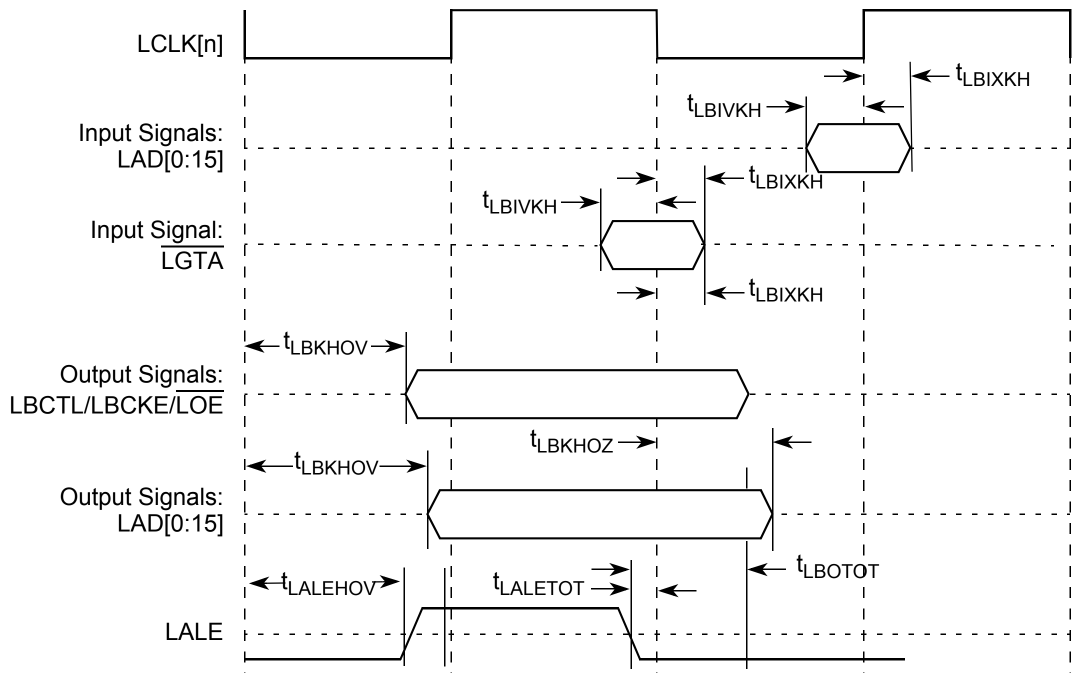



**Figure 8. Local Bus Signals**

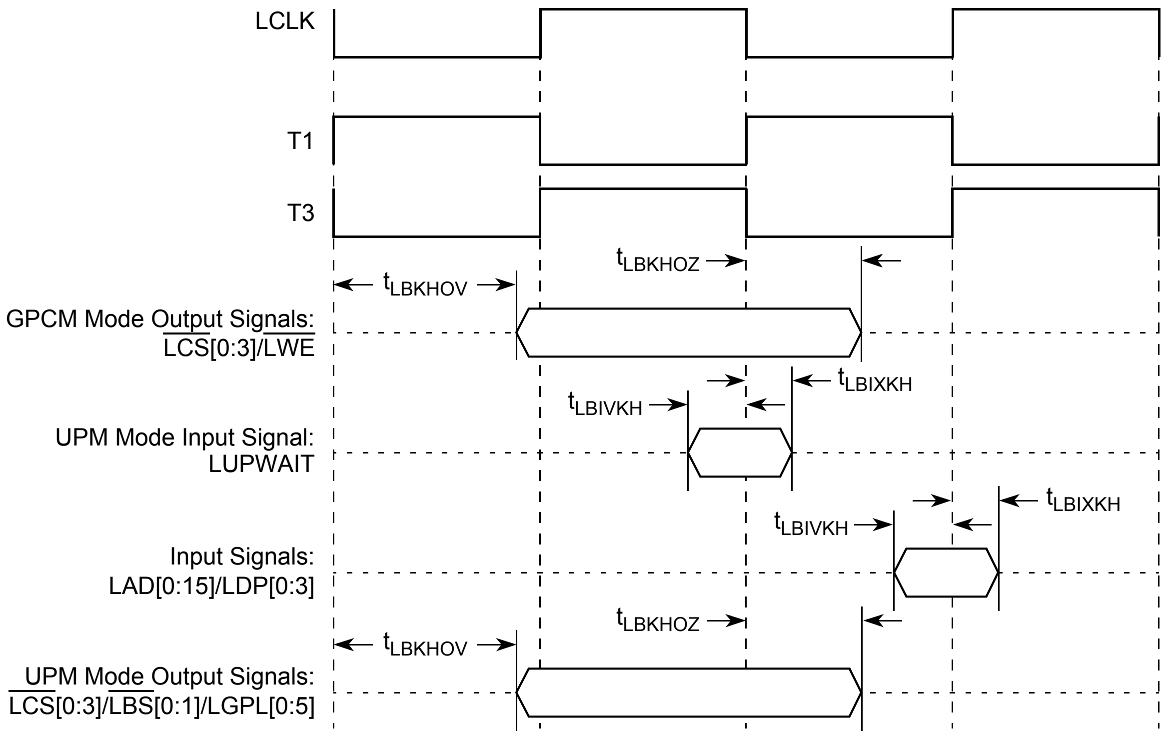



**Figure 9. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2**

The following figure shows the RMII transmit AC timing diagram.

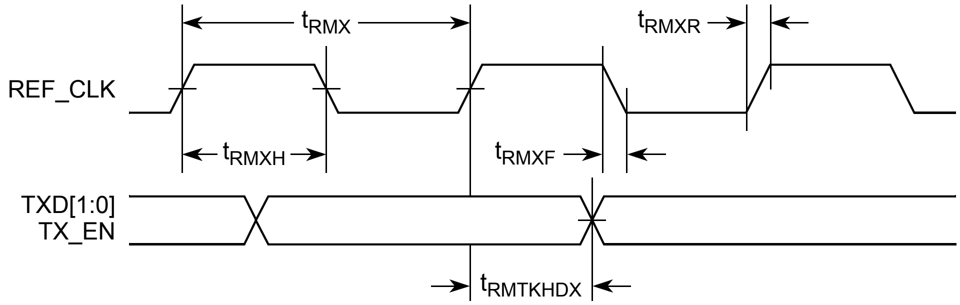



**Figure 15. RMII Transmit AC Timing Diagram**

### 8.2.2.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

**Table 23. RMII Receive AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 300mV.

| Parameter/Condition | Symbol[1] | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock period | $t_{RMX}$ | — | 20 | — | ns |
| REF_CLK duty cycle | $t_{RMXH}/t_{RMX}$ | 35 | — | 65 | % |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK | $t_{RMRDVKH}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK | $t_{RMRDXKH}$ | 2.0 | — | — | ns |
| REF_CLK clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{RMXR}$ | 1.0 | — | 4.0 | ns |
| REF_CLK clock fall time $V_{IH}$(max) to $V_{IL}$(min) | $t_{RMXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{RMX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{RMX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{RMX}$ represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

## 9.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

**Table 29. TDM/SI AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| TDM/SI outputs—External clock delay | $t_{SEKHOV}$ | 2 | 14 | ns |
| TDM/SI outputs—External clock High Impedance | $t_{SEKHOX}$ | 2 | 10 | ns |
| TDM/SI inputs—External clock input setup time | $t_{SEIVKH}$ | 5 | — | ns |
| TDM/SI inputs—External clock input hold time | $t_{SEIXKH}$ | 2 | — | ns |

**Notes:**
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SEKHOX}$ symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

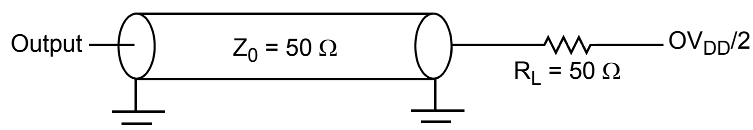
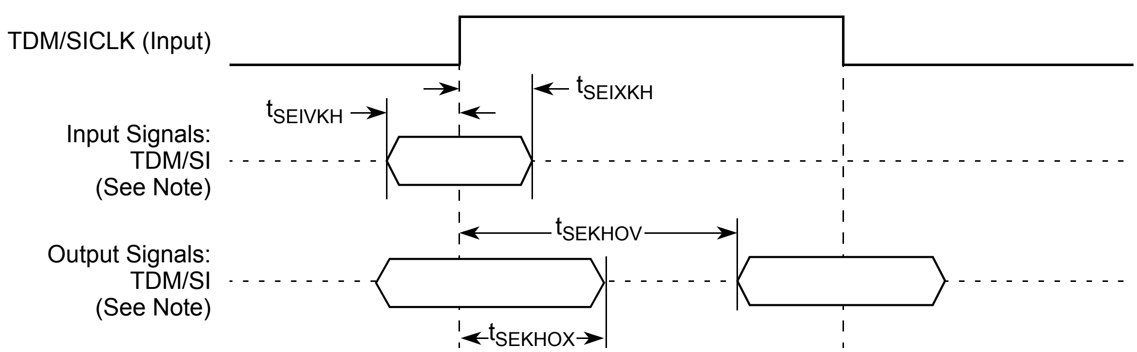



**Figure 20. TDM/SI AC Test Load**

The following figure represents the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.




**Note:** The clock edge is selectable on TDM/SI.

**Figure 21. TDM/SI AC Timing (External Clock) Diagram**

# 10 HDLC

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), of the MPC8306.

## 10.1 HDLC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306 HDLC protocol.

**Table 30. HDLC DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –2.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.5 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | — | ±5 | μA |

## 10.2 HDLC AC Timing Specifications

The following table provides the input and output AC timing specifications for HDLC protocol.

**Table 31. HDLC AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| Outputs—Internal clock delay | $t_{HIKHOV}$ | 0 | 9 | ns |
| Outputs—External clock delay | $t_{HEKHOV}$ | 1 | 12 | ns |
| Outputs—Internal clock high impedance | $t_{HIKHOX}$ | 0 | 5.5 | ns |
| Outputs—External clock high impedance | $t_{HEKHOX}$ | 1 | 8 | ns |
| Inputs—Internal clock input setup time | $t_{HIIVKH}$ | 9 | — | ns |
| Inputs—External clock input setup time | $t_{HEIVKH}$ | 4 | — | ns |
| Inputs—Internal clock input hold time | $t_{HIIXKH}$ | 0 | — | ns |
| Inputs—External clock input hold time | $t_{HEIXKH}$ | 1 | — | ns |

**Notes:**
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{HIKHOX}$ symbolizes the outputs internal timing (HI) for the time $t_{serial}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load.

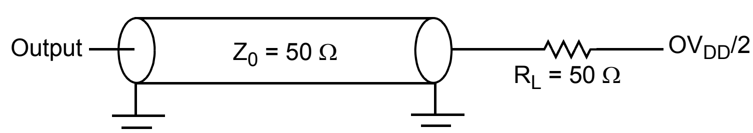



**Figure 22. AC Test Load**

Figure 23 and Figure 24 represent the AC timing from Table 31. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the timing with external clock.

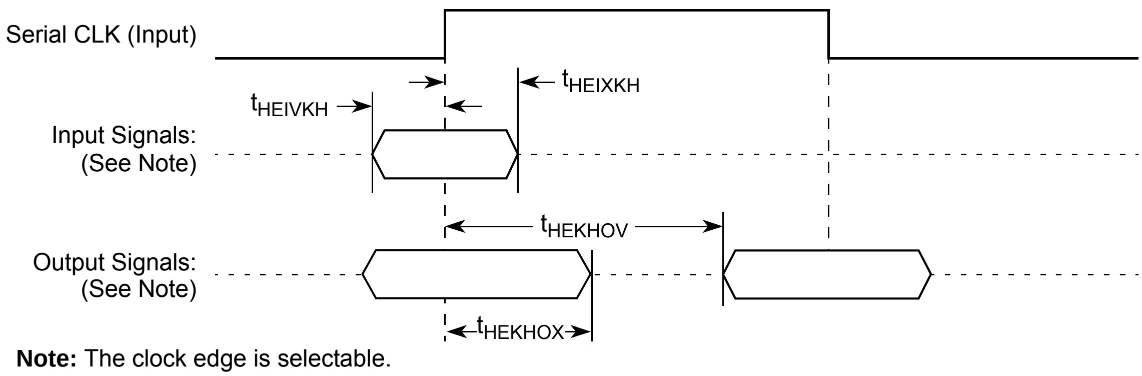



**Figure 23. AC Timing (External Clock) Diagram**

The following figure shows the timing with internal clock.

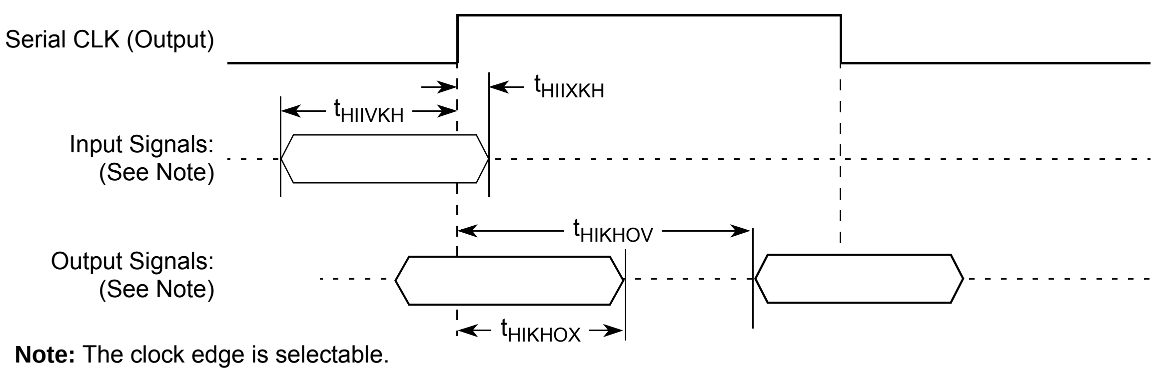



**Figure 24. AC Timing (Internal Clock) Diagram**

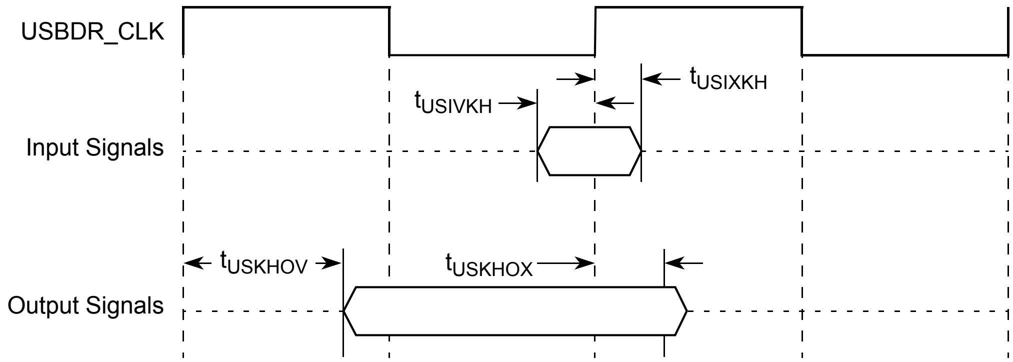
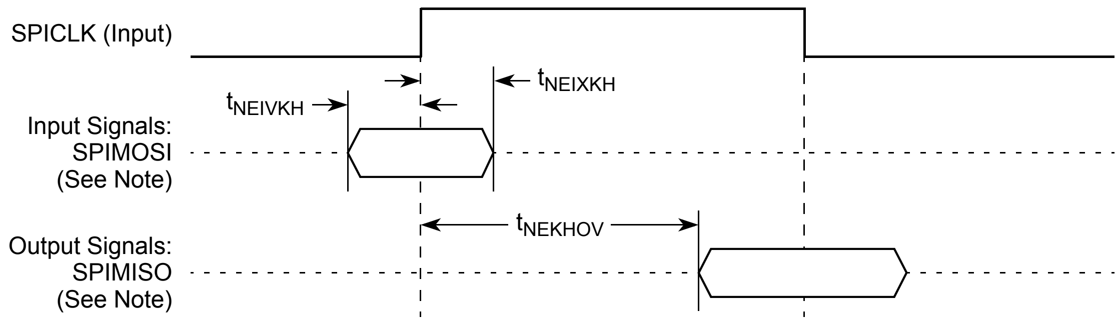



**Figure 26. USB Signals**

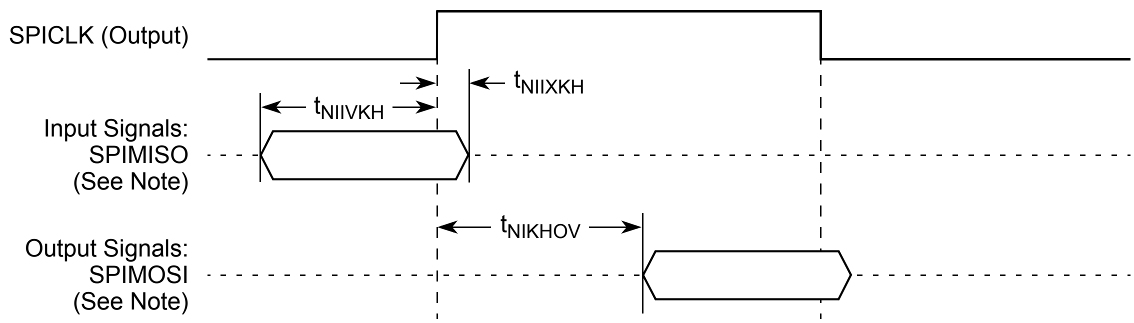
The following figure shows the SPI timing in slave mode (external clock).




**Note:** The clock edge is selectable on SPI.

**Figure 34. SPI AC Timing in Slave Mode (External Clock) Diagram**

The following figure shows the SPI timing in master mode (internal clock).




**Note:** The clock edge is selectable on SPI.

**Figure 35. SPI AC Timing in Master Mode (Internal Clock) Diagram**

# 20 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8306.

## 20.1 JTAG DC Electrical Characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306.

**Table 50. JTAG Interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

**Table 52. MPC8306 Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| MEMC_MA[8] | T1 | O | $GV_{DD}$ | — |
| MEMC_MA[9] | P4 | O | $GV_{DD}$ | — |
| MEMC_MA[10] | L4 | O | $GV_{DD}$ | — |
| MEMC_MA[11] | T2 | O | $GV_{DD}$ | — |
| MEMC_MA[12] | U1 | O | $GV_{DD}$ | — |
| MEMC_MA[13] | U2 | O | $GV_{DD}$ | — |
| MEMC_MWE_B | K1 | O | $GV_{DD}$ | — |
| MEMC_MRAS_B | K2 | O | $GV_{DD}$ | — |
| MEMC_MCAS_B | J1 | O | $GV_{DD}$ | — |
| MEMC_MCS_B[0] | J4 | O | $GV_{DD}$ | — |
| MEMC_MCS_B[1] | H1 | O | $GV_{DD}$ | — |
| MEMC_MCKE[0] | U4 | O | $GV_{DD}$ | — |
| MEMC_MCK[0] | V1 | O | $GV_{DD}$ | — |
| MEMC_MCK_B[0] | W1 | O | $GV_{DD}$ | — |
| MEMC_MODT[0] | H2 | O | $GV_{DD}$ | — |
| MEMC_MODT[1] | H4 | O | $GV_{DD}$ | — |
| MEMC_MVREF | L8 | | $GV_{DD}$ | — |
| **Local Bus Controller Interface** | | | | |
| LAD[0] | B7 | IO | $OV_{DD}$ | — |
| LAD[1] | D9 | IO | $OV_{DD}$ | — |
| LAD[2] | A6 | IO | $OV_{DD}$ | — |
| LAD[3] | B8 | IO | $OV_{DD}$ | — |
| LAD[4] | A7 | IO | $OV_{DD}$ | — |
| LAD[5] | A8 | IO | $OV_{DD}$ | — |
| LAD[6] | A9 | IO | $OV_{DD}$ | — |
| LAD[7] | D10 | IO | $OV_{DD}$ | — |
| LAD[8] | B10 | IO | $OV_{DD}$ | — |
| LAD[9] | A10 | IO | $OV_{DD}$ | — |
| LAD[10] | B11 | IO | $OV_{DD}$ | — |
| LAD[11] | D12 | IO | $OV_{DD}$ | — |
| LAD[12] | D11 | IO | $OV_{DD}$ | — |
| LAD[13] | A11 | IO | $OV_{DD}$ | — |
| LAD[14] | A12 | IO | $OV_{DD}$ | — |
| LAD[15] | B13 | IO | $OV_{DD}$ | — |
| LA[16] | A13 | IO | $OV_{DD}$ | — |

Table 52. MPC8306 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $V_{DD}$ | H8,H9,H10,H11,H12,H13,H14,H15,H16,J8,J16,K8,K16,M8,N16,P8,P16,R8,R16,T8,T9,T10,T11,T12,T13,T14,T15,T16 | — | — | — |
| VSS | A1,B4,B6,B9,B12,B15,B18,B21,C22,D2,D5,D18,D20,F2,F22,J2,J9,J10,J11,J12,J13,J14,J15,J22,K4,K9,K10,K11,K12,K13,K14,K15,L9,L10,L11,L12,L13,L14,L15,M2,M9,M10,M11,M12,M13,M14,M15,M22,N9,N10,N11,N12,N13,N14,N15,P9,P10,P11,P12,P13,P14,P15,R2,R9,R10,R11,R12,R13,R14,R15,R22,T4,V2,V19,V22,W4,Y19,AA2,AA22,AB4,AB6,AB9,AB12,AB15,AB18,AB21,AC1,AC23 | — | — | — |
| NC | A23 | — | — | — |

**Notes**
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to $OV_{DD}$
2. This pin is an open drain signal. A weak pull-up resistor (2-10 kΩ) should be placed on this pin to $OV_{DD}$
3. This pin has weak pull-up that is always enabled.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset.

The following table specifies which units have a configurable clock frequency. For detailed description, refer to the "System Clock Control Register (SCCR)" section in the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

**Table 53. Configurable Clock Units**

| Unit | Default Frequency | Options |
|---|---|---|
| I2C,SDHC, USB, DMA Complex | *csb_clk* | Off, csb_clk, *csb_clk*/2, *csb_clk*/3 |

**NOTE**

Setting the clock ratio of these units must be performed prior to any access to them.

The following table provides the maximum operating frequencies for the MPC8306 MAPBGA under recommended operating conditions (see Table 2).

**Table 54. Operating Frequencies for MAPBGA**

| Characteristic[1] | Max Operating Frequency | Unit |
|---|---|---|
| e300 core frequency (*core_clk*) | 266 | MHz |
| Coherent system bus frequency (*csb_clk*) | 133 | MHz |
| QUICC Engine frequency (*qe_clk*) | 233 | MHz |
| DDR2 memory bus frequency (MCLK)[2] | 167 | MHz |
| Local bus frequency (LCLK*n*)[3] | 66 | MHz |

**Notes:**

1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting csb_clk, MCLK, LCLK, and core_clk frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR2 data rate is 2× the DDR2 memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the lb_clk frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the csb_clk frequency (depending on RCWL[LBCM]).

## 22.2 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 55 shows the multiplication factor encodings for the system PLL.

**NOTE**

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider). The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

As described in Section 22, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (*SYS_CLK_IN)* and the internal

**Table 55. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111–1111 | Reserved |

coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

**Table 56. CSB Frequency Options**

| SPMF | csb_clk : sys_clk_in Ratio | SYS_CLK_IN(MHz) | | |
|---|---|---|---|---|
| | | 25 | 33.33 | 66.67 |
| | | csb_clk Frequency (MHz) | | |
| 0010 | 2:1 | | | 133 |
| 0011 | 3:1 | | | |
| 0100 | 4:1 | | 133 | |
| 0101 | 5:1 | 125 | 167 | |
| 0110 | 6:1 | | | |

## 22.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

**Table 57. e300 Core PLL Configuration**

| RCWL[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider |
|---|---|---|---|---|
| 0-1 | 2-5 | 6 | | |
| nn | 0000 | n | PLL bypassed<br>(PLL off, *csb_clk* clocks core directly) | PLL bypassed<br>(PLL off, *csb_clk* clocks core directly) |
| 00 | 0001 | 0 | 1:1 | ÷2 |
| 01 | 0001 | 0 | 1:1 | ÷4 |
| 10 | 0001 | 0 | 1:1 | ÷8 |
| 11 | 0001 | 0 | 1:1 | ÷8 |

**Table 57. e300 Core PLL Configuration (continued)**

| RCWL[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider |
|---|---|---|---|---|
| 0-1 | 2-5 | 6 | | |
| 00 | 0001 | 1 | 1.5:1 | ÷ 2 |
| 01 | 0001 | 1 | 1.5:1 | ÷ 4 |
| 10 | 0001 | 1 | 1.5:1 | ÷ 8 |
| 11 | 0001 | 1 | 1.5:1 | ÷ 8 |
| 00 | 0010 | 0 | 2:1 | ÷ 2 |
| 01 | 0010 | 0 | 2:1 | ÷ 4 |
| 10 | 0010 | 0 | 2:1 | ÷ 8 |
| 11 | 0010 | 0 | 2:1 | ÷ 8 |
| 00 | 0010 | 1 | 2.5:1 | ÷ 2 |
| 01 | 0010 | 1 | 2.5:1 | ÷ 4 |
| 10 | 0010 | 1 | 2.5:1 | ÷ 8 |
| 11 | 0010 | 1 | 2.5:1 | ÷ 8 |
| 00 | 0011 | 0 | 3:1 | ÷ 2 |
| 01 | 0011 | 0 | 3:1 | ÷ 4 |
| 10 | 0011 | 0 | 3:1 | ÷ 8 |
| 11 | 0011 | 0 | 3:1 | ÷ 8 |

**NOTE**

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

## 22.4 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

**Table 58. QUICC Engine PLL Multiplication Factors**

| RCWL[CEPMF] | RCWL[CEPDF] | QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF) |
|---|---|---|
| 00000–00001 | 0 | Reserved |
| 00010 | 0 | × 2 |
| 00011 | 0 | × 3 |
| 00100 | 0 | × 4 |
| 00101 | 0 | × 5 |
| 00110 | 0 | × 6 |

# 23 Thermal

This section describes the thermal specifications of the MPC8306.

## 23.1 Thermal Characteristics

The following table provides the package thermal characteristics for the 369, 19 × 19 mm MAPBGA of the MPC8306.

**Table 61. Package Thermal Characteristics for MAPBGA**

| Characteristic | Board type | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction-to-ambient natural convection | Single-layer board (1s) | $R_{\theta JA}$ | 39 | °C/W | 1, 2 |
| Junction-to-ambient natural convection | Four-layer board (2s2p) | $R_{\theta JA}$ | 24 | °C/W | 1, 2, 3 |
| Junction-to-ambient (@200 ft/min) | Single-layer board (1s) | $R_{\theta JMA}$ | 32 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) | Four-layer board (2s2p) | $R_{\theta JMA}$ | 21 | °C/W | 1, 3 |
| Junction-to-board | — | $R_{\theta JB}$ | 14 | °C/W | 4 |
| Junction-to-case | — | $R_{\theta JC}$ | 9 | °C/W | 5 |
| Junction-to-package top | Natural convection | $\Psi_{JT}$ | 2 | °C/W | 6 |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 23.1.1 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

### 23.1.2 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, can be obtained from the equation:

$$T_J = T_A + (R_{\theta J A} \times P_D) \qquad \text{Eqn. 1}$$

where:

$T_J$ = junction temperature (°C)

lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

### 23.2.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface.

From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance using the following equation:

$$T_J = T_C + (R_{\theta JC} \times P_D) \qquad \textit{Eqn. 5}$$

where:

$T_C$ = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$P_D$ = power dissipation (W)

# 24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8306.

## 24.1 System Clocking

The MPC8306 includes three PLLs.

- The system PLL ($AV_{DD2}$) generates the system clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the system and SYS_CLK_IN is selected using the system PLL ratio configuration bits as described in Section 22.2, "System PLL Configuration."
- The e300 core PLL ($AV_{DD3}$) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 22.3, "Core PLL Configuration."
- The QUICC Engine PLL ($AV_{DD1}$) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.