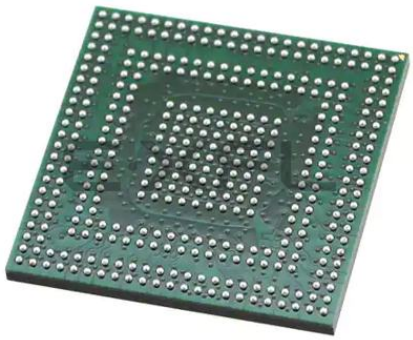

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8306vmaddca

1 Overview

The MPC8306 incorporates the e300c3 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8306 also includes two DMA engines and a 16-bit DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8306. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8306 is shown in the following figure.

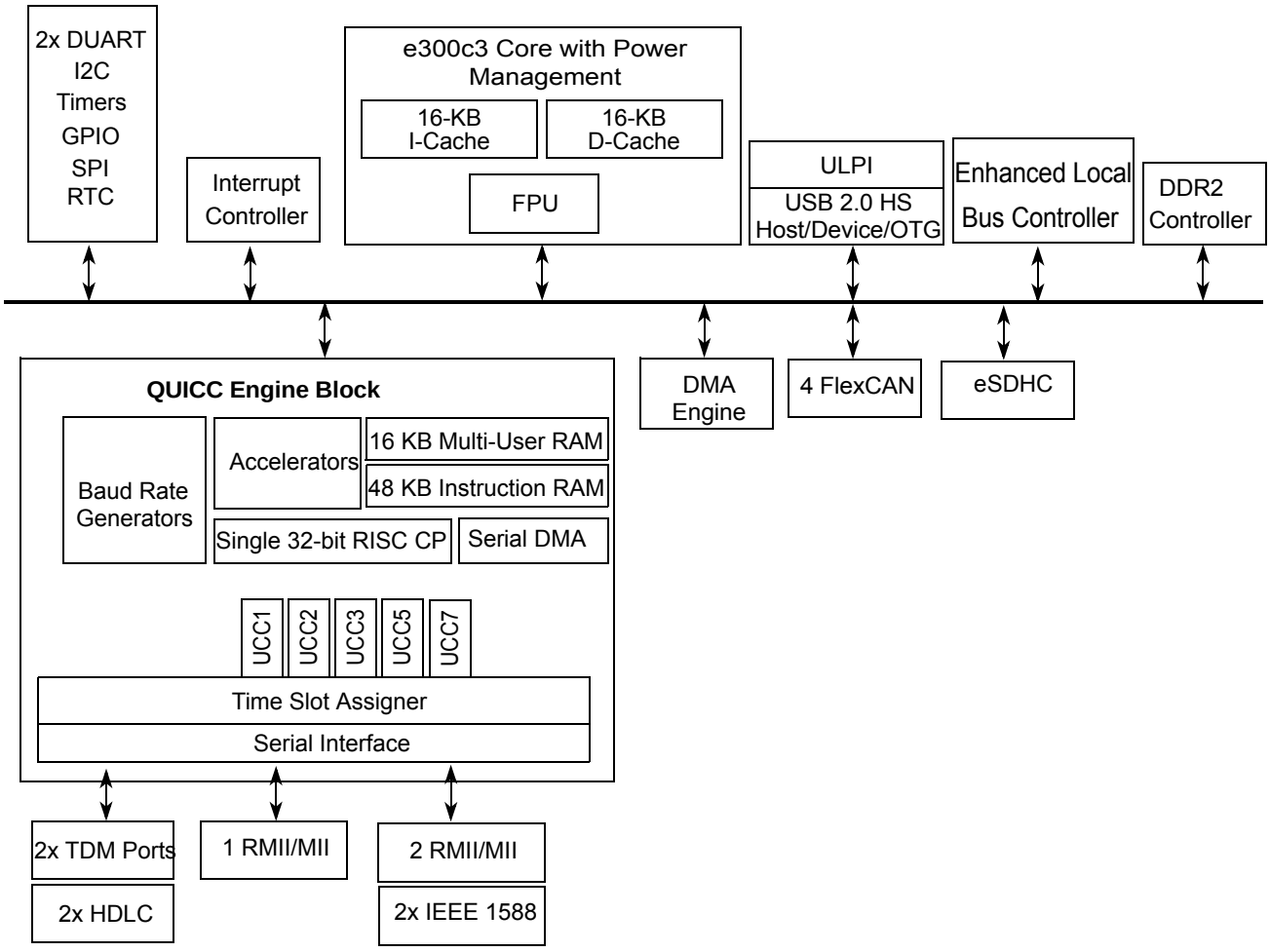

Figure 1. MPC8306 Block Diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, IEEE-1588, HDLC and TDM.

  - Asynchronous HDLC (bit rate up to 2 Mbps)
  - Two TDM interfaces supporting up to 128 QUICC multichannel controller channels, each running at 64 kbps

  For more information on QUICC Engine sub-modules, see *QUICC Engine Block Reference Manual with Protocol Interworking*.

- DDR SDRAM memory controller
  - Programmable timing supporting DDR2 SDRAM
  - Integrated SDRAM clock generation
  - 16-bit data interface, up to 266-MHz data rate
  - 14 address lines
  - The following SDRAM configurations are supported:
    - Up to two physical banks (chip selects), 256-Mbyte per chip select for 16 bit data interface.
    - 64-Mbit to 2-Gbit devices with x8/x16 data ports (no direct x4 support)
    - One 16-bit device or two 8-bit devices on a 16-bit bus,
  - Support for up to 16 simultaneous open pages for DDR2
  - One clock pair to support up to 4 DRAM devices
  - Supports auto refresh
  - On-the-fly power management using CKE
- Enhanced local bus controller (eLBC)
  - Multiplexed 26-bit address and 8-/16-bit data operating at up to 66 MHz
  - Eight chip selects supporting eight external slaves
    - Four chip selects dedicated
    - Four chip selects offered as multiplexed option
  - Supports boot from parallel NOR Flash and parallel NAND Flash
  - Supports programmable clock ratio dividers
  - Up to eight-beat burst transfers
  - 16- and 8-bit ports, separate $\overline{\text{LWE}}$ for each 8 bit
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Variable memory block sizes for FCM, GPCM, and UPM mode
  - Default boot ROM chip select with configurable bus width (8 or 16)
  - Provides two Write Enable signals to allow single byte write access to external 16-bit eLBC slave devices
- Integrated programmable interrupt controller (IPIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for external and internal discrete interrupt sources

The following table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 1.8 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 16 bits	0.141	—	W	—
Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 26 bits	—	0.150	W	1
QUICC Engine block and other I/Os	TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, SPI, Timer output, FlexCAN, eSDHC				

Note:
1. Typical I/O power is based on a nominal voltage of V_{DD} = 3.3V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8306.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of OV_{DD}; fall time refers to transitions from 90% to 10% of OV_{DD}.

4.1 DC Electrical Characteristics

The following table provides the clock input (SYS_CLK_IN) DC specifications for the MPC8306. These specifications are also applicable for QE_CLK_IN.

Table 7. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0.5 V ≤ V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8306 is SYS_CLK_IN. The following table provides the clock input (SYS_CLK_IN) AC timing specifications for the MPC8306. These specifications are also applicable for QE_CLK_IN.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1
SYS_CLK_IN cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	1.1	—	2.8	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8306. The following table provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of PORESET with stable clock applied to SYS_CLK_IN	32	—	$t_{SYS\_CLK\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$	4	—	$t_{SYS\_CLK\_IN}$	1, 2
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
2. POR configuration signals consist of CFG_RESET_SOURCE[0:3].

Table 16. DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
$\overline{MCS}$ output hold with respect to MCK 266 MHz	t_{DDKHCX}	 2.5	 —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MDM output setup with respect to MDQS 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.9	 —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100	 —	ps	5
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjusts in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. t_{DDKHMP} follows the symbol conventions described in note 1.

7 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8306.

7.1 Local Bus DC Electrical Characteristics

The following table provides the DC electrical characteristics for the local bus interface.

Table 17. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	μA

7.2 Local Bus AC Electrical Specifications

The following table describes the general timing parameters of the local bus interface of the MPC8306.

Table 18. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Table 19. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(max) to V_{IH}(min)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(min) to V_{IL}(max)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

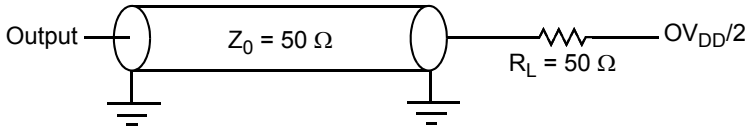

Figure 11. AC Test Load

The following figure shows the MII transmit AC timing diagram.

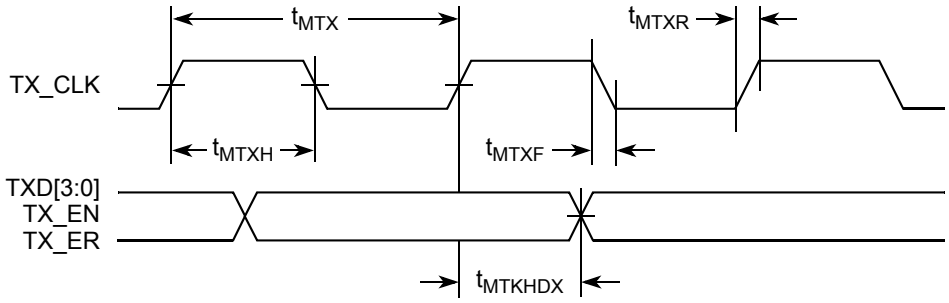

Figure 12. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

Table 21. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(max) to V_{IH}(min)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(min) to V_{IL}(max)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the RMII transmit AC timing diagram.

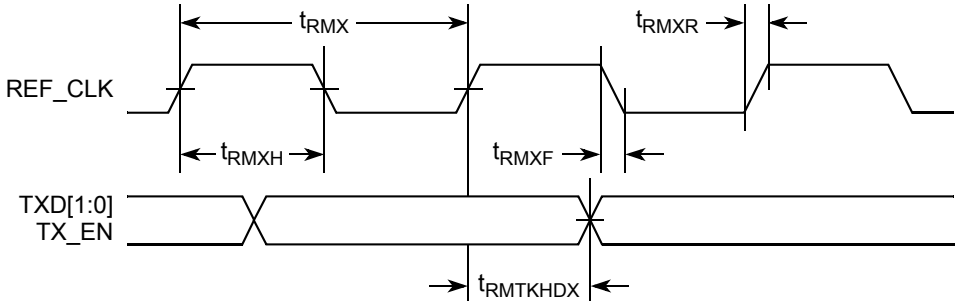

Figure 15. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the RMII receive AC timing diagram.

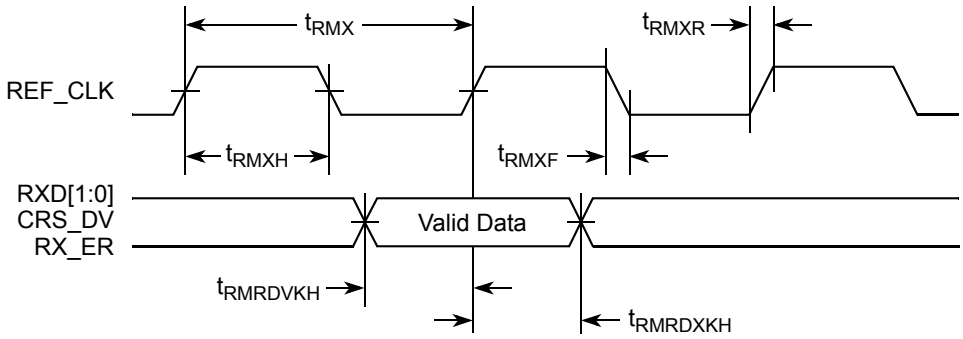

Figure 16. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

The following table provides the MII management AC timing specifications.

Table 25. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

15 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8306.

15.1 I²C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I²C interface of the MPC8306.

Table 40. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8306 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

15.2 I²C AC Electrical Specifications

The following table provides the AC timing parameters for the I²C interface of the MPC8306.

Table 41. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 40).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	300	0.9[3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_B$[4]	300	ns

Table 41. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 40).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8306 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

The following figure provides the AC test load for the I²C.

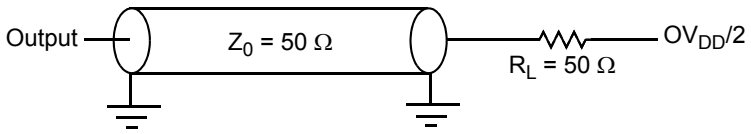

Figure 29. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

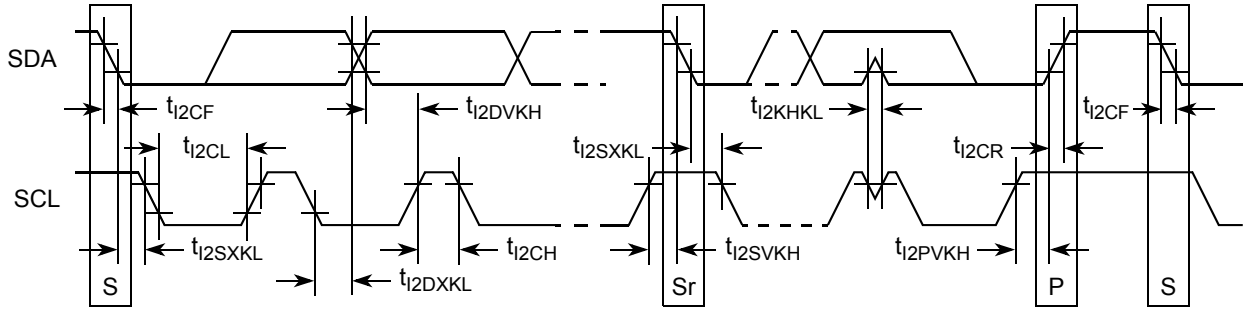

Figure 30. I²C Bus AC Timing Diagram

17 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8306.

17.1 GPIO DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306 GPIO.

Table 44. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

17.2 GPIO AC Timing Specifications

The following table provides the GPIO input and output AC timing specifications.

Table 45. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

The following figure provides the AC test load for the GPIO.

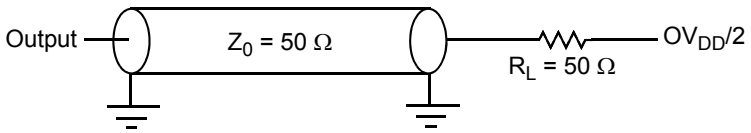

Figure 32. GPIO AC Test Load

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[17]	B14	O	OV_{DD}	—
LA[18]	A14	O	OV_{DD}	—
LA[19]	A15	O	OV_{DD}	—
LA[20]	A16	O	OV_{DD}	—
LA[21]	B16	O	OV_{DD}	—
LA[22]	A17	O	OV_{DD}	—
LA[23]	B17	O	OV_{DD}	—
LA[24]	A18	O	OV_{DD}	—
LA[25]	B19	O	OV_{DD}	—
LCS_B[0]	A19	O	OV_{DD}	3
LCS_B[1]	B20	O	OV_{DD}	3
LCS_B[2]	A20	O	OV_{DD}	3
LCS_B[3]	A21	O	OV_{DD}	3
LCLK[0]	D13	O	OV_{DD}	—
LGPL[0]/LFCLE	B22	O	OV_{DD}	—
LGPL[1]/LFALE	D16	O	OV_{DD}	—
LGPL[2]/LOE_B/LFRE_B	D19	O	OV_{DD}	—
LGPL[3]/LFWP_B	D17	O	OV_{DD}	—
LGPL[4]/LGTA_B/LUPWAIT/LFRB_B	E18	IO	OV_{DD}	—
LGPL[5]	E19	O	OV_{DD}	—
LWE_B[0]/LFWE_B[0]/LBS_B[0]	D15	O	OV_{DD}	—
LWE_B[1]/LBS_B[1]	D14	O	OV_{DD}	—
LBCTL	A22	O	OV_{DD}	—
LALE	B23	O	OV_{DD}	—
JTAG				
TCK	A3	I	OV_{DD}	—
TDI	B5	I	OV_{DD}	3
TDO	D7	O	OV_{DD}	—
TMS	A4	I	OV_{DD}	3
TRST_B	D8	I	OV_{DD}	3
Test Interface				
TEST_MODE	A5	I	OV_{DD}	—
System Control Signals				
HRESET_B	U20	IO	OV_{DD}	1
PORESET_B	V20	I	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USBDR_TXDRXD[7]/GPIO[37]/QE_BRG[11]	Y5	IO	OV_{DD}	—
DUART				
UART1_SOUT[1]/LSRCID4/LCS_B[4]	C23	O	OV_{DD}	—
UART1_SIN[1]/LDVAL/LCS_B[5]	F19	IO	OV_{DD}	—
UART1_SOUT[2]/UART1_RTS_B1/LCS_B[6]	D23	O	OV_{DD}	—
UART1_SIN[2]/UART1_CTS_B[1]/LCS_B[7]	D22	IO	OV_{DD}	—
Interrupts				
IRQ_B0_MCP_IN_B/CE_PI_0	E20	IO	OV_{DD}	—
IRQ_B1/MCP_OUT_B	E23	IO	OV_{DD}	—
IRQ_B2/CKSTOP_OUT_B	E22	IO	OV_{DD}	—
IRQ_B3/CKSTOP_IN_B	F20	I	OV_{DD}	—
I2C / SPI				
IIC_SDA1	G20	IO	OV_{DD}	2
IIC_SCL1	J20	IO	OV_{DD}	2
LCLK1/IIC_SCL2/CKSTOP_IN_B	H20	IO	OV_{DD}	2
SPISEL_BOOT/IIC_SDA2/CKSTOP_OUT_B	F23	O	OV_{DD}	2
SPIMOSI/LSRCID[2]	G22	IO	OV_{DD}	—
SPIMISO/LSRCID[3]	K20	IO	OV_{DD}	—
SPICLK/LSRCID[0]	G23	IO	OV_{DD}	—
SPISEL/LSRCID[1]	H22	I	OV_{DD}	—
FEC Management				
FEC_MDC	H23	O	OV_{DD}	—
FEC_MDIO	L20	IO	OV_{DD}	—
FEC1/GTM/GPIO				
FEC1_COL/GTM1_TIN[1]/GPIO[16]	AB20	IO	OV_{DD}	—
FEC1_CRS/GTM1_TGATE1_B/GPIO[17]	AC21	IO	OV_{DD}	—
FEC1_RX_CLK/GPIO[18]	Y17	IO	OV_{DD}	—
FEC1_RX_DV/GTM1_TIN[2]/GPIO[19]	Y18	IO	OV_{DD}	—
FEC1_RX_ER/GTM1_TGATE[2]_B/GPIO[20]	AB19	IO	OV_{DD}	—
FEC1_RXD0/GPIO[21]	AC20	IO	OV_{DD}	—
FEC1_RXD1/GTM1_TIN[3]/GPIO[22]	AC19	IO	OV_{DD}	—
FEC1_RXD2/GTM1_TGATE[3]_B/GPIO[23]	AC18	IO	OV_{DD}	—
FEC1_RXD3/GPIO[24]	AB17	IO	OV_{DD}	—
FEC1_TX_CLK/GTM1_TIN4/GPIO[25]	Y15	IO	OV_{DD}	—
FEC1_TX_EN/GTM1_TGATE[4]_B/GPIO[26]	Y16	IO	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FEC1_TX_ER/GTM1_TOUT[4]_B/GPIO[27]	AC17	IO	OV_{DD}	—
FEC1_TXD0/GTM1_TOUT[1]_B/GPIO[28]	AB16	IO	OV_{DD}	—
FEC1_TXD1/GTM1_TOUT[2]_B/GPIO[29]	AC16	IO	OV_{DD}	—
FEC1_TXD2/GTM1_TOUT[3]_B/GPIO[30]	AC15	IO	OV_{DD}	—
FEC1_TXD3/GPIO[31]	AB14	IO	OV_{DD}	—
FEC2/GPIO				
FEC2_COL/GPIO[32]	AC14	IO	OV_{DD}	—
FEC2_CRS/GPIO[33]	AB13	IO	OV_{DD}	—
FEC2_RX_CLK/GPIO[34]	Y14	IO	OV_{DD}	—
FEC2_RX_DV/GPIO[35]	AC13	IO	OV_{DD}	—
FEC2_RX_ER/GPIO[36]	Y13	IO	OV_{DD}	—
FEC2_RXD0/GPIO[37]	AC12	IO	OV_{DD}	—
FEC2_RXD1/GPIO[38]	AB11	IO	OV_{DD}	—
FEC2_RXD2/GPIO[39]	AC11	IO	OV_{DD}	—
FEC2_RXD3/GPIO[40]	AB10	IO	OV_{DD}	—
FEC2_TX_CLK/GPIO[41]	Y12	IO	OV_{DD}	—
FEC2_TX_EN/GPIO[42]	AC10	IO	OV_{DD}	—
FEC2_TX_ER/GPIO[43]	AC9	IO	OV_{DD}	—
FEC2_TXD0/GPIO[44]	AC8	IO	OV_{DD}	—
FEC2_TXD1/GPIO[45]	Y11	IO	OV_{DD}	—
FEC2_TXD2/GPIO[46]	AC7	IO	OV_{DD}	—
FEC2_TXD3/GPIO[47]	Y10	IO	OV_{DD}	—
FEC3/GPIO				
FEC3_COL/GPIO[48]	J23	IO	OV_{DD}	—
FEC3_CRS/GPIO[49]	K23	IO	OV_{DD}	—
FEC3_RX_CLK/GPIO[50]	M20	IO	OV_{DD}	—
FEC3_RX_DV/GPIO[51]	K22	IO	OV_{DD}	—
FEC3_RX_ER/GPIO[52]	L22	IO	OV_{DD}	—
FEC3_RXD0/GPIO[53]	L23	IO	OV_{DD}	—
FEC3_RXD1GPIO[54]	M23	IO	OV_{DD}	—
FEC3_RXD2/FEC_TMR_TRIG1/GPIO[55]	N22	IO	OV_{DD}	—
FEC3_RXD3/FEC_TMR_TRIG2/GPIO[56]	N23	IO	OV_{DD}	—
FEC3_TX_CLK/FEC_TMR_CLK/GPIO[57]	N20	IO	OV_{DD}	—
FEC3_TX_EN/FEC_TMR_GCLK/GPIO[58]	P20	IO	OV_{DD}	—
FEC3_TX_ER/FEC_TMR_PP1/GPIO[59]	P22	IO	OV_{DD}	—

23 Thermal

This section describes the thermal specifications of the MPC8306.

23.1 Thermal Characteristics

The following table provides the package thermal characteristics for the 369, 19 × 19 mm MAPBGA of the MPC8306.

Table 61. Package Thermal Characteristics for MAPBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	39	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	24	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	32	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	21	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	14	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

23.1.1 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

23.1.2 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where:

T_J = junction temperature (°C)

lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

23.2.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface.

From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance using the following equation:

$$T_J = T_C + (R_{\theta JC} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8306.

24.1 System Clocking

The MPC8306 includes three PLLs.

- The system PLL (AV_{DD2}) generates the system clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the system and SYS_CLK_IN is selected using the system PLL ratio configuration bits as described in Section 22.2, “System PLL Configuration.”
- The e300 core PLL (AV_{DD3}) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 22.3, “Core PLL Configuration.”
- The QUICC Engine PLL (AV_{DD1}) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 44, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

The following figure shows the PLL power supply filter circuit.

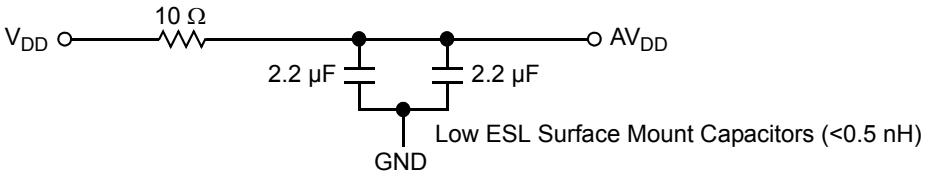

Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8306 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8306 system, and MPC8306 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8306. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias

26 Document Revision History

The following table provides a revision history for this document.

Table 65. Document Revision History

Rev. No.	Date	Substantive Change(s)
3	12/2014	• In Table 20 an Table 21, V_{IL}(min) is replaced with V_{IL}(max) and V_{IH}(max) is replaced with V_{IL}(min) • Removed following signals from Table 52: – FEC1_TMR_TX_ESFD – FEC1_TMR_RX_ESFD – FEC2_TMR_TX_ESFD – FEC2_TMR_RX_ESFD • Updated following signal names in Table 52: – LGPL[0] to LGPL[0]/LFCLE – LGPL[1] to LGPL[1]/LFALE – LGPL[2] to LGPL[2]/LOE_B/LFRE_B – LGPL[3] to LGPL[3]/LFWP_B – LGPL[4] to LGPL[4]/LGTA_B/LUPWAIT/LFRB_B – LWE_B[0] to LWE_B[0]/LFWE_B[0]/LBS_B[0] – LWE_B[1] to LWE_B[1]/LBS_B[1]
2	09/2011	• Added Power numbers for core frequency of 333 MHz in Table 5. • Added new PLL configurations as per new core frequency in Table 60. • Added AF to indicate 333 MHz in Table 63.
1	06/2011	• Updated QE frequency in Table 5. • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 54. • Updated CEMF and CEDF as per new QE frequency in Table 60. • In Part Nomenclature field for QUICC Engine frequency, C now denotes 233 MHz. Updated Table 63. • Added SPISEL_BOOT in MPC8306 Pin out Listing Table 52. • Corrected SPISEL Pin Type in Table 52.
0	03/2011	Initial Release