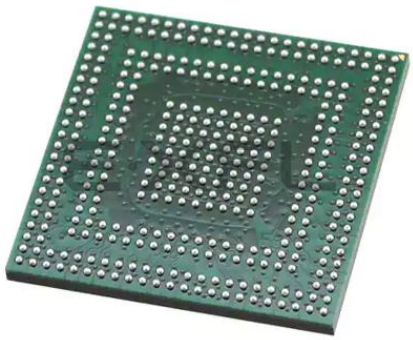

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8306vmaddca

1 Overview

The MPC8306 incorporates the e300c3 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8306 also includes two DMA engines and a 16-bit DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8306. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8306 is shown in the following figure.

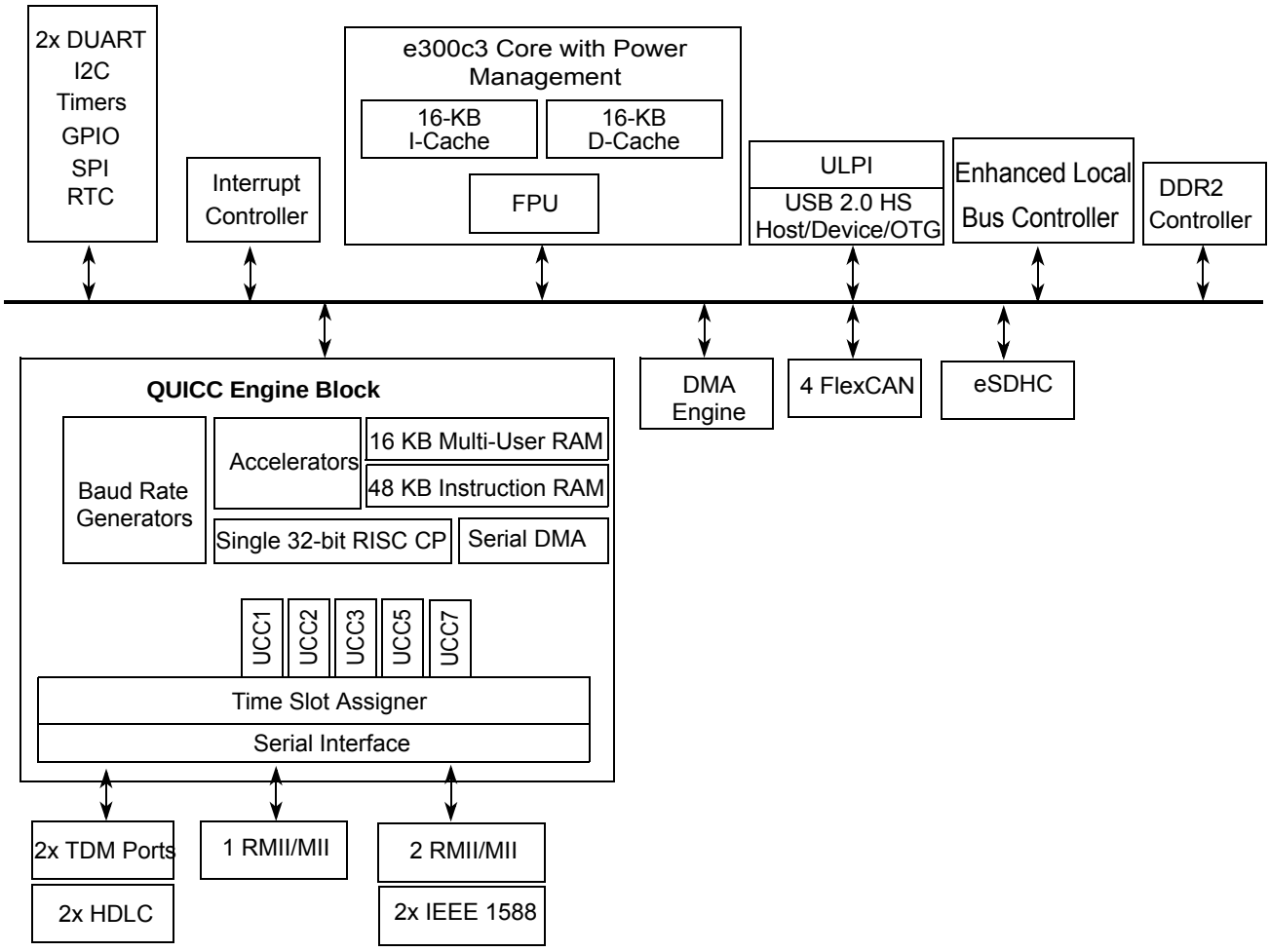


Figure 1. MPC8306 Block Diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, IEEE-1588, HDLC and TDM.

  - Programmable highest priority request
  - Six groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Unique vector number for each interrupt source
- Enhanced secure digital host controller (eSDHC)
  - Compatible with the *SD Host Controller Standard Specification Version 2.0* with test event register support
  - Compatible with the *MMC System Specification Version 4.2*
  - Compatible with the *SD Memory Card Specification Version 2.0* and supports the high capacity SD memory card
  - Compatible with the *SD Input/Output (SDIO) Card Specification, Version 2.0*
  - Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, and RS-MMC cards
  - Card bus clock frequency up to 33.33 MHz.
  - Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    - Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  - Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
  - Up to 64 flexible message buffers of zero to eight bytes data length
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - Selectable backwards compatibility with previous FlexCAN module version
  - Programmable loop-back mode supporting self-test operation
  - Global network time, synchronized by a specific message
  - Independent of the transmission medium (an external transceiver is required)
  - Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer

- DMA Engine
  - Support for the DMA engine with the following features:
    - Sixteen DMA channels
    - All data movement via dual-address transfers: read from source, write to destination
    - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - Explicit software initiation
      - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - Support for fixed-priority and round-robin channel arbitration
    - Channel completion reported via optional interrupt requests
  - Support for scatter/gather DMA processing
- DUART
  - Two 2-wire interfaces (RxD, TxD)
    - The same can be configured as one 4-wire interface (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI)
  - Master or slave support
- Power managemnt controller (PMC)
  - Supports core doze/nap/sleep/ power management
  - Exits low power state and returns to full-on mode when
    - The core internal time base unit invokes a request to exit low power state
    - The power management controller detects that the system is not idle and there are outstanding transactions on the internal bus or an external interrupt.
- Parallel I/O
  - General-purpose I/O (GPIO)
    - 56 parallel I/O pins multiplexed on various chip interfaces
    - Interrupt capability
- System timers
  - Periodic interrupt timer
  - Software watchdog timer
  - Eight general-purpose timers
- Real time clock (RTC) module
  - Maintains a one-second count, unique over a period of thousands of years
  - Two possible clock sources:
    - External RTC clock (RTC_PIT_CLK)
    - CSB bus clock
- IEEE Std. 1149.1™ compliant JTAG boundary scan

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8306. The MPC8306 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1} AV_{DD2} AV_{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.98	V	—
Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN, USB and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	2
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

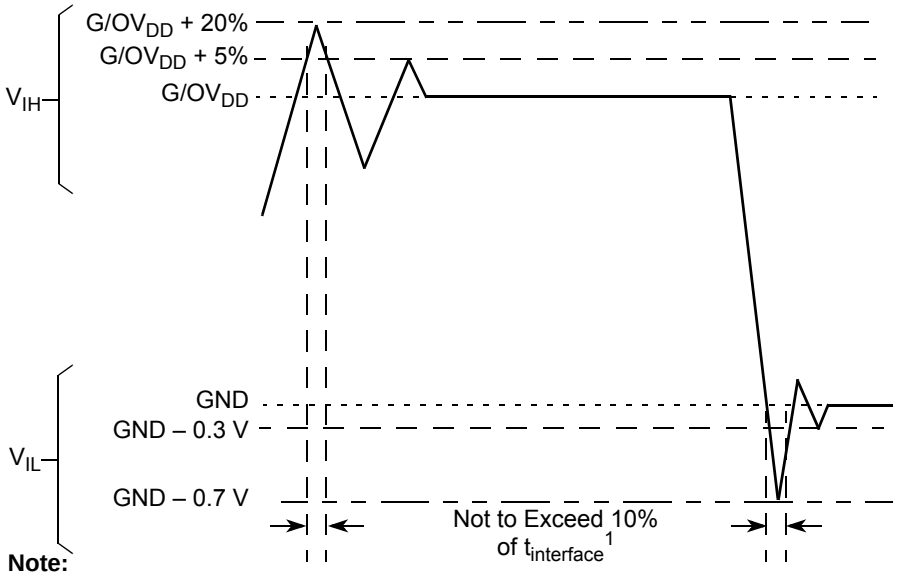
The following table provides the recommended operating conditions for the MPC8306. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV_{DD1} AV_{DD2} AV_{DD3}	1.0 V ± 50 mV	V	1
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V ± 100 mV	V	1
Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN, USB and JTAG I/O voltage	OV_{DD}	3.3 V ± 300 mV	V	1, 3
Junction temperature	T_A/T_J	0 to 105	°C	2

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A(Ambient Temperature); maximum temperature is specified with T_J(Junction Temperature).
3. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8306



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}

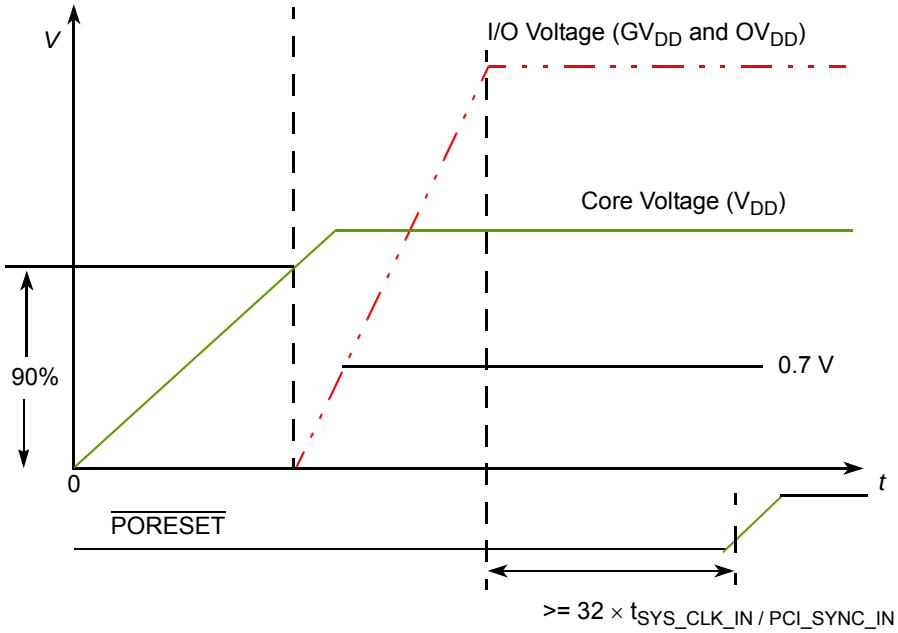


Figure 3. MPC8306 Power-Up Sequencing Example

3 Power Characteristics

The typical power dissipation for this family of MPC8306 devices is shown in the following table.

Table 5. MPC8306 Power Dissipation

Core Frequency (MHz)	QUICC Engine Frequency (MHz)	CSB Frequency (MHz)	Typical	Maximum	Unit	Note
133	133	133	0.272	0.618	W	1, 2, 3
200	233	133	0.291	0.631	W	1, 2, 3
266	233	133	0.451	0.925	W	1, 2, 3
333	233	133	0.471	0.950	W	1, 2, 3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}), but it does include V_{DD} and AV_{DD} power. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, WC process, a junction T_J = 105°C, and a smoke test code.

The following figure provides the AC test load for the local bus.

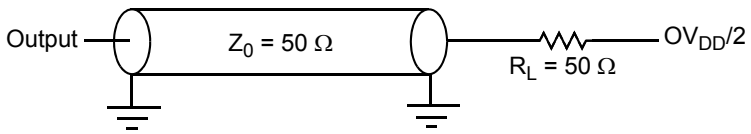


Figure 7. Local Bus AC Test Load

The following figures show the local bus signals. These figures has been given indicate timing parameters only and do not reflect actual functional operation of interface.

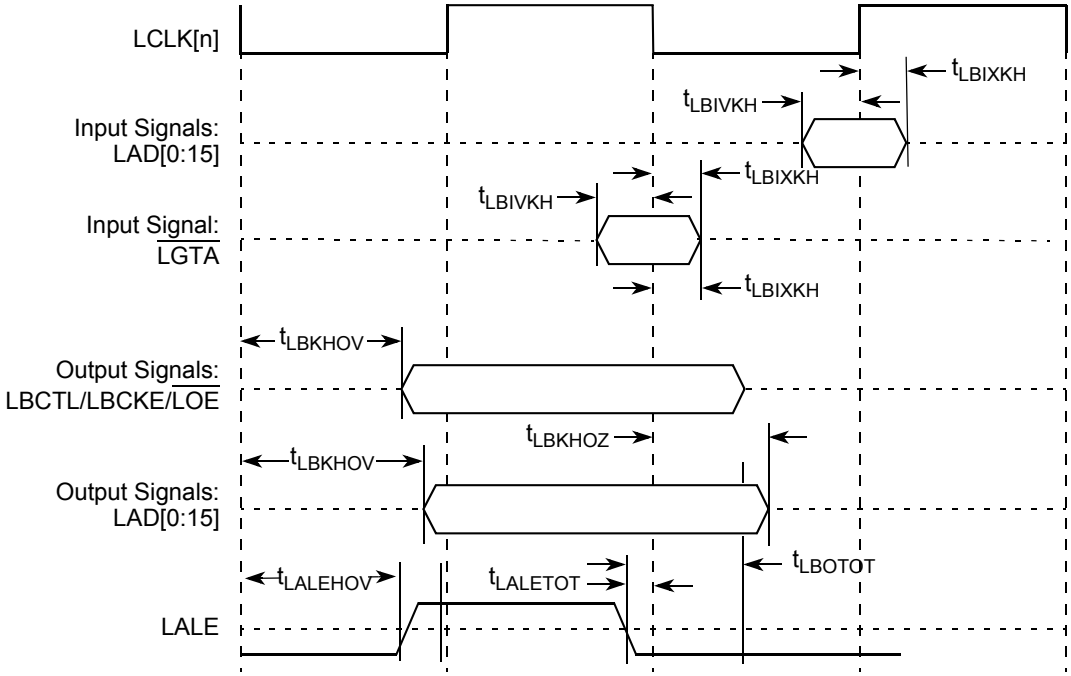


Figure 8. Local Bus Signals

Table 25. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	8.5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII management AC timing diagram.

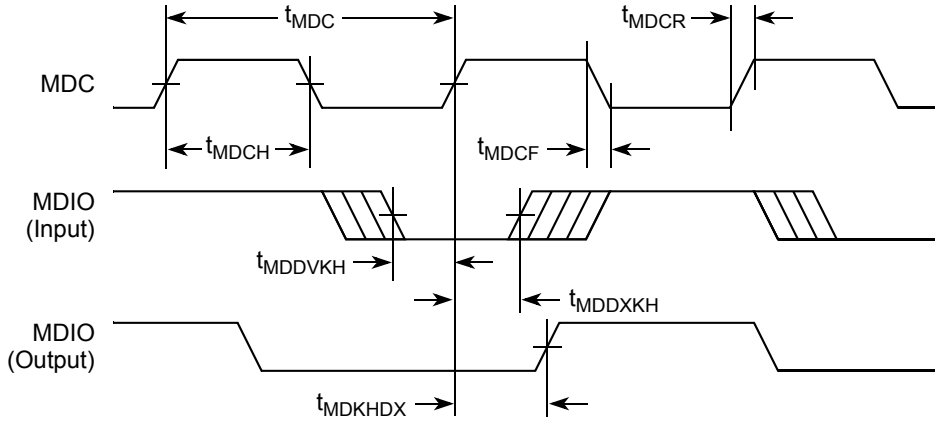


Figure 17. MII Management Interface Timing Diagram

8.3.3 IEEE 1588 DC Specifications

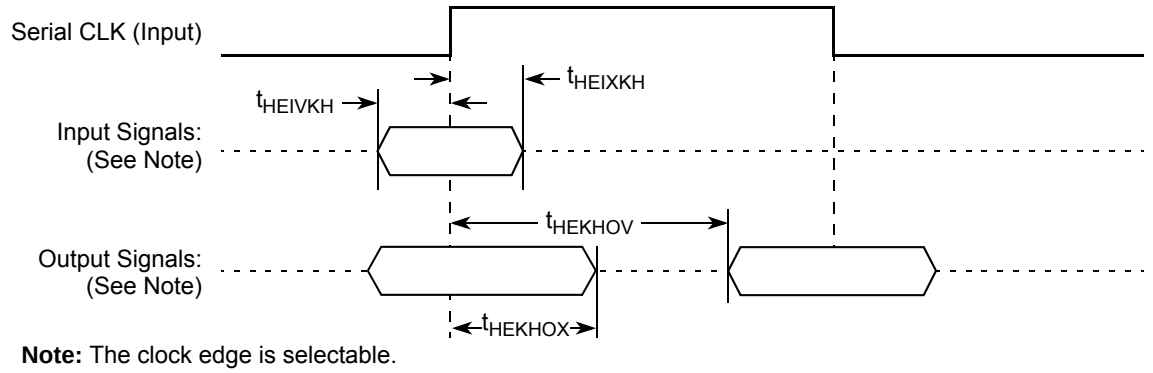
The IEEE 1588 DC timing specifications are given in the following table.

Table 26. IEEE 1588 DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	unit
Output high voltage	V_{OH}	I_{OH} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2mA	—	0.4	V

Figure 23 and Figure 24 represent the AC timing from Table 31. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

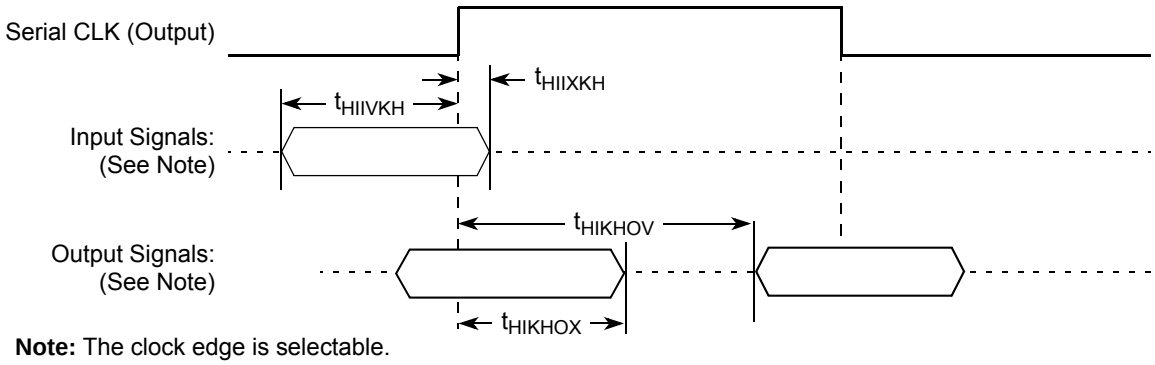
The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 23. AC Timing (External Clock) Diagram

The following figure shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 24. AC Timing (Internal Clock) Diagram

Table 41. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 40).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8306 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

The following figure provides the AC test load for the I²C.

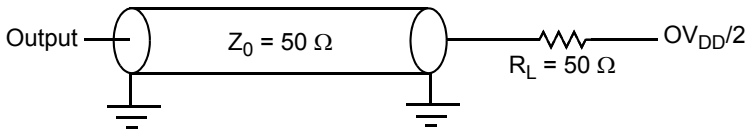


Figure 29. I²C AC Test Load

The following figure shows the AC timing diagram for the I²C bus.

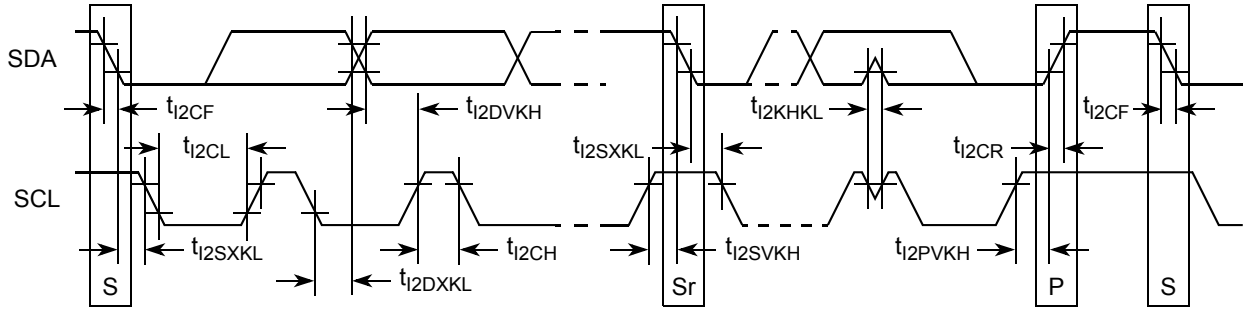


Figure 30. I²C Bus AC Timing Diagram

The following figure provides the boundary-scan timing diagram.

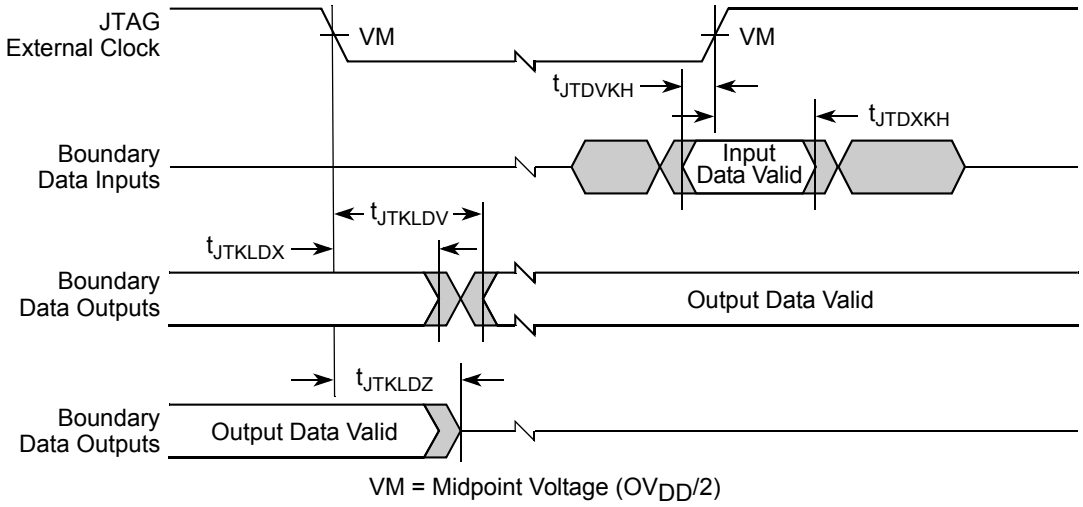


Figure 39. Boundary-Scan Timing Diagram

The following figure provides the test access port timing diagram.

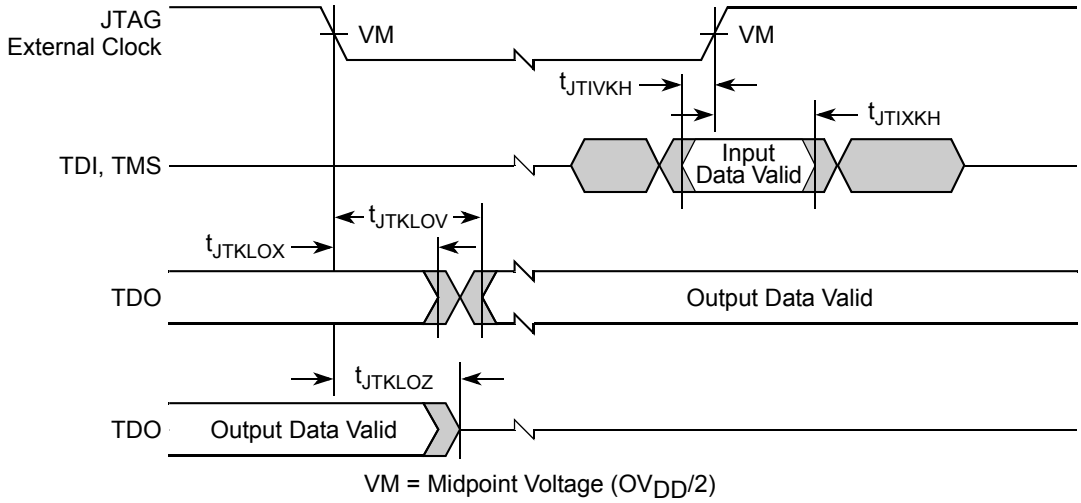


Figure 40. Test Access Port Timing Diagram

21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8306 is available in a thermally enhanced MAPBGA (mold array process-ball grid array); see Section 21.1, “Package Parameters for the MPC8306,” and Section 21.2, “Mechanical Dimensions of the MPC8306 MAPBGA,” for information on the MAPBGA.

21.1 Package Parameters for the MPC8306

The package parameters are as provided in the following list.

Package outline	19 mm × 19 mm
Package Type	MAPBGA
Interconnects	369
Pitch	0.80 mm
Module height (typical)	1.48 mm; Min = 1.31mm and Max 1.61mm
Solder Balls	96 Sn / 3.5 Ag / 0.5 Cu (VM package)
Ball diameter (typical)	0.40 mm

21.2 Mechanical Dimensions of the MPC8306 MAPBGA

The following figure shows the mechanical dimensions and bottom surface nomenclature of the MPC8306, 369-MAPBGA package.

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA[17]	B14	O	OV_{DD}	—
LA[18]	A14	O	OV_{DD}	—
LA[19]	A15	O	OV_{DD}	—
LA[20]	A16	O	OV_{DD}	—
LA[21]	B16	O	OV_{DD}	—
LA[22]	A17	O	OV_{DD}	—
LA[23]	B17	O	OV_{DD}	—
LA[24]	A18	O	OV_{DD}	—
LA[25]	B19	O	OV_{DD}	—
LCS_B[0]	A19	O	OV_{DD}	3
LCS_B[1]	B20	O	OV_{DD}	3
LCS_B[2]	A20	O	OV_{DD}	3
LCS_B[3]	A21	O	OV_{DD}	3
LCLK[0]	D13	O	OV_{DD}	—
LGPL[0]/LFCLE	B22	O	OV_{DD}	—
LGPL[1]/LFALE	D16	O	OV_{DD}	—
LGPL[2]/LOE_B/LFRE_B	D19	O	OV_{DD}	—
LGPL[3]/LFWP_B	D17	O	OV_{DD}	—
LGPL[4]/LGTA_B/LUPWAIT/LFRB_B	E18	IO	OV_{DD}	—
LGPL[5]	E19	O	OV_{DD}	—
LWE_B[0]/LFWE_B[0]/LBS_B[0]	D15	O	OV_{DD}	—
LWE_B[1]/LBS_B[1]	D14	O	OV_{DD}	—
LBCTL	A22	O	OV_{DD}	—
LALE	B23	O	OV_{DD}	—
JTAG				
TCK	A3	I	OV_{DD}	—
TDI	B5	I	OV_{DD}	3
TDO	D7	O	OV_{DD}	—
TMS	A4	I	OV_{DD}	3
TRST_B	D8	I	OV_{DD}	3
Test Interface				
TEST_MODE	A5	I	OV_{DD}	—
System Control Signals				
HRESET_B	U20	IO	OV_{DD}	1
PORESET_B	V20	I	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USBDR_TXDRXD[7]/GPIO[37]/QE_BRG[11]	Y5	IO	OV_{DD}	—
DUART				
UART1_SOUT[1]/LSRCID4/LCS_B[4]	C23	O	OV_{DD}	—
UART1_SIN[1]/LDVAL/LCS_B[5]	F19	IO	OV_{DD}	—
UART1_SOUT[2]/UART1_RTS_B1/LCS_B[6]	D23	O	OV_{DD}	—
UART1_SIN[2]/UART1_CTS_B[1]/LCS_B[7]	D22	IO	OV_{DD}	—
Interrupts				
IRQ_B0_MCP_IN_B/CE_PI_0	E20	IO	OV_{DD}	—
IRQ_B1/MCP_OUT_B	E23	IO	OV_{DD}	—
IRQ_B2/CKSTOP_OUT_B	E22	IO	OV_{DD}	—
IRQ_B3/CKSTOP_IN_B	F20	I	OV_{DD}	—
I2C / SPI				
IIC_SDA1	G20	IO	OV_{DD}	2
IIC_SCL1	J20	IO	OV_{DD}	2
LCLK1/IIC_SCL2/CKSTOP_IN_B	H20	IO	OV_{DD}	2
SPISEL_BOOT/IIC_SDA2/CKSTOP_OUT_B	F23	O	OV_{DD}	2
SPIMOSI/LSRCID[2]	G22	IO	OV_{DD}	—
SPIMISO/LSRCID[3]	K20	IO	OV_{DD}	—
SPICLK/LSRCID[0]	G23	IO	OV_{DD}	—
SPISEL/LSRCID[1]	H22	I	OV_{DD}	—
FEC Management				
FEC_MDC	H23	O	OV_{DD}	—
FEC_MDIO	L20	IO	OV_{DD}	—
FEC1/GTM/GPIO				
FEC1_COL/GTM1_TIN[1]/GPIO[16]	AB20	IO	OV_{DD}	—
FEC1_CRS/GTM1_TGATE1_B/GPIO[17]	AC21	IO	OV_{DD}	—
FEC1_RX_CLK/GPIO[18]	Y17	IO	OV_{DD}	—
FEC1_RX_DV/GTM1_TIN[2]/GPIO[19]	Y18	IO	OV_{DD}	—
FEC1_RX_ER/GTM1_TGATE[2]_B/GPIO[20]	AB19	IO	OV_{DD}	—
FEC1_RXD0/GPIO[21]	AC20	IO	OV_{DD}	—
FEC1_RXD1/GTM1_TIN[3]/GPIO[22]	AC19	IO	OV_{DD}	—
FEC1_RXD2/GTM1_TGATE[3]_B/GPIO[23]	AC18	IO	OV_{DD}	—
FEC1_RXD3/GPIO[24]	AB17	IO	OV_{DD}	—
FEC1_TX_CLK/GTM1_TIN4/GPIO[25]	Y15	IO	OV_{DD}	—
FEC1_TX_EN/GTM1_TGATE[4]_B/GPIO[26]	Y16	IO	OV_{DD}	—

Table 52. MPC8306 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FEC3_TXD0/FEC_TMR_PP2/GPIO[60]	R20	IO	OV_{DD}	—
FEC3_TXD1/FEC_TMR_PP3/GPIO[61]	T22	IO	OV_{DD}	—
FEC3_TXD2/FEC_TMR_ALARM1/GPIO[62]	T23	IO	OV_{DD}	—
FEC3_TXD3/FEC_TMR_ALARM2/GPIO[63]	T20	IO	OV_{DD}	—
HDLC/GPIO/TDM				
HDLC1_RXCLK/TDM1_RCK/GPIO[1]	U23	IO	OV_{DD}	—
HDLC1_RXD/TDM1_RD/GPIO[3]	U22	IO	OV_{DD}	—
HDLC1_TXCLK/GPIO[0]/TDM1_TCK/ QE_BRG[5]	AC22	IO	OV_{DD}	—
HDLC1_TXD/GPIO[2]/TDM1_TD/ CFG_RESET_SOURCE[0]	W18	IO	OV_{DD}	—
HDLC1_CD_B/GPIO[4]/TDM1_TFS	W19	IO	OV_{DD}	—
HDLC1_CTS_B/GPIO[5]/TDM1_RFS	Y20	IO	OV_{DD}	—
HDLC1_RTS_B/GPIO[6]/TDM1_STROBE_B/ CFG_RESET_SOURCE[1]	AB22	IO	OV_{DD}	—
HDLC2_TXCLK/GPIO[16]/TDM2_TCK/ QE_BRG[7]	AB23	IO	OV_{DD}	—
HDLC2_RXCLK/GPIO[17]/TDM2_RCK/ QE_BRG[8]	AA23	IO	OV_{DD}	—
HDLC2_TXD/GPIO[18]/TDM2_TD/ CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	—
HDLC2_RXD/GPIO[19]/TDM2_RD	Y23	IO	OV_{DD}	—
HDLC2_CD_B/GPIO[20]/TDM2_TFS	Y22	IO	OV_{DD}	—
HDLC2_CTS_B/GPIO[21]/TDM2_RFS	W23	IO	OV_{DD}	—
HDLC2_RTS_B/GPIO[22]/TDM2_STROBE_B/ CFG_RESET_SOURCE[3]	W22	IO	OV_{DD}	—
Power				
AV_{DD1}	L16	—	—	—
AV_{DD2}	M16	—	—	—
AV_{DD3}	N8	—	—	—
GV_{DD}	G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5	—	—	—
OV_{DD}	E7,E8,E9,E10,E11,E12, E13,E14, E15, E16,E17,G19,H19,J19,K 19,L19,M19, N19,P19,R19,T19,U19, W7,W8,W9, W10,W11, W12,W13, W14,W15, W16, W17	—	—	—

Table 55. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

Table 56. CSB Frequency Options

SPMF	csb_clk : sys_clk_in Ratio	SYS_CLK_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

22.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 57. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

23.1.3 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \qquad \text{Eqn. 2}$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.1.4 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \text{Eqn. 3}$$

where:

T_J = junction temperature (°C)

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 44, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

The following figure shows the PLL power supply filter circuit.

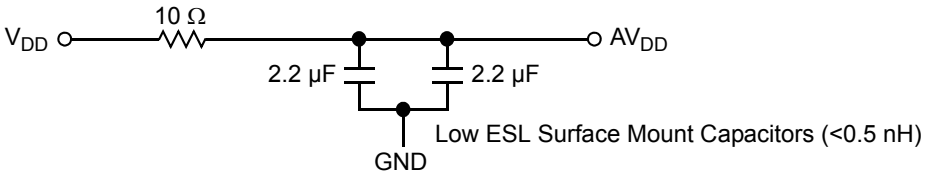


Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8306 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8306 system, and MPC8306 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8306. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias

Table 63. Part Numbering Nomenclature

MPC	*nnnn*	*C*	*VM*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR2 Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8306	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free	AB = 133MHz AC = 200 MHz AD = 266 MHz AF = 333 MHz	D = 266 MHz F = 333 MHz	C = 233 MHz	Contact local Freescale sales office

Notes:
1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 21, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

25.2 Part Marking

Parts are marked as in the example shown in the following figure.

MAPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 46. Freescale Part Marking for MAPBGA Devices

The following table shows the SVR Settings.

Table 64. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)
MPC8306	MAPBGA	0x8110_0210	0x8110_0211
Note: PVR = 0x8085_0020			

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