Microchip Technology - ATSAMHA1E14A-MBT-BVAO Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus SBC, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	0V ~ 3.8V
Data Converters	A/D 6x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TC)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamha1e14a-mbt-bvao

	SAMHA0/1
Event System channels	12
SW Debug Interface	Yes
Watchdog Timer (WDT)	Yes

14. Peripherals Configuration Summary

Table 14-1. Peripherals Configuration Summary

Periph. Name	Base Address	IRQ Line	AHB Clock Index	AHB Clock Enabled at Reset	APB Clock Index	APB Clock Enabled at Reset	Generic Clock Index	PAC Index	PAC Prot. at Reset	Events User	Events Generator	DMA Index	Sleep Walking
AHB-APB Bridge A	0x40000000		0	Y									
PAC0	0x40000000				0	Y							
PM	0x40000400	0			1	Y		1	N				Y
SYSCTRL	0x40000800	1			2	Y	0: DFLL48M reference 1: FDPLL96M clk source 2: FDPLL96M 32kHz	2	N				Y
GCLK	0x40000C00				3	Y		3	N				Y
WDT	0x40001000	2			4	Y	3	4	N				
RTC	0x40001400	3			5	Y	4	5	N		1: CMP0/ALARM0 2: CMP1 3: OVF 4-11: PER0-7		Y
EIC	0x40001800	NMI, 4			6	Y	5	6	N		12-27: EXTINT0-15		Y
AHB-APB Bridge B	0x41000000		1	Y									
PAC1	0x41000000				0	Y							
DSU	0x41002000		3	Y	1	Y		1	Y				
NVMCTRL	0x41004000	5	4	Y	2	Y		2	N				
PORT	0x41004400				3	Y		3	N				
DMAC	0x41004800	6	5	Y	4	Y		4	N	0-3: CH0-3	30-33: CH0-3		
MTB	0x41006000							6	N				
AHB-APB Bridge C	0x42000000		2	Y									
PAC2	0x42000000				0	N							
EVSYS	0x42000400	8			1	N	7-18: one per CHANNEL	1	N				Y
SERCOM0	0x42000800	9			2	N	20: CORE 19: SLOW	2	N			1: RX 2: TX	Y
SERCOM1	0x42000C00	10			3	N	21: CORE 19: SLOW	3	N			3: RX 4: TX	Y
SERCOM2	0x42001000	11			4	N	22: CORE 19: SLOW	4	N			5: RX 6: TX	Y
SERCOM3	0x42001400	12			5	N	23: CORE 19: SLOW	5	N			7: RX 8: TX	Y
SERCOM4	0x42001800	13			6	N	24: CORE 19: SLOW	6	N			9: RX 10: TX	Y
SERCOM5	0x42001C00	14			7	N	25: CORE 19: SLOW	7	N			11: RX 12: TX	Y
TCC0	0x42002000	15			8	N	26	8	N	4-5: EV0-1 6-9: MC0-3	34: OVF 35: TRG 36: CNT 37-40: MC0-3	13: OVF 14-17: MC0-3	Y
TCC1	0x42002400	16			9	N	26	9	N	10-11: EV0-1 12-13: MC0-1	41: OVF 42: TRG 43: CNT 44-45: MC0-1	18: OVF 19-20: MC0-1	Y
TCC2	0x42002800	17			10	N	27	10	N	14-15: EV0-1 16-17: MC0-1	46: OVF 47: TRG 48: CNT 49-50: MC0-1	21: OVF 22-23: MC0-1	Y
TC3	0x42002C00	18			11	N	27	11	N	18: EV	51: OVF 52-53: MC0-1	24: OVF 25-26: MC0-1	Y
TC4	0x42003000	19			12	N	28	12	N	19: EV	54: OVF 55-56: MCX0-1	27: OVF 28-29: MC0-1	Y

17.5.2 Power Management

The GCLK can operate in sleep modes, if required. Refer to the sleep mode description in the Power Manager (PM) section.

Related Links

PM – Power Manager

17.5.3 Clocks

The GCLK bus clock (CLK_GCLK_APB) can be enabled and disabled in the Power Manager, and the default state of CLK_GCLK_APB can be found in the Peripheral Clock Masking section of PM – Power Manager.

Related Links

PM – Power Manager

17.5.4 DMA

Not applicable.

17.5.5 Interrupts

Not applicable.

17.5.6 Events

Not applicable.

17.5.7 Debug Operation

Not applicable.

17.5.8 Register Access Protection

All registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC).

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

Write-protection does not apply for accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

17.5.9 Analog Connections

Not applicable.

17.6 Functional Description

17.6.1 Principle of Operation

The GCLK module is comprised of eight Generic Clock Generators (Generators) sourcing m Generic Clock Multiplexers.

A clock source selected as input to a Generator can either be used directly, or it can be prescaled in the Generator. A generator output is used as input to one or more the Generic Clock Multiplexers to provide a peripheral (GCLK_PERIPHERAL). A generic clock can act as the clock to one or several of peripherals.

17.8.1 Control

Name: CTRL
Offset: 0x0
Reset: 0x00
Property: Write-Protected, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
								SWRST
Access								R/W
Reset								0

Bit 0 – SWRST Software Reset
Writing a zero to this bit has no effect.

Writing a one to this bit resets all registers in the GCLK to their initial state after a power reset, except for generic clocks and associated generators that have their WRTLOCK bit in CLKCTRL read as one.

Refer to *GENCTRL.ID* for details on GENCTRL reset.

Refer to *GENDIV.ID* for details on GENDIV reset.

Refer to *CLKCTRL.ID* for details on CLKCTRL reset.

Due to synchronization, there is a delay from writing CTRL.SWRST until the reset is complete. CTRL.SWRST and STATUS.SYNCBUSY will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	There is a reset operation ongoing.

If On Demand is disabled the oscillator will always be running when enabled.

In standby sleep mode, the On Demand operation is still active if the DFLLCTRL.RUNSTDBY bit is one. If DFLLCTRL.RUNSTDBY is zero, the oscillator is disabled.

Value	Description
0	The oscillator is always on, if enabled.
1	The oscillator is enabled when a peripheral is requesting the oscillator to be used as a clock source. The oscillator is disabled if no peripheral is requesting the clock source.

Bit 4 – LLAW Lose Lock After Wake

Value	Description
0	Locks will not be lost after waking up from sleep modes if the DFLL clock has been stopped.
1	Locks will be lost after waking up from sleep modes if the DFLL clock has been stopped.

Bit 3 – STABLE Stable DFLL Frequency

Value	Description
0	FINE calibration tracks changes in output frequency.
1	FINE calibration register value will be fixed after a fine lock.

Bit 2 – MODE Operating Mode Selection

Value	Description
0	The DFLL operates in open-loop operation.
1	The DFLL operates in closed-loop operation.

Bit 1 – ENABLE DFLL Enable
Due to synchronization, there is delay from updating the register until the peripheral is enabled/disabled. The value written to DFLLCTRL.ENABLE will read back immediately after written.

Value	Description
0	The DFLL oscillator is disabled.
1	The DFLL oscillator is enabled.

22.10.4 Block Transfer Destination Address

Name: DSTADDR
Offset: 0x08
Property: -

The DSTADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	31	30	29	28	27	26	25	24
	DSTADDR[31:24]							
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	DSTADDR[23:16]							
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DSTADDR[15:8]							
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	DSTADDR[7:0]							
Access								
Reset								

Bits 31:0 – DSTADDR[31:0] Transfer Destination Address
This bit group holds the destination address corresponding to the last beat transfer address in the block transfer.

23.4 Signal Description

Signal Name	Type	Description
EXTINT[15..0]	Digital Input	External interrupt pin
NMI	Digital Input	Non-maskable interrupt pin

One signal may be available on several pins.

Related Links

I/O Multiplexing and Considerations

23.5 Product Dependencies

In order to use this EIC, other parts of the system must be configured correctly, as described below.

23.5.1 I/O Lines

Using the EIC's I/O lines requires the I/O pins to be configured.

Related Links

PORT - I/O Pin Controller

23.5.2 Power Management

All interrupts are available down to STANDBY sleep mode, but the EIC can be configured to automatically mask some interrupts in order to prevent device wake-up.

The EIC will continue to operate in any sleep mode where the selected source clock is running. The EIC's interrupts can be used to wake up the device from sleep modes. Events connected to the Event System can trigger other operations in the system without exiting sleep modes.

Related Links

PM – Power Manager

23.5.3 Clocks

The EIC bus clock (CLK_EIC_APB) can be enabled and disabled in the Power Manager, and the default state of CLK_EIC_APB can be found in the *Peripheral Clock Masking* section in PM – Power Manager.

A generic clock (GCLK_EIC) is required to clock the peripheral. This clock must be configured and enabled in the Generic Clock Controller before using the peripheral. Refer to *GCLK – Generic Clock Controller*.

This generic clock is asynchronous to the user interface clock (CLK_EIC_APB). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

Peripheral Clock Masking

GCLK - Generic Clock Controller

23.5.4 DMA

Not applicable.

- Status register (STATUS)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Related Links

PAC - Peripheral Access Controller

24.5.6 Analog Connections

Not applicable.

24.6 Functional Description

24.6.1 Principle of Operation

The NVM Controller is a slave on the AHB and APB buses. It responds to commands, read requests and write requests, based on user configuration.

24.6.1.1 Initialization

After power up, the NVM Controller goes through a power-up sequence. During this time, access to the NVM Controller from the AHB bus is halted. Upon power-up completion, the NVM Controller is operational without any need for user configuration.

24.6.2 Memory Organization

Refer to the Physical Memory Map for memory sizes and addresses for each device.

The NVM is organized into rows, where each row contains four pages, as shown in the NVM Row Organization figure. The NVM has a row-erase granularity, while the write granularity is by page. In other words, a single row erase will erase all four pages in the row, while four write operations are used to write the complete row.

Figure 24-2. NVM Row Organization

Row n	Page (n*4) + 3	Page (n*4) + 2	Page (n*4) + 1	Page (n*4) + 0

The NVM block contains a calibration and auxiliary space plus a dedicated EEPROM emulation space that are memory mapped. Refer to the NVM Organization figure below for details.

The calibration and auxiliary space contains factory calibration and system configuration information. These spaces can be read from the AHB bus in the same way as the main NVM main address space.

In addition, a boot loader section can be allocated at the beginning of the main array, and an EEPROM section can be allocated at the end of the NVM main address space.

25. PORT - I/O Pin Controller

25.1 Overview

The IO Pin Controller (PORT) controls the I/O pins of the device. The I/O pins are organized in a series of groups, collectively referred to as a PORT group. Each PORT group can have up to 32 pins that can be configured and controlled individually or as a group. The number of PORT groups on a device may depend on the package/number of pins. Each pin may either be used for general-purpose I/O under direct application control or be assigned to an embedded device peripheral. When used for general-purpose I/O, each pin can be configured as input or output, with highly configurable driver and pull settings.

All I/O pins have true read-modify-write functionality when used for general-purpose I/O; the direction or the output value of one or more pins may be changed (set, reset or toggled) explicitly without unintentionally changing the state of any other pins in the same port group by a single, atomic 8-, 16- or 32-bit write.

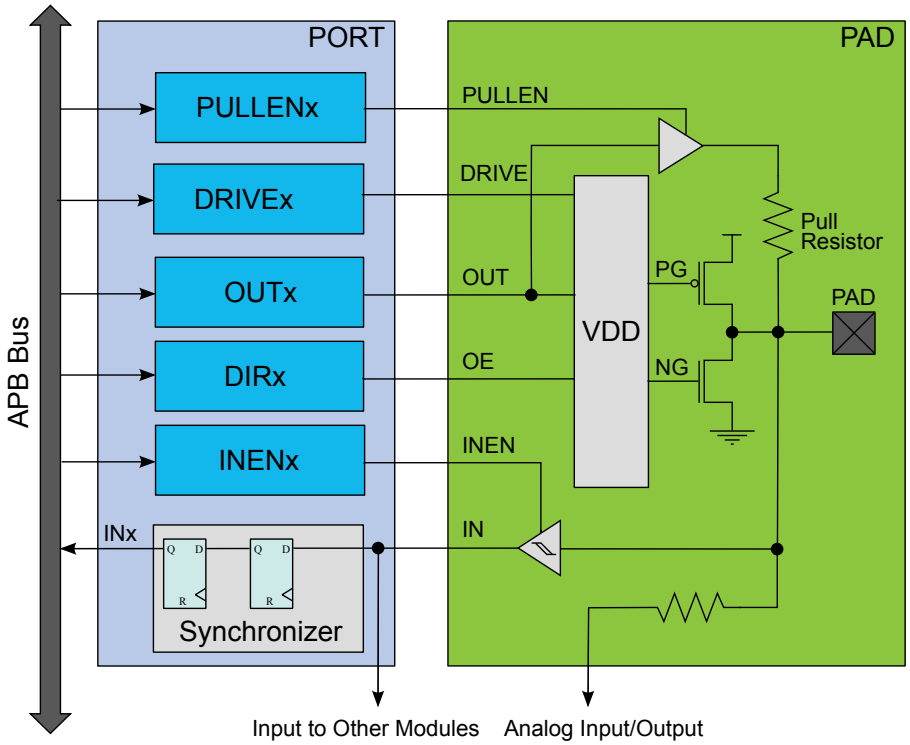
The PORT is connected to the high-speed bus matrix through an AHB/APB bridge. The Pin Direction, Data Output Value and Data Input Value registers may also be accessed using the low-latency CPU local bus (IOBUS; ARM® single-cycle I/O port) .

25.2 Features

- Selectable input and output configuration for each individual pin
- Software-controlled multiplexing of peripheral functions on I/O pins
- Flexible pin configuration through a dedicated Pin Configuration register
- Configurable output driver and pull settings:
  - Totem-pole (push-pull)
  - Pull configuration
  - Driver strength
- Configurable input buffer and pull settings:
  - Internal pull-up or pull-down
  - Input sampling criteria
  - Input buffer can be disabled if not needed for lower power consumption

25.6 Functional Description

Figure 25-2. Overview of the PORT



25.6.1 Principle of Operation

Each PORT group of up to 32 pins is controlled by the registers in PORT, as described in the figure. These registers in PORT are duplicated for each PORT group, with increasing base addresses. The number of PORT groups may depend on the package/number of pins.

Offset	Name	Bit Pos.								
		31:24	HWSEL	WRPINCFG		WRPMUX	PMUX[3:0]			
0x2C ... 0x2F	Reserved									
0x30	PMUX0	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x31	PMUX1	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x32	PMUX2	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x33	PMUX3	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x34	PMUX4	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x35	PMUX5	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x36	PMUX6	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x37	PMUX7	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x38	PMUX8	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x39	PMUX9	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x3A	PMUX10	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x3B	PMUX11	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x3C	PMUX12	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x3D	PMUX13	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x3E	PMUX14	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x3F	PMUX15	7:0	PMUXO[3:0]				PMUXE[3:0]			
0x40	PINCFG0	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x41	PINCFG1	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x42	PINCFG2	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x43	PINCFG3	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x44	PINCFG4	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x45	PINCFG5	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x46	PINCFG6	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x47	PINCFG7	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x48	PINCFG8	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x49	PINCFG9	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x4A	PINCFG10	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x4B	PINCFG11	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x4C	PINCFG12	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x4D	PINCFG13	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x4E	PINCFG14	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x4F	PINCFG15	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x50	PINCFG16	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x51	PINCFG17	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x52	PINCFG18	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x53	PINCFG19	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x54	PINCFG20	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x55	PINCFG21	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x56	PINCFG22	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x57	PINCFG23	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x58	PINCFG24	7:0		DRVSTR				PULLEN	INEN	PMUXEN
0x59	PINCFG25	7:0		DRVSTR				PULLEN	INEN	PMUXEN

25.9.1 Data Direction

Name: DIR
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to configure one or more I/O pins as an input or output. This register can be manipulated without doing a read-modify-write operation by using the Data Direction Toggle (DIRTGL), Data Direction Clear (DIRCLR) and Data Direction Set (DIRSET) registers.

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers, with a 0x80 address spacing. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

Bit	31	30	29	28	27	26	25	24
	DIR[31:24]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DIR[23:16]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DIR[15:8]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DIR[7:0]							
Access	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DIR[31:0] Port Data Direction
These bits set the data direction for the individual I/O pins in the PORT group.

Value	Description
0	The corresponding I/O pin in the PORT group is configured as an input.
1	The corresponding I/O pin in the PORT group is configured as an output.

USER[7:0]	User Multiplexer	Description	Path Type
0x07	TCC0 MC1	Match/Capture 1	Asynchronous, synchronous and resynchronized paths
0x08	TCC0 MC2	Match/Capture 2	Asynchronous, synchronous and resynchronized paths
0x09	TCC0 MC3	Match/Capture 3	Asynchronous, synchronous and resynchronized paths
0x0A	TCC1 EV0		Asynchronous, synchronous and resynchronized paths
0x0B	TCC1 EV1		Asynchronous, synchronous and resynchronized paths
0x0C	TCC1 MC0	Match/Capture 0	Asynchronous, synchronous and resynchronized paths
0x0D	TCC1 MC1	Match/Capture 1	Asynchronous, synchronous and resynchronized paths
0x0E	TCC2 EV0		Asynchronous, synchronous and resynchronized paths
0x0F	TCC2 EV1		Asynchronous, synchronous and resynchronized paths
0x10	TCC2 MC0	Match/Capture 0	Asynchronous, synchronous and resynchronized paths
0x11	TCC2 MC1	Match/Capture 1	Asynchronous, synchronous and resynchronized paths
0x12	TC0		Asynchronous, synchronous and resynchronized paths
0x13	TC1		Asynchronous, synchronous and resynchronized paths
0x14	TC2		Asynchronous, synchronous and resynchronized paths
0x15	TC3		Asynchronous, synchronous and resynchronized paths
0x16	TC4		Asynchronous, synchronous and resynchronized paths
0x17	ADC START	ADC start conversion	Asynchronous path only
0x18	ADC SYNC	Flush ADC	Asynchronous path only
0x19	AC COMP0	Start comparator 0	Asynchronous path only
0x1A	AC COMP1	Start comparator 1	Asynchronous path only
0x1B	DAC START	DAC start conversion	

26.8.4 Channel Status

Name: CHSTATUS
Offset: 0x0C
Reset: 0x000F00FF
Property: -

Bit	31	30	29	28	27	26	25	24
					CHBUSYn	CHBUSYn	CHBUSYn	CHBUSYn
Access					R	R	R	R
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
					USRRDYn	USRRDYn	USRRDYn	USRRDYn
Access					R	R	R	R
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CHBUSYn	CHBUSYn	CHBUSYn	CHBUSYn	CHBUSYn	CHBUSYn	CHBUSYn	CHBUSYn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	USRRDYn	USRRDYn	USRRDYn	USRRDYn	USRRDYn	USRRDYn	USRRDYn	USRRDYn
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 27,26,25,24,15,14,13,12,11,10,9,8 – CHBUSYn Channel n Busy [n=11..0]
This bit is cleared when channel n is idle

This bit is set if an event on channel n has not been handled by all event users connected to channel n.

Bits 19,18,17,16,7,6,5,4,3,2,1,0 – USRRDYn Channel n User Ready [n=11..0]
This bit is cleared when at least one of the event users connected to the channel is not ready.

This bit is set when all event users connected to channel n are ready to handle incoming events on channel n.

- Data register (DATA)
- Address register (ADDR)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

27.5.9 Analog Connections

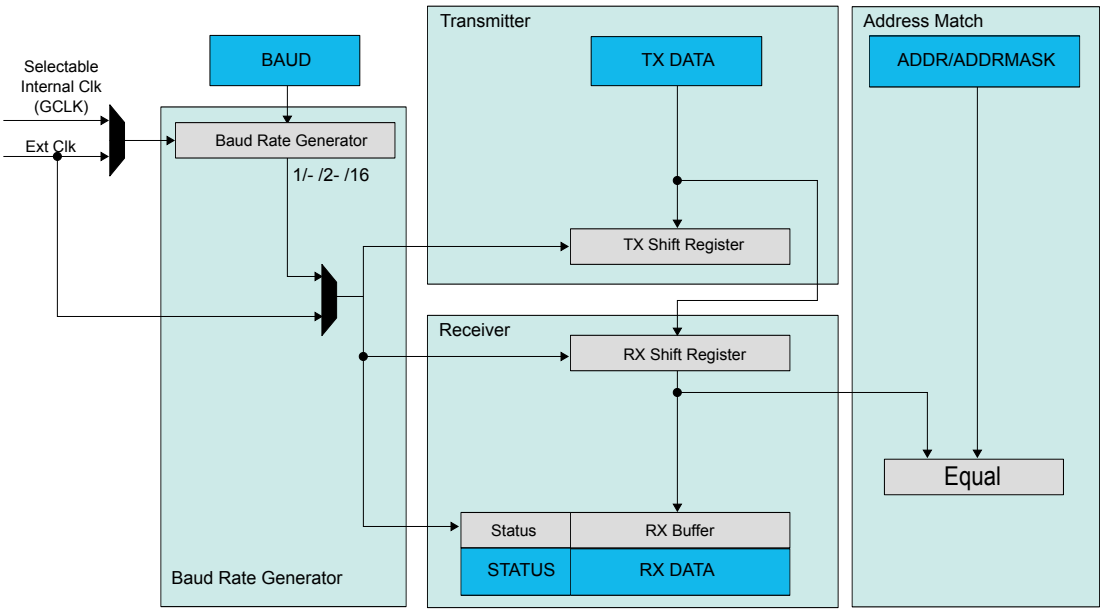
Not applicable.

27.6 Functional Description

27.6.1 Principle of Operation

The basic structure of the SERCOM serial engine is shown in Figure 27-2. Labels in capital letters are synchronous to the system clock and accessible by the CPU; labels in lowercase letters can be configured to run on the GCLK_SERCOMx_CORE clock or an external clock.

Figure 27-2. SERCOM Serial Engine



The transmitter consists of a single write buffer and a shift register.

The receiver consists of a one-level (I^2C), two-level (USART, SPI) receive buffer and a shift register.

The baud-rate generator is capable of running on the GCLK_SERCOMx_CORE clock or an external clock.

Address matching logic is included for SPI and I^2C operation.

30.8.8 Address

Name: ADDR
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
						ADDRMASK[9:7]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDRMASK[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit	15	14	13	12	11	10	9	8
	TENBITEN					ADDR[9:7]		
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[6:0]							GENCEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 26:17 – ADDRMASK[9:0] Address Mask
These bits act as a second address match register, an address mask register or the lower limit of an address range, depending on the CTRLB.AMODE setting.

Bit 15 – TENBITEN Ten Bit Addressing Enable

Value	Description
0	10-bit address recognition disabled.
1	10-bit address recognition enabled.

Bits 10:1 – ADDR[9:0] Address
These bits contain the I^2C slave address used by the slave address match logic to determine if a master has addressed the slave.

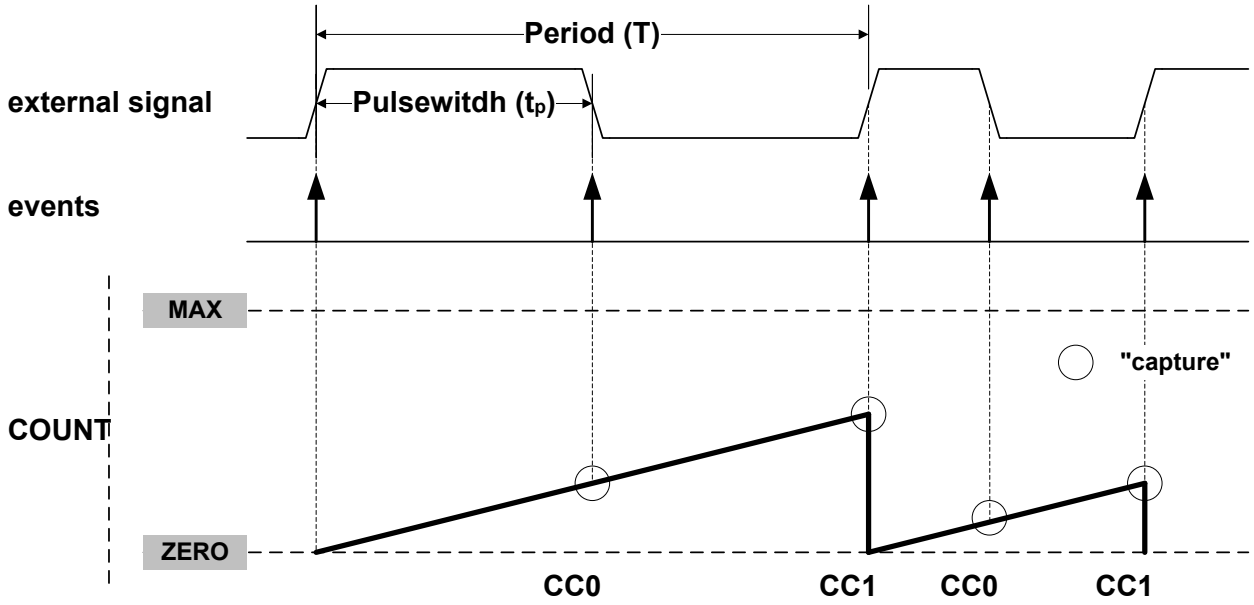
When using 7-bit addressing, the slave address is represented by ADDR[6:0].

When using 10-bit addressing (ADDR.TENBITEN=1), the slave address is represented by ADDR[9:0]

When the address match logic detects a match, INTFLAG.AMATCH is set and STATUS.DIR is updated to indicate whether it is a read or a write transaction.

Bit 0 – GENCEN General Call Address Enable
A general call address is an address consisting of all-zeroes, including the direction bit (master write).

Figure 31-10. PWP Capture



31.6.3 Additional Features

31.6.3.1 One-Shot Operation

When one-shot is enabled, the counter automatically stops on the next counter overflow or underflow condition. When the counter is stopped, the Stop bit in the Status register (STATUS.STOP) is automatically set and the waveform outputs are set to zero.

One-shot operation is enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT), and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TC will count until an overflow or underflow occurs and stops counting operation. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event, or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

31.6.4 DMA, Interrupts and Events

Table 31-3. Module Request for TC

Condition	Interrupt request	Event output	Event input	DMA request	DMA request is cleared
Overflow / Underflow	YES	YES		YES	Cleared on next clock cycle
Channel Compare Match or Capture	YES	YES		YES[1]	For compare channel – Cleared on next clock cycle. For capture channel – cleared when CCx register is read

31.8.4 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Bit	7	6	5	4	3	2	1	0
	CMD[1:0]					ONESHOT		DIR
Access	R/W	R/W				R/W		R/W
Reset	0	0				0		0

Bits 7:6 – CMD[1:0] Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Table 31-9. Command

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	-	Reserved

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

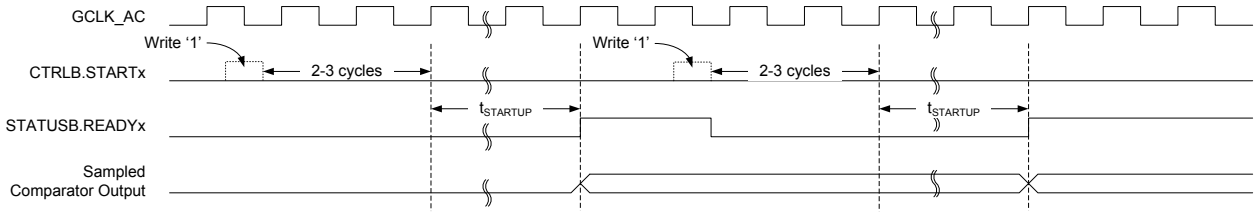
Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the bit and make the counter count up.

Figure 34-3. Single-Shot Example



For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the Power Manager will start CLK_AC_DIG. The comparator is enabled, and after the startup time has passed, a comparison is done and appropriate peripheral events and interrupts are also generated. The comparator and CLK_AC_DIG are then disabled again automatically, unless configured to wake up the system from sleep.

Related Links

Electrical Characteristics

34.6.3 Selecting Comparator Inputs

Each comparator has one positive and one negative input. The positive input is one of the external input pins (AINx). The negative input can be fed either from an external input pin (AINx) or from one of the several internal reference voltage sources common to all comparators. The user selects the input source as follows:

- The positive input is selected by the Positive Input MUX Select bit group in the Comparator Control register (COMPCTRLx.MUXPOS)
- The negative input is selected by the Negative Input MUX Select bit group in the Comparator Control register (COMPCTRLx.MUXNEG)

In the case of using an external I/O pin, the selected pin must be configured for analog use in the PORT Controller by disabling the digital input and output. The switching of the analog input multiplexers is controlled to minimize crosstalk between the channels. The input selection must be changed only while the individual comparator is disabled.

Note: For internal use of the comparison results by the CCL, this bit must be 0x1 or 0x2.

34.6.4 Window Operation

Each comparator pair can be configured to work together in window mode. In this mode, a voltage range is defined, and the comparators give information about whether an input signal is within this range or not. Window mode is enabled by the Window Enable x bit in the Window Control register (WINCTRL.WENx). Both comparators in a pair must have the same measurement mode setting in their respective Comparator Control Registers (COMPCTRLx.SINGLE).

To physically configure the pair of comparators for window mode, the same I/O pin must be chosen as positive input for each comparator, providing a shared input signal. The negative inputs define the range for the window. In Figure 34-4, COMP0 defines the upper limit and COMP1 defines the lower limit of the window, as shown but the window will also work in the opposite configuration with COMP0 lower and COMP1 higher. The current state of the window function is available in the Window x State bit group of the Status register (STATUS.WSTATEx).

Window mode can be configured to generate interrupts when the input voltage changes to below the window, when the input voltage changes to above the window, when the input voltage changes into the window or when the input voltage changes outside the window. The interrupt selections are set by the Window Interrupt Selection bit field in the Window Control register (WINCTRL.WINTSEL). Events are

Description	Symbol	Max.	Unit
DAC input clock frequency	f_{GCLK_DAC}	350	kHz
PTC input clock frequency	f_{GCLK_PTC}	48	MHz

37.8 Power Consumption

The values in Table 37-13 are measured values of power consumption of the microcontroller through the VDDIN, VDDIO and VDDANA pins under the following conditions, except where noted. Note that the values are given for case temperatures. The power consumption of the SBC through the VS pin found in Table 37-6 has to be added to obtain the full power consumption for the device.

- Operating conditions
  - V_{VDDIN} = 3.3 V
  - V_{VDDIN} = 2.7V, CPU is running on Flash with 1 wait state
- Wake up time from sleep mode is measured from the edge of the wakeup signal to the execution of the first instruction fetched in flash.
- Oscillators
  - XOSC (crystal oscillator) stopped
  - XOSC32K (32 kHz crystal oscillator) running with external 32kHz crystal
  - DFLL48M using XOSC32K as reference and running at 48 MHz
- Clocks
  - DFLL48M used as main clock source, except otherwise specified
  - CPU, AHB clocks undivided
  - APBA clock divided by 4
  - APBB and APBC bridges off
- The following AHB module clocks are running: NVMCTRL, APBA bridge
  - All other AHB clocks stopped
- The following peripheral clocks running: PM, SYSCTRL, RTC
  - All other peripheral clocks stopped
- I/Os are inactive with internal pull-up
- CPU is running on flash with 1 wait states
- Cache enabled
- BOD33 disabled

Table 37-13. Current Consumption

Mode	Conditions	T_{VJ}	V_{CC}	Typ.	Max.	Unit
ACTIVE	CPU running a While(1) algorithm	25°C	3.3V	3.32	3.63	mA
		105°C	3.3V	3.57	3.98	
	CPU running a While(1) algorithm, with GCLKIN as reference	25°C	3.3V	64 × Freq + 110	70 × Freq + 131	µA (with freq in MHz)
		105°C	3.3V	65 × Freq + 342	65 × Freq + 764	